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High Voltage Buck Converter Topology for Common Mode Voltage Reduction

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Abstract - **A new DC buck converter topology to actively reduce common mode voltage applied to the load is presented in this paper. The supply is designed to interface universal input DC-DC power supplies to a rectified 480 Vac (700 Vdc) bus. By minimizing the common mode voltage produced, the size and cost of the passive filter elements can be significantly reduced. In the topology presented, an additional switching device to cancel the common mode voltage augments the traditional buck converter. Canceling the common mode voltage reduces the EMI filter requirements. It is shown that the switching losses remain unchanged while the voltage rating of the switching devices can be reduced. By using de-rated devices, the cost of the converter is reduced.**

I. INTRODUCTION

Over the past few years, problems created by Electromagnetic Interference (EMI) have significantly increased due, mainly, to the proliferation of solid state power converters. Traditionally, the most popular method of EMI mitigation is passive filtering techniques at a significant size and cost penalty. As an alternative to passive filtering for common mode conducted EMI mitigation, a modification to the circuit topology is presented that actively cancels the common mode voltage created by the converter. This concept has been applied to three phase and six phase inverters [1,2,3]. To date no references have been identified that apply this technique to a DC-DC buck converter. Here, active cancellation of common mode (CM) voltage is applied to a simple buck converter however, this technique can be used in many power electronic topologies.

The purpose of this work is to develop a DC-DC converter to produce control power for a three-phase inverter intended to meet the EMI specifications of MIL STD 461D. Many inverters fail conducted EMI tests before power to the load is even applied due to EMI generated by the internal power supplies [4]. For this reason, to meet today's stringent specifications, attention must be given to any sub-system that would contribute to the overall EMI production.

In this particular case, no isolation in the DC converter was included, as the scope was to produce a voltage level suitable for a universal input, commercial DC-DC power supply from a 700V DC bus. Most universal power supplies cannot accommodate a 700Vdc bus input.

In the topology presented, an additional active switching device and a split winding inductor to cancel the CM voltage augments the traditional buck converter topology. As the cost of solid state devices continues to decrease, such active filter alternatives to bulky, expensive magnetics, such as CM chokes, become more attractive.

II. TWO SWITCH BUCK CONVERTER OPERATION

A. *Topology*

Fig. 1 shows the proposed buck converter topology. The two solid state switches in Fig. 1 are identical and require no additional control logic since they both receive the same gate signal.

When the two switches are on, the DC source voltage is applied to the filter inductor terminals. The positive inductor terminal (V_{ch1}) switches to +Vdc/2 while the negative inductor terminal (V_{ch2}) switches to –Vdc/2. The CM voltage applied is defined as,

$$V_{cm} = \frac{V_{ch1} + V_{ch2}}{2} \qquad (1)$$

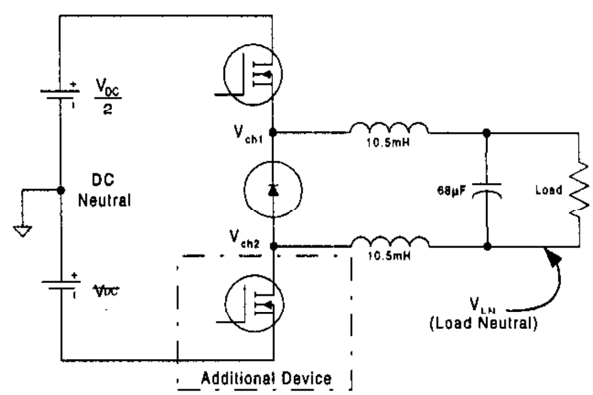

Figure 1 - Buck converter topology for CM voltage reduction

which in this case is zero because $V_{ch1} + V_{ch2} = 0$. When the switches are off, the CM voltage applied to the filter inductor terminals (with respect to the DC neutral) is again zero, provided the switching devices share the voltage equally.

However, this is no guarantee that the output will not see a CM voltage. In order to preserve the CM voltage cancellation, the filter inductor must be split as shown in Fig. 1. Splitting the inductor balances the inductor voltage with respect to the DC neutral. The combination of the extra switch and the split inductor is essential to common mode cancellation in this topology.

Fig. 2 shows a simulation of the two-switch buck converter operation under continuous conduction conditions. At all times, the CM voltage as defined in (1) is zero.

B. *Device Voltage Sharing*

When two devices are operated in series combination there is no guarantee of the degree to which they will share the voltage due to device parameter tolerances. Differences in leakage current can cause static voltage unbalance. Likewise, other device or gate drive tolerances give rise to differing switching speeds, which can cause dynamic voltage unbalance. Therefore, steps must be taken to ensure proper voltage sharing of the two switching devices.

To do this, snubber circuits are incorporated. The snubber circuit shown in Fig. 3 provides both static and dynamic voltage sharing [5]. The snubber capacitor C_D is sized to minimize the voltage difference between the two switches during turn-off, while the parallel resistance ensures static voltage sharing.

If the snubber can force the switches to share the voltage evenly, under all operating conditions including power up and power down, then the switch voltage rating can be reduced with respect to the voltage rating required if only one switch were used.

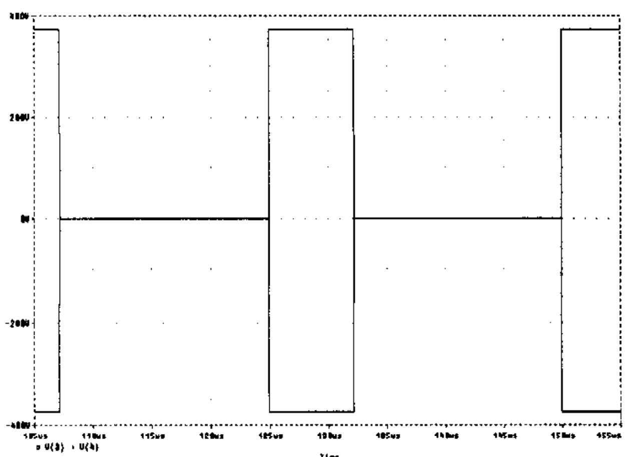

Figure. 2 - Simulated voltage waveforms (V_{ch1} and V_{ch2}) for a buck converter with extra MOSFET

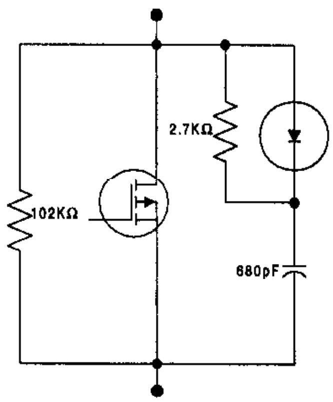

Figure 3 – Snubber circuit to ensure proper voltage sharing between series devices

For MOSFET devices, Table 1 data shows the cost of a 500V device is less than one third of that for a 1000V device. Because no additional control hardware is required to drive two switches since they are operated simultaneously, this represents a cost saving to the circuit design.

TABLE 1
MOSFET COST/VOLTAGE RATING COMPARISON

Manuf.	Part No.	V_{DSS} [V]	I_D [A]	R_{DSon} [Ω]	List Price [US $]
IR	IRFPG50	1000	6.1	2	$ 21.73 *
	IRF840	500	8	0.8	$ 4.50
Motorola	MTW6N100E	1000	6	1.5	$ 13.08 **
	MTP8N50E	500	4	0.8	$ 3.01
Harris	IRFP640	1000	4.3	3.5	$ 7.00 *
	IRF830	500	4.5	1.5	$ 2.30

* Newark Electronics Catalog #115, 1997
** Digi-key Catalog, #976B, Nov-Dec, 1997

Table 1 also shows that the on state resistance of the lesser-rated device is less than half that of the higher voltage device. Because the two devices see the same current as would the one higher voltage device, the conduction losses will remain the same, or be slightly reduced.

III. EXPERIMENTAL RESULTS

A prototype printed circuit board for the new topology has been constructed. The original design, the results of which are presented here, was an open control loop power supply. This was done mainly for simplicity sake, however implementing a closed loop control would not effect the results regarding its CM voltage reduction capabilities.

Initial measurements at low voltage have been recorded. The laboratory results correlate well with the simulation (Fig. 2) as is shown in Fig. 4.

Channel 1 (V_{ch1}) is the source voltage of the upper device and channel 2 (V_{ch2}) is the drain voltage of the lower device both with respect to the DC neutral. (The nodes are indicated on the circuit of Fig. 1).

The common mode voltage applied to the load is measured at the load neutral with respect to the DC bus neutral (V_{LN}). Fig. 5 compares the V_{LN} waveform of the circuit when the additional MOSFET is utilized (referred to here as the two switch topology) to that measured when one device is shorted drain to source (rendering the traditional one switch topology).

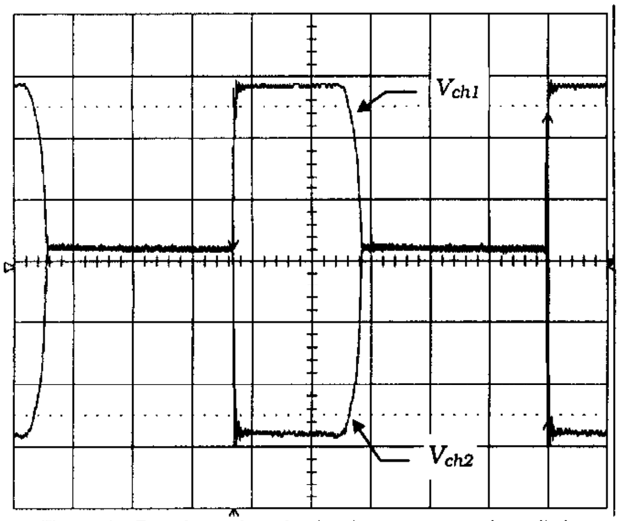

Figure. 4 – Experimental results showing common mode applied to the filter inductor terminals for two switch buck converter topology. (50V/div, 5• s/div)

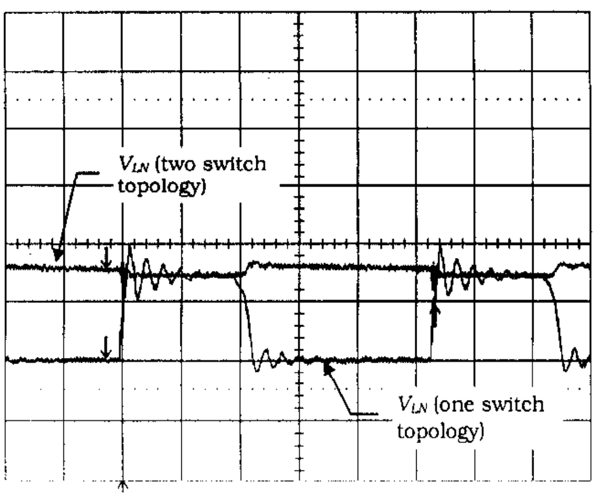

Figure 5 - Common mode voltage comparison between one and two switch buck converter. (100V/div, 5µs/div)

The size of the magnetics required to effectively filter the CM current is driven by the lowest frequency component of the CM voltage waveform. As can be seen from Fig. 5, the lowest frequency component of the CM voltage is at the switching frequency and it has been drastically reduced by the addition of the extra device.

The higher frequency components result from parasitic resonance excited by the high dv/dt of the main CM voltage. When the main component is reduced, it may also result in a reduction of higher frequency components as well.

Additional attenuation was achieved by adding a small bypass capacitor (27µF) from the V_{L+} terminal to the positive DC bus, and another from the V_{LN} terminal to the negative DC bus. The CM voltage measured after the addition of the extra filter capacitors is shown in Fig. 6. With the two switch topology, this capacitor sees virtually no AC voltage component. Therefore, less expensive capacitors may be used as the ESR is no longer an issue.

The harmonic spectrum of V_{LN} with respect to DC neutral for the two topologies is compared in Figs. 7 and 8. As the figures show, the lower frequency CM voltage for the two switch converter has been reduced by a factor of approximately 50dB with respect to that of the one switch topology.

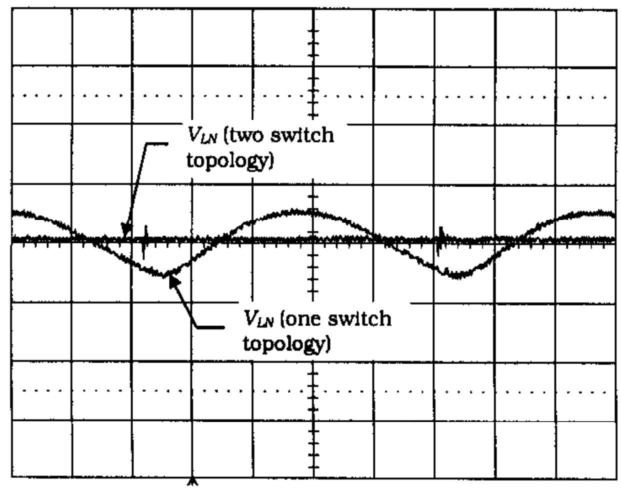

Figure 6 – Common mode voltage after addition of small filter capacitor. (100V/div, 5µs/div, ac coupled)

Fig. 9 shows the experimental circuit board used to obtain the experimental results

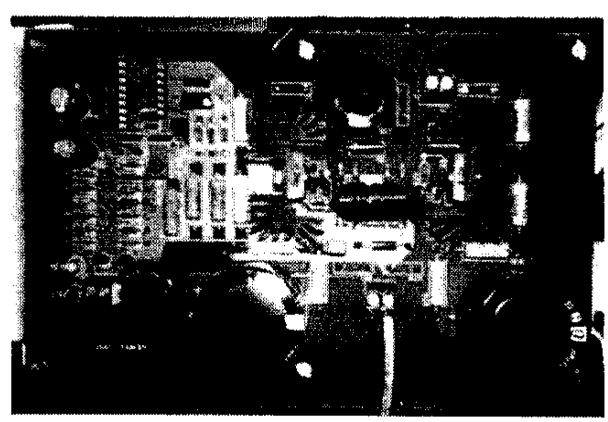

Figure 9 – Experimental circuit board

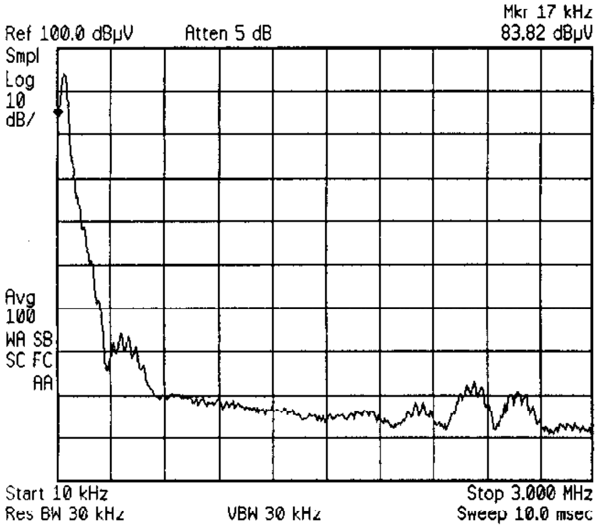

Figure 7 – Common mode voltage spectrum of one switch buck converter topology. (200V/V with 10dB external attenuation)

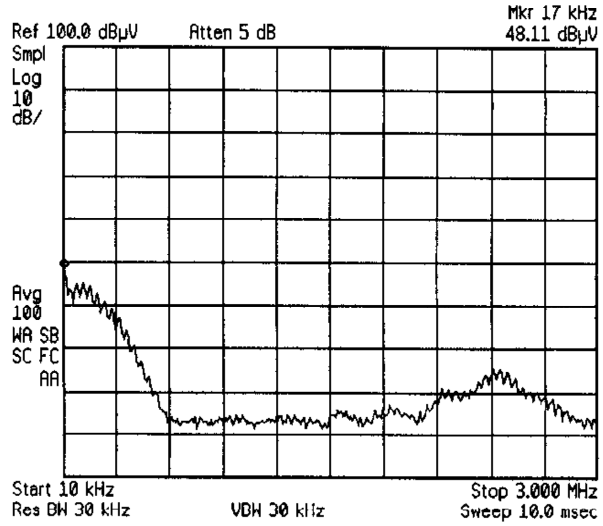

Figure 8 – Common mode voltage spectrum of two switch buck converter topology (200V/V with 10dB external attenuator)

IV. CONCLUSION

A buck converter topology using two de-rated switching devices and a split inductor to actively reduce CM voltage has been presented. By actively reducing CM voltage, the size and cost of the magnetic components required to filter it are reduced. In addition, for high voltage applications, due to the relative cost of de-rated switching devices (500V MOSFET vs. 1000V), this topology may even result in a cost saving to the circuit. A power supply has been constructed and has been shown to significantly reduce the CM voltage over the traditional one switch buck converter topology.

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