Research Report

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Investigation of a Modified Single Phase Inverter Topology for Reduction of Common Mode Voltage

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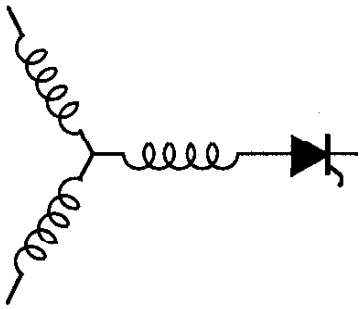

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(*Topic Category* : Industrial Power Converters)

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Abstract

Switching frequencies of power electronic converters have been on the rise in recent years due to advances in power semiconductor technology. This has led to significant increases in their levels of EMI. Several techniques of attenuating conducted EMI have been developed over the years, a significant number of which rely on the use of passive filters. This paper addresses the problem of common mode conducted EMI reduction in single phase PWM inverters by investigating a novel topology to actively cancel the common mode voltage applied to the load. The size and cost of passive filter components can be significantly reduced by minimizing the common mode voltage applied to the load. In the topology proposed, two additional switching devices (to perform the function of one bidirectional device) are added to the conventional single phase inverter to minimize the common mode voltage applied to the load. Operating principles and experimental results will be discussed in the paper. The performance of the proposed topology will be compared to that of the conventional single phase inverter in order to determine its efficacy.

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Digest

In recent years, the levels of EMI generated by power electronic converters have increased significantly as a result of faster switching semiconductor devices. One of the most widely used techniques for EMI reduction has been the use of passive filters [1]. The use of these filters (such as common mode chokes), unfortunately, is associated with a significant cost, size and weight penalty. The application of active filtering techniques, however, can significantly reduce their size and cost. With the recent improvements in power semi-conductor technology, the cost of solid-state switching devices has been continually falling. The use of active techniques for EMI reduction, therefore, is becoming both feasible and attractive. In the recent past, these techniques have been applied for the reduction of conducted EMI in polyphase inverters and drives [2,3]. This paper proposes a novel topology for the reduction of conducted common mode EMI in single phase inverters. Minimizing the common mode voltage applied to the load would enable a considerable reduction in the size and cost of passive filters required for EMI reduction.

A schematic diagram of the proposed single phase inverter topology is shown in Figure 1. In this topology, the conventional single phase inverter (Figure 2) is augmented by two additional switching devices which perform the function of one bidirectional switching device ("S_B"). The inverter maybe operated so as to generate a sinusoidal pulse width modulated output voltage. The switches S5 and S6 are gated on when the switching algorithm demands a zero output voltage state. These switches therefore serve to balance the switching pattern of the inverter.

In contrast, in the conventional single phase inverter (Figure 2), the zero state is implemented by switching either devices S1 and S3 or S2 and S4. Clearly therefore, during this state, the

common mode voltage (with respect to the mid-point of the DC bus) applied to the load becomes [5] :

$$V_{cm} = \frac{V_1 + V_2}{2} = \pm \frac{V_{dc}}{2} \qquad \ldots[1]$$

During other switching states, the common mode voltage applied to the load is theoretically zero. Since the operation of a single phase inverter involves the alternation of non-zero and zero switching states, the common mode voltage pulsates at the switching frequency of the inverter. This oscillation results in conducted common mode EMI. Clearly, this problem becomes increasingly serious as switching frequencies increase and necessitates the use of large passive filtering components.

In the case of the proposed topology however, the zero state is synthesized by the operation of switches S5 and S6 (all the other switches are off). Assuming equal voltage sharing across both inverter legs, the common mode voltage applied to the load is clearly zero (from equation [1]). The oscillation of common mode voltage is therefore theoretically eliminated by the proposed topology. In practice however, a relatively small common mode filter may have to be used to cancel the common mode voltage applied to the load, since device dependencies and other non-idealities will inevitably result in imperfect voltage balancing.

The operation of the proposed topology was simulated and the resulting common mode voltage is compared with that of the conventional topology in Figure 3. It is seen from the Figure that the proposed topology indeed attenuates the common mode voltage applied to the load. Further, the load current wave-form of the proposed inverter topology (Figure 4) is seen to be virtually indistinguishable from that of a conventional single phase inverter.

The preceding discussion indicates that the proposed topology would result in a significant reduction of the cost and size of passive filters required for EMI reduction. This would be particularly beneficial for single phase inverter applications such as uninterruptible power supplies. A point to be borne in mind, however, is that the use of the two additional switching devices represents a cost penalty. Also, the switching losses of the inverter are increased due to the additional switching devices, necessitating more effective heat sinking. With the reduction in prices of power semiconductor devices, however, the cost penalty associated with the use of additional devices is not likely to be severe and the economic impact of the proposed topology is likely to be beneficial in most applications requiring stringent adherence to EMI limits.

Laboratory testing of the proposed topology is being carried out to establish the validity of the theoretical and simulation results and will be presented in the complete paper.

References

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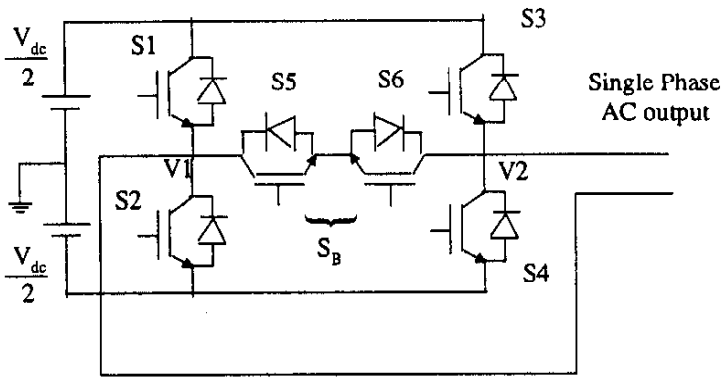
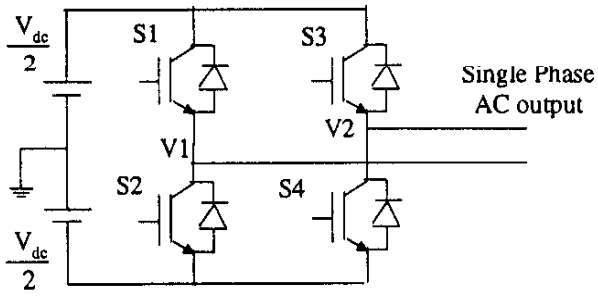
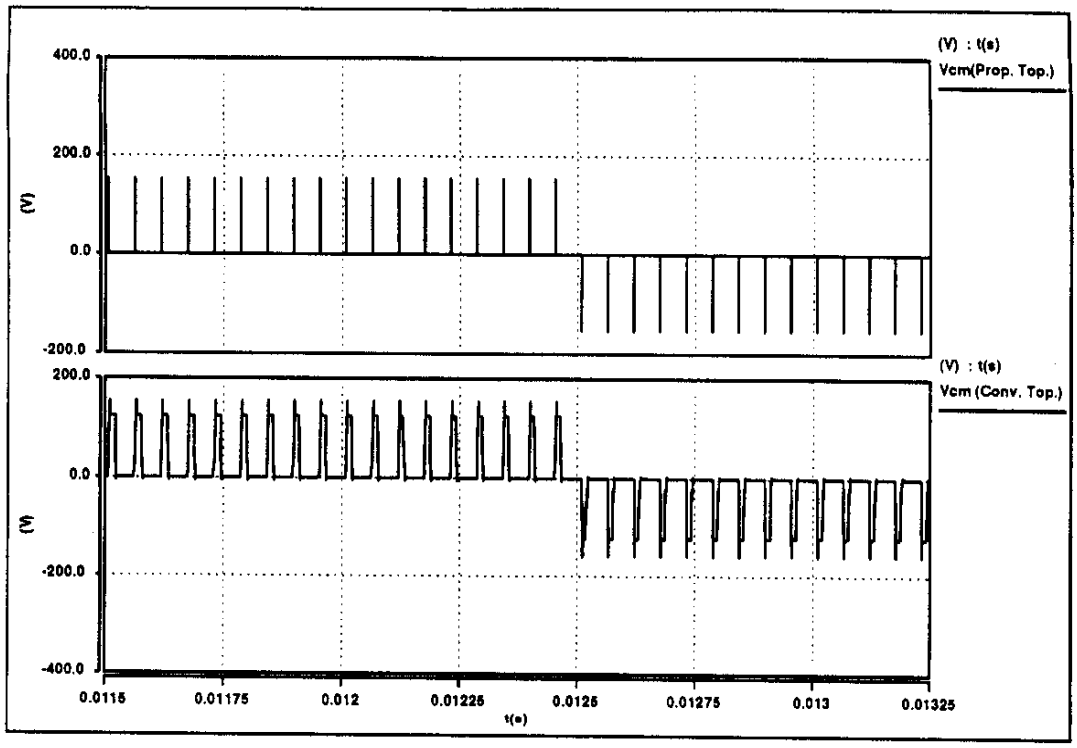


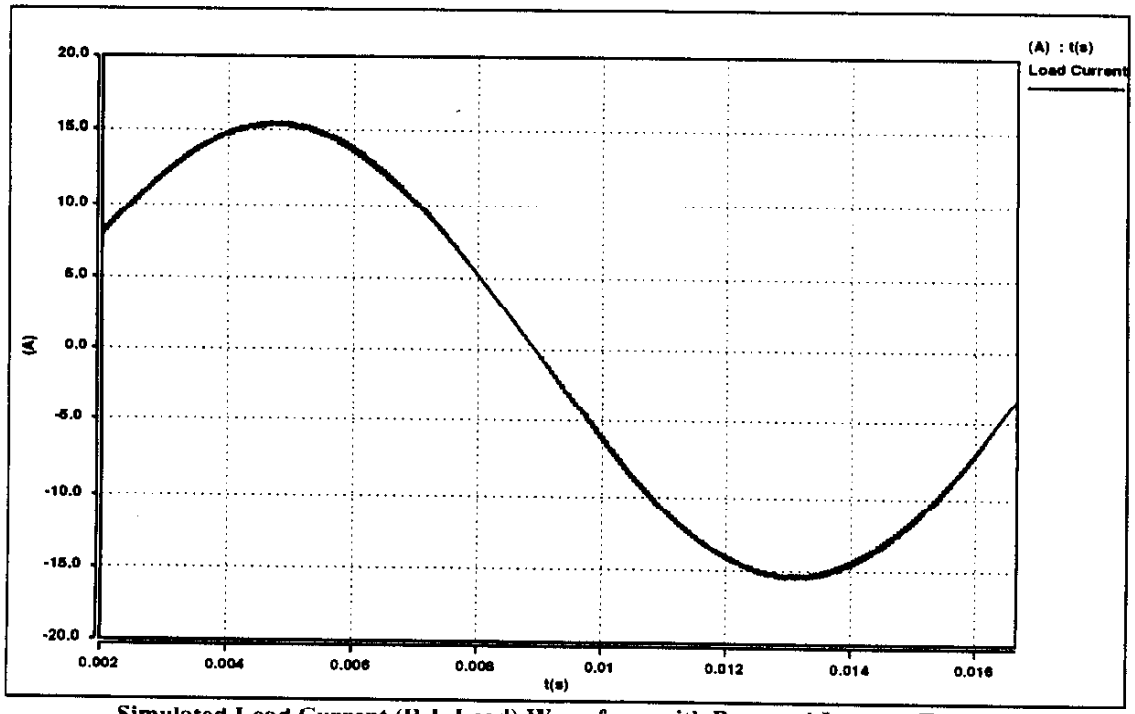
Proposed Topology for Active Common Mode Voltage Cancellation
Figure 1



Conventional Single Phase Inverter Topology
Figure 2



Simulated Common Mode Voltage Waveforms of Conventional and Proposed Inverter Topologies
(Inverter Rating : 250 V-DC to 1 ϕ AC, 2 kW; Switching Frequency : 18 kHz)
Figure 3



Simulated Load Current (R-L Load) Wave-form with Proposed Inverter Topology
Figure 4