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Switching Angles and DC Link Voltages Optimization for Multilevel Cascade Inverters

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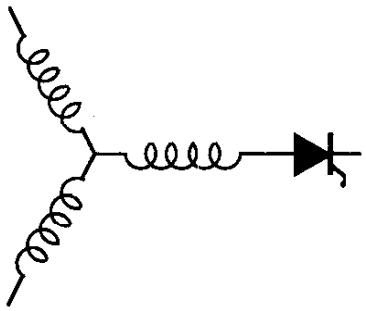

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Abstract

Semiconductor switch ratings and problems concerned with series connection of these switches have limited the development of high power inverters. This limitation can be overcome by the multilevel structure for the voltage source inverter [1-3]. The concept of multilevel inverter drives was introduced by Bhagwat and Stefanovic [1] in 1983. The structure, being based on the Neutral Point Clamped (NPC) inverter topology [2], has attractive features such as reduced voltage and current THDs, higher output voltages using devices of lower ratings and reduced dv/dt stresses. However, as the number of levels increase, the NPC based multilevel inverters become difficult to control. In this case, the topology using modular H bridges in a cascade connection has been preferred [3,4], where the generation of M-level voltage waveforms can easily be produced by cascading (M-1)/2 H-bridges. Such extension is much more difficult in the case of NPC type multilevel inverters.

The cascade inverter appears to be superior to other multilevel structure inverters in applications at higher power ratings. When such applications are considered, most of them do not require too high a dynamic response, but an excellent harmonic performance is a necessity for cleaner power, high efficiency and less electromagnetic interference. The suitable switching strategies are those based on the fundamental frequency switching with minimum weighted total harmonic distortion (WTHD).

Previous work in the area of fundamental switching for multilevel cascade inverter is highlighted by the pulse width optimization technique proposed in [4], where the switching angle of each H bridge is optimized, so that the resulting staircase output voltage has the minimum harmonic content. The dc link voltage of each level is assumed to be the same and constant.

As an extension to this work the optimization of both dc link voltages and switching angles of the output waveform is investigated in this paper. With the addition of one more degrees of freedom in the optimization, harmonic minimization is demonstrated to be substantially improved.

Digital simulation results of optimized values and WTHD for both 7-level and 5-level cascade inverters are presented and compared with those of pulse width optimization technique as well as the six-step switching technique.

Switching Angles and DC Link Voltages Optimization for Multilevel Cascade Inverters

1. Introduction

Semiconductor switch ratings and problems concerned with series connection of these switches have limited the development of high power inverters. This limitation can be overcome by the multilevel structure for the voltage source inverter [1-3]. The concept of multilevel inverter drives was introduced by Bhagwat and Stefanovic [1] in 1983. The structure, being based on the Neutral Point Clamped (NPC) inverter topology [2], has attractive features such as reduced voltage and current THDs, higher output voltages using devices of lower ratings and reduced dv/dt stresses. However, as the number of levels increase, the NPC based multilevel inverters become difficult to control. In this case, the topology using modular H bridges in a cascade connection has been preferred [3,4], where the generation of M-level voltage waveforms can easily be produced by cascading (M-1)/2 H-bridges. Such extension is much more difficult in the case of NPC type multilevel inverters.

The applications of the multilevel cascade inverter to ac drives and static VAR generation have the same circuit configuration for the inverter portion. However, the interfaces of the portion with the utility differ from each other, as is the case for the two level system. Fig. 1 shows the single-phase configuration of the two applications for a 7-level voltage source cascade inverter. In Fig.1 (a), the cascade inverter is used as ac drives [3,5], each H-bridge is powered by an isolated secondary winding of an integral isolation transformer, which are wound to obtain a phase angle difference by multiples of 20° for 3 H bridges in cascade. In this manner, the harmonic cancellation between the reflected secondary current is caused to produce an 18-pulse primary current. The lowest harmonic that is not cancelled is the 17^{th}.

In the case of using cascade inverter for static VAR generation [4], the H-bridge is directly connected to the utility, from which the dc source of each H-bridge is supplied as shown in Fig.1(b). The regulation of the dc link voltage is closely related to the operation of the inverter. This arrangement is different from the structure of Fig.1(a), where the dc source is supplied via the rectifier and is independent from the operation of the inverter. This difference must be taken into account in the control of the cascade inverter.

The cascade inverter appears to be superior to other multilevel structure inverters in applications at higher power ratings. When such applications are considered, most of them do not require too high a dynamic response, but an excellent harmonic performance is a necessity for cleaner power, high efficiency and less electromagnetic interference. The suitable switching strategies are those based on the fundamental frequency switching with minimum weighted total harmonic distortion (WTHD). The fundamental frequency switching requires each device to be switched on and off just once per cycle of the fundamental frequency output.

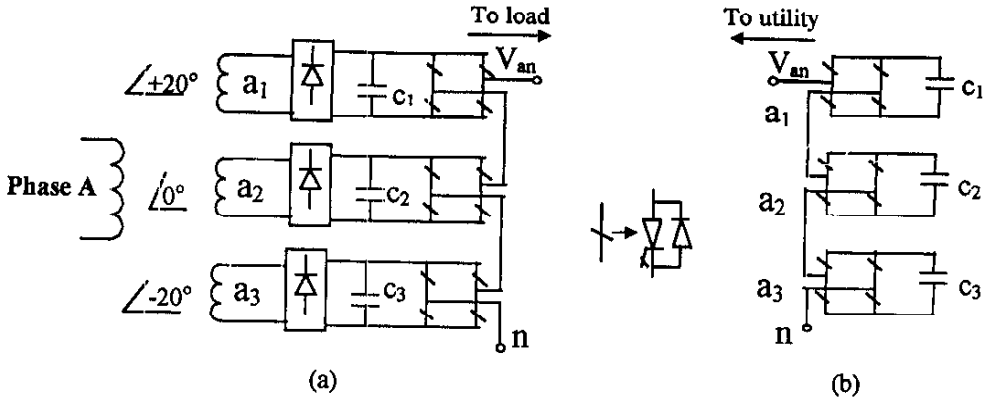

Fig.1 Single phase structure of a 7-level cascade inverter
(a) for AC drives. (b) for static var generation.

Previous work in the area of fundamental switching for multilevel cascade inverter is highlighted by the pulse width optimization technique proposed in [4], where the switching angle of each H bridge is optimized, so that the resulting staircase output voltage has the minimum harmonic content. The dc link voltage of each level is assumed to be the same and constant.

As an extension to this work the optimization of both dc link voltages and switching angles of the output waveform will be investigated in this paper. With the addition of one more degrees of freedom in the optimization, harmonic minimization is demonstrated to be substantially improved.

2. Review of switching strategies for the cascade inverter

Most switching strategies applied to control a single H-bridge inverter are ready to be extended to a multilevel cascade inverter with certain modifications to take the full advantage of the multilevel structure. The selection of specific switching strategy depends on given performance specifications. To achieve high-dynamic response the hysteresis band current control method and the sine PWM technique for a multilevel structure were proposed in [3, 5]. If the minimum harmonic content in the output voltage is a main concern, then switching at the fundamental frequency with switching angle optimization at each voltage level is preferred [4]. The latter is exclusive to the multilevel structure, where the access to each level of the dc voltages is possible. In [4] each dc voltage was maintain at the same level, E_d, while the switching angle of each bridge is optimized for minimum harmonic distortion of the output waveform.

To take the full advantage of the separate control of dc link voltages of the cascade inverter, the optimizations of both dc voltages and switching angles is explored in this paper. When both the pulse height and the pulse width are optimized, harmonic performance is greatly enhanced.

A case study approach is taken to investigate this technique, where the 7-level cascade inverter of Fig.1 is used as an example. In Fig.1, each H-bridge has its own dc source E_1,

E_2, and E_3, respectively, and is isolated from one another. If each H-bridge is to be switched to E_1 at α_1, E_2 at α_2 and E_3 at α_3 respectively, the output waveform produced is the staircase-type as show in Fig.2 for phase a, V_{an}. The outputs of phase b and c are 120° phase shift from V_{an}. The Fourier coefficients of the output voltage are calculated as the simple sum of the coefficients of the three rectangular waves:

$$H(n) = \frac{4}{\pi}\frac{1}{n}[E_1\cos(n\alpha_1) + E_2\cos(n\alpha_2) + E_3\cos(n\alpha_3)] \quad \text{.....(1)}$$

Where n=1, 3, 5, 7, ...

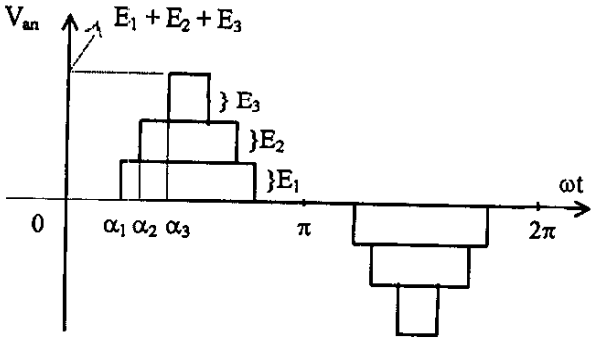

Fig.2 Switched output voltage of the 7-level cascade inverter.

From (1) one can derive two control options for the output voltage:

1. The dc voltages E_i's remain constant at a same level, $E_1 = E_2 = E_3$, and angles α_i varied to control the fundamental voltage as proposed in [4];
2. The angles α_i remain constant at their optimal values, whereas the dc voltage steps are varied to control the fundamental component of the output voltage, as proposed in this paper.

The first and second methods, hereafter are referred to as option 1 and option 2 respectively in the following sections.

3. Option 1 technique

Option 1 is a pulse width control at a constant dc voltage E_d. The fundamental output voltage, $H(1)$, is controlled by switching angles which can be optimized by eliminating the lowest harmonics while achieving the target fundamental voltage output. Different cost functions are required for the optimization depending on the modulation index concerned. If the modulation index, M, is defined as the ratio of H(1) or V_{com}, to that of the six-step output, having a voltage level of $3E_d$ and zero switching angles, then we have

$$M = V_{com} / (3E_d \frac{4}{\pi}\} \quad \text{.....(2)}$$

where V_{com} is the voltage command. To optimize switching angles α_1, α_2, and α_3 at $M = M_{max}$, the cost function, f_{cost}, is defined as:

$$f_{cost} = \begin{cases} H(5) = 0 \\ H(7) = 0 \text{.....} for.(M = M_{\max}) \text{.....(3)} \\ H(11) = 0 \end{cases}$$

It can be seen that the 5th, 7th and 11th harmonics are eliminated in this case. Solving (3) for α_1, α_2, and α_3, and calculating $H(1)$ in terms of (1), $M_{max} = 0.92$ can be obtained by substituting resulting H(1) into (2). This implies that with these constraints the maximum fundamental voltage output attainable is 92% that of the six-step output voltage.

For other values of M ($0 < M < M_{max}$), the cost function differs from (3) in that the target fundamental voltage, $H(1)$, has to be defined in the cost function, and leave only the 5th and 7th harmonics to be eliminated as given in (4):

$$f_{cost} = \begin{cases} H(1) - \frac{12}{\pi} E_d \times M = 0 \\ H(5) = 0 \text{.....} for.(0 < M < M_{\max}) \text{....(4)} \\ H(7) = 0 \end{cases}$$

4. Option 2 technique

The second option is the approach proposed and investigated in this paper. The technique requires the regulation of dc link voltage at different levels in addition to that of switching angles, so that not only the pulse width but also the pulse height of the output voltage can be optimized. To proceed with the dc voltage optimization, it is useful to define

$$\begin{aligned} E_1 &= E_d \\ E_2 &= E_d + \Delta e_1 \\ E_3 &= E_d + \Delta e_2 \end{aligned} \qquad (5)$$

where Δe_i represents the voltage incremental portion of E_d. It is convenient to introduce the per unit value approach into the dc voltage optimization by normalizing variables in (5) to
E_d. Substituting (5) into (1), the Fourier coefficients of the output voltage is rewritten:

$$H(n) = \frac{4}{\pi} \frac{1}{n} \left\{ E_d [\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] + \Delta e_1 \cos(n\alpha_2) + \Delta e_2 \cos(n\alpha_3) \right\} \text{.....(6)}$$

It is useful to keep in mind that E_d is equal to one and Δe_1 and Δe_2 are per unit values when using (6) for optimization. With the introduction of the voltage increments Δe_1 and Δe_2, the number of variables to be optimized are increased to 5, including the three switching angles α_i. Harmonics up to the 17th can be eliminated in the cost function of option 2 :

$$f_{cost} = \begin{cases} H(5) = 0 \\ H(7) = 0 \\ H(11) = 0 \\ H(13) = 0 \\ H(17) = 0 \end{cases} \quad \text{.....(7)}$$

Substituting (6) into (7) and solving the 5 equations for the five unknowns in (7) yields optimal values of Δe_1, Δe_2, α_1, α_2, and α_3. Once the optimal values are found, they should be kept constant over the entire modulation range to maintain the best harmonic performance. Whereas the amplitude of the fundamental component of the output waveform can be controlled by the dc link voltages E_1, E_2, and E_3, as defined in (5), according to the nominal value E_d:

$$E_d = \frac{V_{com}\pi}{4k} \text{.....(8)}$$

Where k consists of the five optimal values and is a constant after optimization:

$$k = \cos\alpha_1 + (1 + \Delta e_1)\cos\alpha_2 + (1 + \Delta e_2)\cos\alpha_3 \text{.....(9)}$$

If the modulation index defined in (2) is used, then $M_{max} = k/3$ can be obtained in (10) below. However, as the principle of the option 2 technique allows for a variable E_d to be operated, the M_{max} is not limited by k but by E_{d_max}. This is a unique feature of option 2.

$$M_{max} = \frac{4}{\pi} E_d \times k / (3E_d \times \frac{4}{\pi}) = k/3 \text{.....(10)}$$

5. Harmonic analysis

To measure the harmonic performance of option 1 and 2 for purpose of comparison, the weighted THD (WTHD), which evaluates harmonics in the line current into an inductive load, was chosen as criteria. The WTHD is defined in (11) as the rms value of the harmonic voltages (line-to-line) normalized to the maximum fundamental voltage and divided by the harmonic number, n. For fundamental switching, harmonic numbers up to $n = 50$ is used in this study and is found to be adequate.

$$WTHD = \frac{\sqrt{\sum_{i=2}^{n} (\frac{V_i}{i})^2}}{V_1} \text{.....(11)}$$

Where V_i is the harmonic components of the switched line voltage obtained by subtracting the switching phase voltages from each other. The phase leg output voltages can be formed by optimal values of dc voltages and switching angles as shown in Fig.2. The digital solution for the WTHD in (11) was obtained using the FFT capability of the MatLab package to analyze the simulated switched line voltage waveform, $V_{ab}(.)$. The MatLab solution is an accurate representation of a real inverter output under the same modulation conditions, with the exclusion of crossover delay effects. However, this

simplification involved in neglected crossover delay does not affect the conclusions of this paper. The following tasks have been performed in the digital simulation:

1. invoke the optimization process;
2. generate the waveform of inverter output line voltage;
3. perform a harmonic analysis of the line voltage.

The simulation results are given in the following section.

6. Digital simulation results

Simulation results of a 7-level cascade inverter, including optimal values of switching angle and voltage increment as well as the WTHD for options 1 and 2 respectively are summarized in Table 1. The corresponding values for the six-step switching technique are included for comparison. The switched line voltage of the inverter under option 2 switching is depicted in Fig.3.

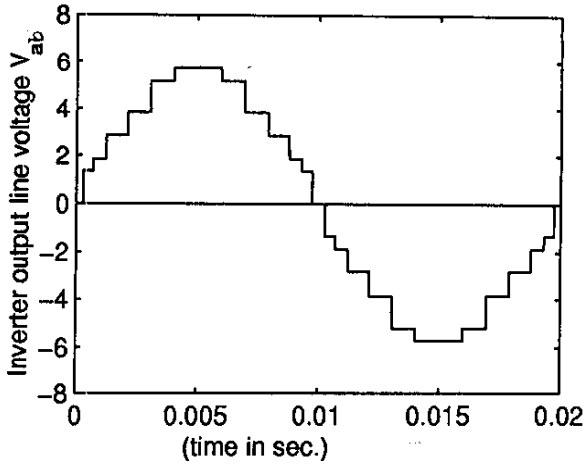

Fig.3 The switched line voltage V_{ab} of a 7-level cascade inverter

Table 1: Simulation results for a 7-level cascade inverter

	α_1 (deg)	α_2 (deg)	α_3 (deg)	Δe_1 (p.u.)	Δe_2 (p.u.)	M_{max}	WTHD (%)
Option 2	7.94	25.04	42.47	0.3327	-0.4688	0.91*	0.2515
Option 1	7.097	15.86	36.18	0	0	0.92	0.3220
Six-step	0	0	0	0	0	1	4.63

To summarize the characteristics of option 2:

1. In the cases of option 1 and six step switching, there is $E_1 = E_2 = E_3 = E_d$, i.e. the dc voltage sum is $3E_d$, based on which the M_{max} values of Table 1 are calculated. In fact the dc voltage sum of option 2 is $2.86E_d$, for $E_1=E_d$, $E_2=1.33E_d$, and $E_3 =0.53E_d$ respectively. Therefore the nominal value of E_d is increased by 1.049 in the calculation of M_{max} for option 2, as $2.86(1.049E_d)=3E_d$;

2. The limit of M_{max} of option 2 depends on that of E_i, (I = 1,2,3), or E_{d_max};

3. For the case of a 7-level structure, the WTHD is 22% reduced from that of option 1 at $M=M_{max}$

Digital simulation is also performed for a 5-level cascade inverter for comparison, and results of both options 1 and 2 are given in Table 2.

Table 2: Simulation results for a 5-level cascade inverter

	α_1 (deg)	α_2 (deg)	Δe (p.u.)	WTHD(%)
Option 2	10.97	35.24	0.734	0.5087
Option 1	5.14	30.86	0	0.8051

It can be seen in the Table 2 that if the option 2 switching strategy is implemented, the dc voltage ratio for the 5-level cascade inverter is 1:1.734, and WTHD is 40% reduced from that of option 1. Comparing with the dc voltage ratio of 1:1.33:0.53 and 20% WTHD reduction in the case of the 7-level structure, the result indicates that dc voltages and harmonic differences between options 1 and 2 decrease with the increase number of levels. It is therefore expected for levels higher than 11, i.e. a total 5 H-bridges per phase in series connection, the WTHD of option 2 would approach that of option 1. Eventually, the switched waveform of option 2 would approach that of option 1.

7. Conclusion

In this paper, the effect of different dc voltages on the WTHD performance of a multilevel cascade inverter is investigated. Results of digital simulation are presented and compared with those of pulse width optimization technique as well as the six-step switching technique. The harmonic distortion of option 2 is significantly reduced from that of option 1 for 5 and 7-level structure. For number of levels higher than 7, the harmonic and dc voltage difference between the two options become marginal.

Since the separate regulation of dc link voltage is an expensive measure, the best application of the option 2 technique is for the cascade inverter to be operated under a constant load condition. Hence, the dc link voltages can be fixed at their preset points, no on-line regulation of E_i is required, the implementation of option 2 is thus simplified

compared to option 1, while achieving a better harmonic performance than that of option 1.

With different dc voltages operated in option 2, capacitances of the dc capacitors should be designed separately to match their voltage ratings. Also different voltage rating and thermal capability of the converter switches need to be taken into account in the design of each H bridge.

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