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A Generalized Structure of Multilevel Power Converter

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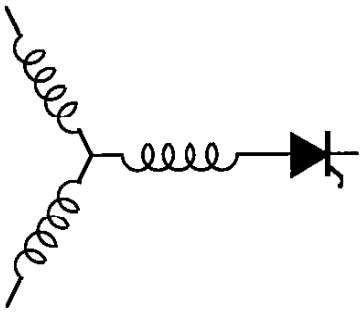

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Abstract - **Multilevel inverters are becoming popular in the past few years for high voltage and high power applications. Various topologies and modulation strategies have been investigated for utility and drive applications in the recent literature. However, most of the reported topologies for multilevel structures employ dc voltage sources of equal magnitudes. This paper is devoted to the investigation of a generalized structure of multilevel power converter where these discrete voltage sources are not necessarily equal. The topological structures, operating principles and performance characteristics resulting from this general approach are presented. Various design criteria and issues like spectral structure are discussed. A comparative evaluation of various alternatives obtained from the generalized structure is presented.**

I. INTRODUCTION

Multilevel power conversion is a rapidly growing discipline in the field of power engineering [1]. Numerous topologies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating.

Topologically, a multilevel structure can be considered as a 'large' voltage synthesizer realized from multiple 'smaller' discrete dc voltage sources. A conventional multilevel power converter topology employs multiple dc sources / link voltages of *equal* magnitudes. It can be modeled as a uniform quantizer which approximates an analog input reference voltage by discrete levels of voltages available at the dc bus. Additional improvements in the waveform quality are accomplished by using various pulse width modulation techniques [2].

The number of synthesized levels at the phase output of such an inverter is usually a linear function of the number of split dc buses used. This structure has been studied extensively in the literature with a view of sharing high dc bus voltages equally [3]. An inherent advantage in adopting this approach is that all the primary devices need to have equal voltage blocking capability. However, depending upon the ratings of the devices used, it may be possible to use unequal voltages at the dc link. Moreover, one can also use assorted devices to meet respective diverse rating requirements, thereby optimizing power conversion capability of the converter [4]. This paper demonstrates that, with an appropriate choice of these voltage sources, one can obtain a substantial increase in the number of synthesized levels thus improving output waveform quality. Furthermore, with a combination of different devices, one can employ a hybrid modulation strategy to optimize the performance in terms of switching losses etc. [4].

A multilevel power converter employing *unequal* dc voltage sources has seldom been studied in detail in literature. This paper will discuss a generalized approach towards employing dc voltage sources as basic building blocks in a multilevel structure. The conventional topologies are then special cases of this generalized approach which restrict the dc source voltages to be of equal magnitude. The primary reasons for investigating a generalized structure are:

- Increasing number of synthesized levels thereby improving waveform quality;
- Employing combination of devices so as to optimize their power processing capability;
- Adopting hybrid modulation strategies to decrease switching losses etc.

A cascaded arrangement of single phase inverters, commonly known as the "H-bridge multilevel inverter", is used as a candidate topology to demonstrate the basic concept in this paper. However, the phenomena discussed here, with suitable modifications, are also applicable to other multilevel topologies viz. diode clamped, flying capacitor etc [5].

The following section of this paper describes extension of conventional multilevel topology to

configurations with uncqual dc voltage sources. A brief design-oriented analysis and comparative evaluation of the resulting multilevel structures is presented in Section III. The conclusions include a summary of results presented in the paper.

II. Evolution Of Configurations With Unequal DC Voltage Sources

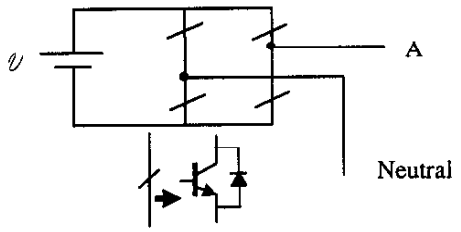

Fig. 1: A basic cell of the H-bridge multilevel inverter.

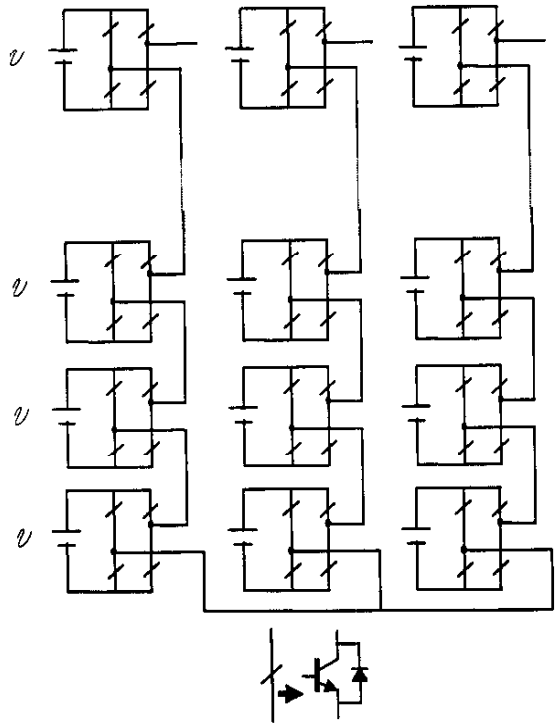

Fig. 2: Order-1 configuration for multilevel inverters.

In order to simplify the analysis let us first consider a simple single phase inverter as shown in Fig. 1 which is a basic building block of the H-bridge topology. The switches can be realized by any power devices such as Insulated Gate Bipolar Transistors (IGBT). This inverter is capable of synthesizing three distinct voltage levels ($-\mathcal{V}$, 0, $+\mathcal{V}$) at the phase output if the dc bus voltage is equal to $\mathcal{V}$. Fig. 2 presents a simplified sketch of the power circuit of an H-bridge multilevel power converter with 'n' such equal dc voltage sources of magnitude $\mathcal{V}$. This particular arrangement follows the conventional approach [6] and will be termed as *Order-1 configuration*. It is fairly easy to generalize that the number of distinct levels (N_1) at the output with 'n' such blocks with Order-1 arrangement are given by (1).

$$N_1 = 2n + 1 \qquad (1)$$

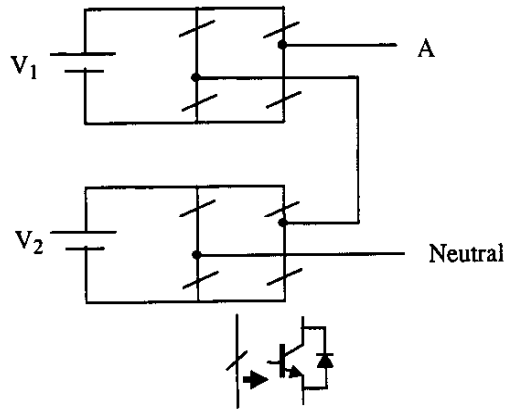

Fig. 3: H-bridge multilevel inverter with two dc voltage sources per phase.

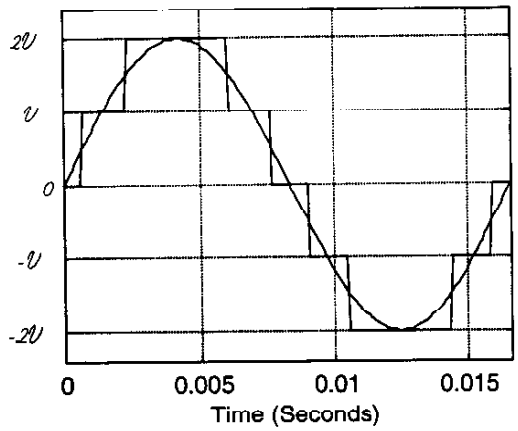

Fig. 4: Output voltage for multilevel inverter with voltage sources $V_1 = V_2 = \mathcal{V}$.

Next, consider a multilevel inverter with two dc voltage sources (V_1 and V_2) per phase. A simplified power circuit of a single leg is drawn in Fig. 3. This inverter comprises of two single phase inverters connected in series. By normal convention, both the dc source voltages are designed to be equal ($V_1 = V_2 = \mathcal{V}$). Hence, such an inverter is capable of synthesizing five

distinct voltage levels (0, $\pm V$, $\pm 2V$) at the output as shown in Fig. 4.

The performance attributes of the output waveform, in terms of levels, can be further enhanced by using unequal dc voltage levels. For instance, with a configuration of $V_1 = V$ and $V_2 = 2V$, it is possible to obtain seven levels at the output as shown in Fig. 5 [4].

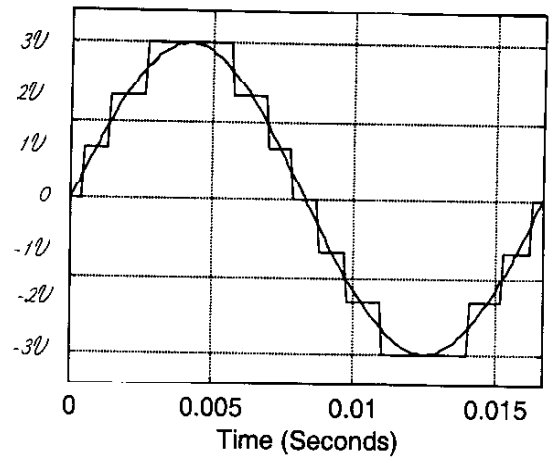

Fig. 5: Output voltage for multilevel inverter with voltage sources $V_1 = V$ and $V_2 = 2V$.

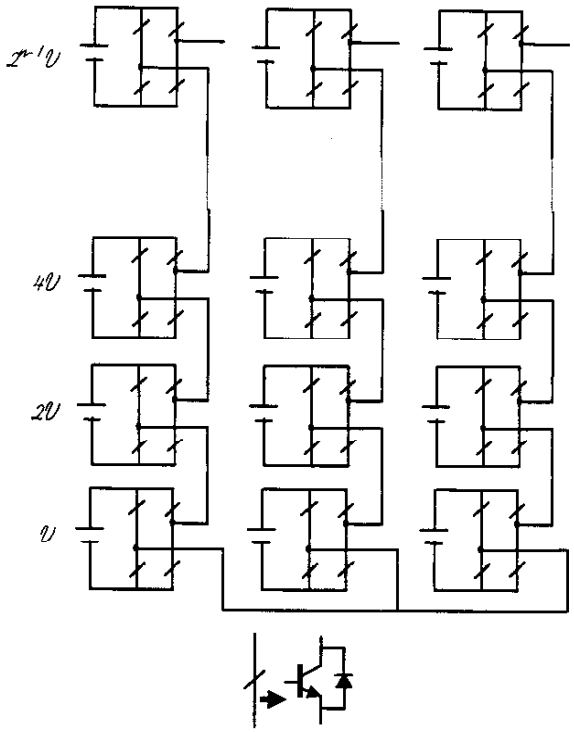

Fig. 6: Order-2 configuration for multilevel inverters.

As may be seen from Fig. 5, the *basic output levels* of this inverter are 0, $\pm 1V$ and $\pm 2V$. It is possible to synthesize $\pm 3V$ by combining $\pm 1V$ and $\pm 2V$. Hence levels $\pm 3V$ are termed as *derived output levels*. One can also generalize this concept for 'n' such cascaded inverters, with dc voltage levels varying in binary fashion as shown in Fig. 6. This arrangement of dc source voltages will be termed as *Order-2 configuration*. With simple mathematics, it can be determined that the number of distinct levels (N_2) one can achieve with this arrangement is given by (2).

$$N_2 = 2^{n+1} - 1 \qquad (2)$$

It is interesting to observe a close resemblance of this binary configuration with the process of analog and digital interconversion [4], [7]. As in a digital to analog converter, one can obtain all the combinations of voltages arranged in binary fashion here. As demonstrated earlier, it is possible to obtain 0, $\pm 1V$, $\pm 2V$ and $\pm 3V$ levels (i.e. seven levels) with only two dc sources (V and $2V$) per phase. It may be observed that the conventional H-bridge topology with identical dc sources (Order-1 configuration) would need three sources per phase to synthesize seven levels. Also, it has been reported that it is possible to construct a 'hybrid' topology which consists of a low voltage fast switching IGBT inverter and a high voltage slow switching GTO thyristor inverter based on Order-2 arrangement [4].

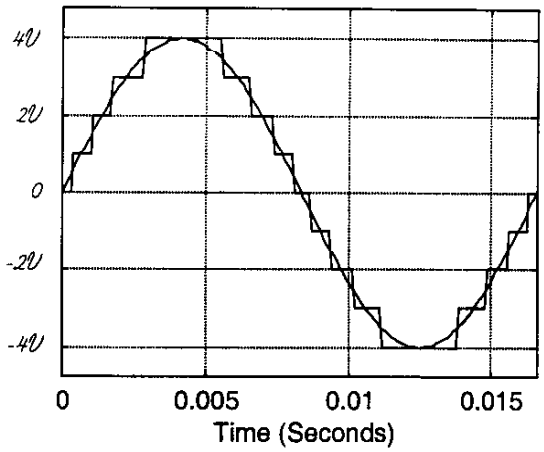

Fig. 7: Output voltage for multilevel inverter with voltage sources $V_1 = V$ and $V_2 = 3V$.

Continuing with the above seven-level illustration of Order-2 configuration, it may be noted that, it is also possible to generate an additional derived level $1V$ by subtracting $1V$ from $2V$. But this would be redundant

since, $1V$ is already a basic output level of the inverter. This leads to the possibility of employing dc source voltages with magnitudes $1V$ and $3V$. This configuration can generate nine distinct output levels (0, $\pm V$, $\pm 2V$, $\pm 3V$, $\pm 4V$) which are illustrated in Fig. 7. As may be seen from Fig. 7, one can synthesize derived levels viz. $\pm 2V$ and $\pm 4V$ with the basic levels $\pm 1V$ and $\pm 3V$. It may also be observed that there is no redundancy in the derived levels.

One can generalize the same concept for 'n' such cascaded inverters, with dc voltage levels varying in a geometric progression with a factor of 3 as shown in Fig. 8. This arrangement of dc voltage sources will be termed as *Order-3 configuration*. With simple mathematics, it is determined that the number of distinct levels (N_3) one can achieve with this arrangement is given by (3).

$$N_3 = 3^n \quad (3)$$

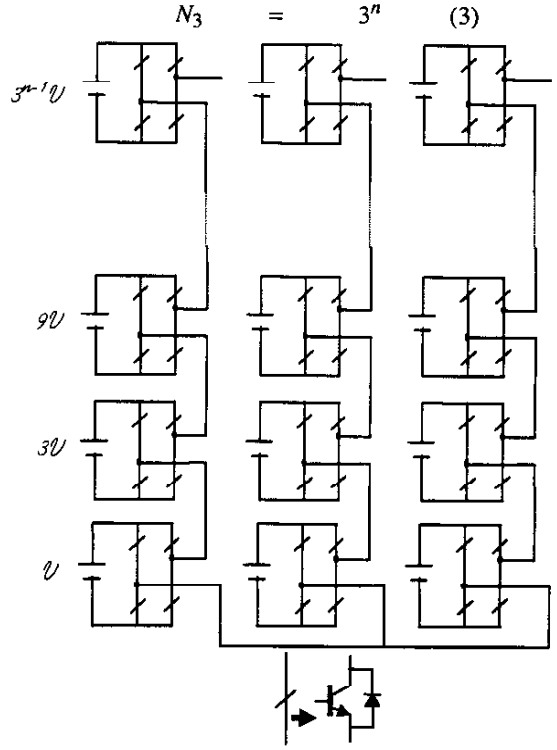

Fig. 8: Order-3 configuration for multilevel inverters.

It may be noted that one cannot extend this concept any further, eg. $1V$ and $4V$ configuration is not possible, because, one loses an intermediate level (in this example, one cannot synthesize $2V$). This deprives of adjacent level switching which penalizes the spectral performance. Moreover there is no additional advantage in the number of synthesized levels. A design-oriented analysis addressing these issues is presented in the following section.

III. Theotertical Analysis And Comparative Evaluation

A basic H-bridge cell is capable of synthesizing *three* distinct states at the output (Fig. 1 and Eqn. 1). Hence one can derive the maximum number of output levels that can be achieved in a topology with 'n' such cells is 3^n. It may be observed that it is possible to achieve 3^n number of levels using 'n' cells with *only* an Order–3 configuration (Eqn. 3). Hence it may be safely concluded that Order–3 configuration fetches the maximum number of levels in an H-bridge type multilevel inverter for a given number of dc voltage sources. Moreover it has the capability of generating all the intermediate levels thereby maintaining a uniformly predictive spectral structure at the output. It may be noted that, when compared to a conventional equal dc voltage configuration (Order–1), an Order–3 arrangement is capable of generating substantially high number of voltage levels. e.g. A conventional multilevel inverter with three equal dc voltage sources can synthesize only seven distinct voltage levels at the output. But with an Order-3 arrangement, one can obtain twenty-seven distinct levels which results in substantial improvement in spectral performance. However, it should be noted that the basic levels of an Order-3 configuration vary in the ratio 1:3:9. This implies that the voltage ratings of these three inverters are 0.07 per unit, 0.23 per unit and 0.70 per unit respectively. It may not always be feasible to distribute a high voltage with such disparity in a practical situation. This is the principal limitation in extending Order-3 approach beyond two or three dc sources per phase. However it is possible to use intermediate configurations such as 1:3:4 / 1:3:5 etc. which still produce sixteen / eighteen levels while restricting the disparity.

The analysis presented so far is relevant to the cases where stepped waveform synthesis or staircase modulation is adopted. Such control methodology is primarily used in utility applications and high power drive systems [8]. The spectral quality of the staircase waveform can be further enhanced by employing Pulse Width Modulation (PWM) techniques. It is possible to use conventional modulation strategies such as sub-harmonic modulation and space vector modulation with the above inverters to obtain further improvement in the synthesized waveform. However this approach is not particularly suitable for the multilevel configurations

with unequal dc voltage sources. An alternative modulation strategy which incorporates stepped synthesis in conjunction with variable pulse width of the consecutive steps has been proposed in [4]. The control philosophy combines a faster switching low voltage cell with a slower switching high voltage cell. Under this hybrid modulation strategy, the effective spectral structure of the output depends on the switching of low voltage cell, while the overall voltage generation capability is decided by the voltage ratings of the high voltage cell.

The hybrid modulation strategy, as presented in [4], can be extended for a general multilevel configuration with unequal dc voltage sources. The cell with the smallest dc voltage source, V, can be switched at high frequency, and its output can be combined with the baseline staircase waveform to enhance its spectral quality. Thus for example, with a configuration like $1V$, $2V$ and $5V$, one can generate derived levels $\pm 3V$ and $\pm 7V$ from basic levels $\pm 2V$ and $\pm 5V$. Now, if a switching pattern is obtained between $0 \leftrightarrow V$ and $0 \leftrightarrow -V$, one can superimpose it on the basic and derived levels to get a complete PWM waveform between all possible levels from $-8V$ to $+8V$. This is illustrated in Fig. 9.

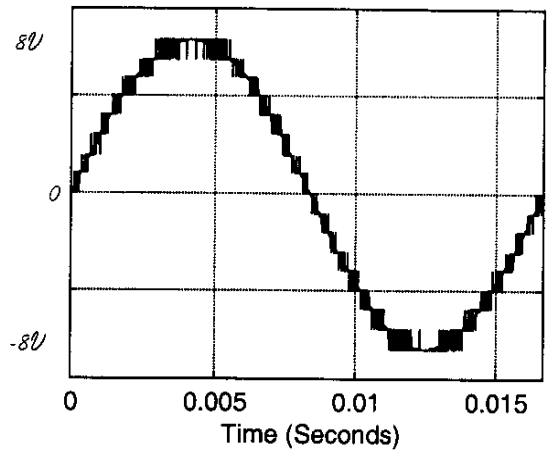

Fig. 9: Full PWM capability with $1V$-$2V$-$5V$ structure.

In order to be able to satisfy a complete PWM capability, all the dc voltage sources other than $1V$ should be able to synthesize every alternate step on the staircase waveform. This implies that the remaining voltage sources should be capable of generating all the even levels viz. $2V$, $4V$, $6V$...etc. If this condition is satisfied, then, one can combine a PWM pattern switching between $+V$, 0 and $-V$ with these levels to obtain a complete PWM waveform. It may be easily observed that the requirement of synthesizing $2V$, $4V$, $6V$ etc. can be translated to generating equivalent of twice the conventional pattern of adjacent steps; i.e. $2V = 2 \times 1V$, $4V = 2 \times 2V$, $6V = 2 \times 3V$ and so on. Hence, from our earlier discussion on the Order-3 configuration, which can generate all the consecutive steps with least number of dc voltage sources, it is fairly straightforward to guess such a configuration for a complete PWM capability to be as $1V$, 2 x ($1V$), 2 x ($3V$), 2 x ($9V$) etc. It may be noted that the numbers in bracket form an Order-3 configuration. Hence, in conclusion, a configuration which can generate maximum number of all the consecutive steps with an intermediate variation in their pulse widths, for a given number of dc voltage sources is

$$1V, 2V, 6V, \ldots 2*3^{n-2}V \qquad (4)$$

All normalized configurations of dc voltage sources, arranged in an ascending order, are completely PWM capable if each individual voltage source is smaller than or equal to the corresponding voltage in the above sequence. Order-1 and Order-2 configurations are completely PWM capable by this rule. In contrast, Order-3 configuration does not qualify to be completely PWM capable, which may be easily verified.

Table I. Comparison of different configurations of H-bridge multilevel inverters.

No. of dc voltage sources per phase (n)	Configuration $V_1 V_2 \ldots V_i \ldots V_n$	Total no. of levels $2\Sigma V_i + 1$	Measure of disparity $\frac{1}{n-1}\frac{\Sigma V_i}{V_{i-1}}$	PWM capability
1	$1V$	3	1.00	FULL
2	$1V$ $1V$	5	1.00	FULL
	$1V$ $2V$	7	2.00	FULL
	$1V$ $3V$	9	3.00	PARTIAL
3	$1V$ $1V$ $1V$	7	1.00	FULL
	$1V$ $1V$ $2V$	9	1.50	FULL
	$1V$ $1V$ $3V$	11	2.00	FULL
	$1V$ $1V$ $4V$	13	2.50	FULL
	$1V$ $1V$ $5V$	15	3.00	PARTIAL
	$1V$ $2V$ $2V$	11	1.50	FULL
	$1V$ $2V$ $3V$	13	1.75	FULL
	$1V$ $2V$ $4V$	15	2.00	FULL
	$1V$ $2V$ $5V$	17	2.25	FULL
	$1V$ $2V$ $6V$	19	2.50	FULL
	$1V$ $2V$ $7V$	21	2.75	PARTIAL
	$1V$ $3V$ $3V$	15	2.00	PARTIAL
	$1V$ $3V$ $4V$	17	2.17	PARTIAL
	$1V$ $3V$ $5V$	19	2.34	PARTIAL
	$1V$ $3V$ $6V$	21	2.50	PARTIAL
	$1V$ $3V$ $7V$	23	2.67	PARTIAL
	$1V$ $3V$ $8V$	25	2.84	PARTIAL
	$1V$ $3V$ $9V$	27	3.00	PARTIAL
4	V V V V	9	1.00	FULL
	.. ..	..	..	..

A comparative evaluation summarizing these features is presented in Table I. Entries in this table are all possible entries which qualify for adjacent step synthesis rule. This means that all the configurations in this table can generate all the intermediate consecutive steps in a multilevel waveform. It may be reiterated that, *only* the configurations presented in the table are qualified to do so. As may be observed, the number of synthesized levels increases as one approaches Order-3 configuration. However, it is accompanied by a corresponding increase in disparity among the dc voltage sources. Conventional configurations with equal dc voltage sources have no disparity (=1). The maximum disparity (=3) is attributed to Order-3 configurations. So also, no configuration with sources $>2V$ but without $2V$ features full PWM capability. A comparison between representative cases viz. $1V$-$2V$-$6V$ and $1V$-$3V$-$6V$ is illustrated in Figs. 10 and 11. It may be noted that both these configurations have equal amount of disparity (2.5) and they generate almost same number of levels (19 and 21). However, the former one is completely PWM capable while the latter one is not.

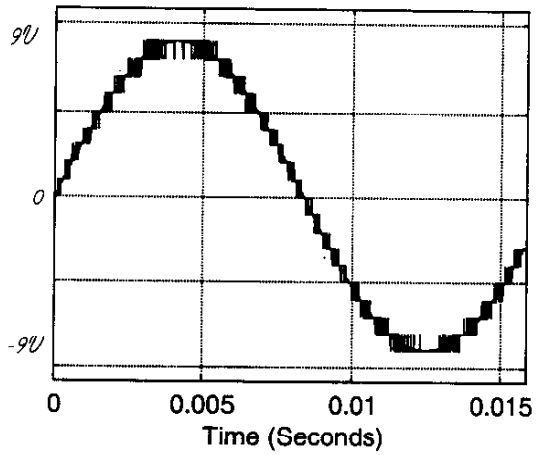

Fig. 10: Output voltage for multilevel inverter with voltage sources V, $2V$ and $6V$.

IV. Conclusions

This paper has presented a generalized approach towards synthesizing multiple levels in a multilevel inverter. Configurations particularly 'favorable' to H-bridge topology are discussed. It is shown that the conventional configurations employing equal dc voltage sources form a small subset of the generalized structure. It is possible to improve the spectral performance with an appropriate combination of voltage sources. A trade-off has been observed in terms of number of synthesized levels and factors such as disparity and PWM capability. Analytical derivations and discussion is presented to prove some general concepts. Computer simulation results presented in the paper support the theoretical claims. The concept described in this paper can be extended to other topologies such as diode-clamped or flying capacitor with certain modifications.

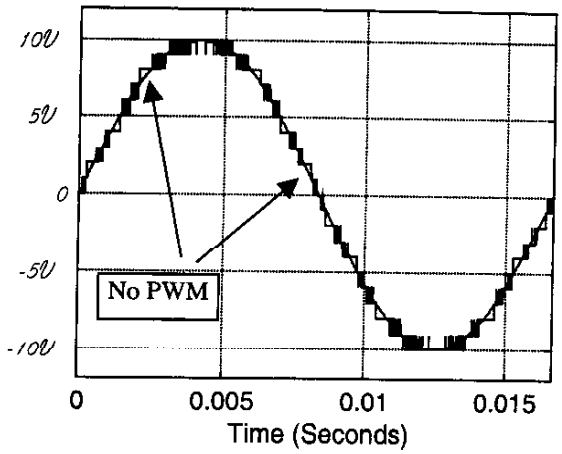

Fig. 11: Output voltage for multilevel inverter with voltage sources V, $3V$ and $6V$.

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