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Multilevel Power Conversion - An Overview of Topologies and Modulation Strategies

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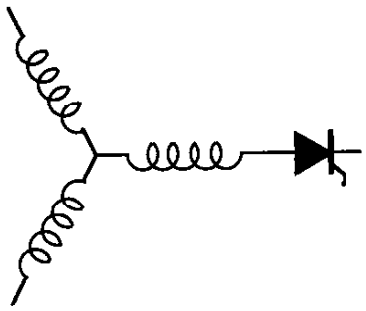

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Multilevel Power Conversion - An Overview of Topologies and Modulation Strategies

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Abstract – **Multilevel power converters represent a potential breakthrough in employing switching converters to medium voltage applications (2-13 kV). This paper summarizes the state of the art in this rapidly developing field of power electronics.**

I. INTRODUCTION

Multilevel power converters have been attracting increasing attention in recent years and have been selected as the power converter of choice in several high voltage and high power applications [1]-[4]. Numerous topologies to realize these converters have been introduced and widely studied [5]-[10]. Waveform synthesis methods for these converters include staircase modulation, sine-triangle carrier modulation, space vector modulation and other predictive methods [11]-[16]. This paper documents an overview of topologies and modulation strategies reported in literature for multilevel power conversion.

Topologically, a general structure of multilevel power converters can be considered as a 'large' voltage synthesizer realized from a number of 'smaller' discrete dc voltage sources. This technology was initially evolved from the need for reducing the harmonic content in inverter output voltage. Subsequently it has been practically implemented to serve the need for realizing inverters driven from high voltage dc bus. The state-of-the-art switching devices have been either very highly stressed or not of sufficient voltage rating to realize high voltage and high power converters. By using multilevel structures, the stress on each switching device can be proportionately reduced. Thus a high dc bus voltage level can be handled without using bulky and lossy step up / down transformers.

In principle, a multilevel inverter offers several advantages over the conventional two-level counterpart as follows:

- Synthesis of higher voltage levels using power devices of lower voltage ratings;
- Increased number of voltage levels which leads to better voltage waveforms and reduced Total Harmonic Distortion (THD) in voltage;
- Reduced switching dv/dt stresses which is advantageous for reducing existing electromagnetic interference problems.

It may also be noted that multilevel power converters have a significant distinguishing feature of redundancy regarding the voltage synthesis. Most voltage vectors in an n-level inverter have one or more constitutive switching states for a total of n^3 states with a three-phase inverter. An n-level inverter has 1 vector of (n) redundancy, 6 vectors of (n-1) redundancy, 12 vectors of (n-2) redundancy and so on. Therefore, a large number of redundant switching states offer a potential means for balancing dc capacitor voltages and minimizing switching frequency.

In general, the main issues of concern in devising a modulation strategy for multilevel inverters are as follows:

- Minimization of load current harmonics;
- Minimization of switching frequency;
- Ensuring uniform switching frequency for all switching devices;
- Ensuring dc bus capacitor voltage balancing on an average / instantaneous basis.

Conversely, the main issues in devising a modulation strategy for multilevel rectifiers are:

- Minimization of utility line harmonics;
- Maintain unity power factor operation;
- Ensuring uniform switching frequency for all switching devices;
- Ensuring dc bus capacitor voltage balancing on an instantaneous / average basis.

This paper presents an overview of the research directed towards development of multilevel power conversion technology. The following section is devoted to the classification and comparative evaluation of topological structures available to synthesize multilevel waveforms. The topologies are broadly classified in five groups depending on the basic structural differences. Representative example structures from each category are illustrated and discussed. The next section deals with a literature survey of modulation strategies developed for multilevel power converters. The modulation strategies are grouped in seven categories. A comparative evaluation of the advantages and disadvantages of most of the strategies is included. Finally, the paper concludes with a summary of the development and refinement of the multilevel power conversion technology and a discussion about its future prospects.

II. REVIEW OF TOPOLOGIES

A. Multilevel Configurations with Diode Clamps

Early interest in multilevel power conversion technology was triggered by the work of Nabae et al. in 1980 who introduced the so-called Neutral-Point-Clamped (NPC) Pulse Width Modulated (PWM) inverter topology [5]. It has been shown that the resultant three-level PWM waveform has considerably better spectral performance compared to that of a conventional PWM Voltage Source Inverter (VSI). Subsequently, the original NPC topology has been extended to higher number of levels using the similar principle of clamping the intermittent levels with diodes [8], [9]. In addition to improving the waveform quality, these multilevel inverters substantially reduce voltage stress on the devices. This stress reduction is directly proportional to the number of levels. Such multilevel structures are generically known as "Diode Clamped Multilevel Inverters".

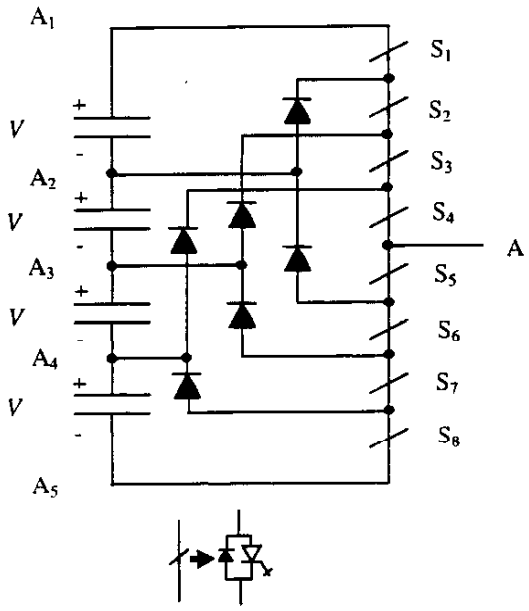


Fig. 1. Simplified schematic of one leg of a five-level diode clamped inverter.

One leg of a representative five-level diode clamped multilevel structure is shown in Fig. 1. The remaining two legs have the same switch-diode configuration and share the same dc bus points. From Fig. 1, it may be observed that a five-level waveform can be synthesized at output point A by tapping five points (A_1, A_2, A_3, A_4, A_5) on the quadruple dc bus of magnitude '$4V$'. The circuit can be thought of as a multiplexer, attaching output to one of the five available voltage levels. All the capacitors are identical and the dc voltage levels are 'V' each. Hence, a peak output voltage of $\pm$ $2V$ (with reference to A_3) can be realized by clamping the phase output to the top (A_1) or bottom (A_5) of the dc bus. These are achieved by closing a set of four switches viz. S_1-S_4 or S_5-S_8. The inner voltage levels $+V$, 0 and $-V$ can be synthesized by closing switches S_2-S_5 or S_3-S_6 or S_4-S_7, respectively. This creates a current path connecting two of the clamp diodes back-to-back. The other end of these back-to-back clamp diodes is connected to one of the voltage taps (A_2, A_3, A_4) along the dc bus. These diodes also prevent an undesired voltage level from being connected to the output and create a bi-directional current path for an inductive load.

A combination of PWM rectifier and inverter based on these diode clamped structures is also possible and proven to be a promising solution for high power ac drive applications [17], [18].

It may be noted that only the topologies with odd number of levels (1,3,5...) offer a neutral point access. It is not possible to obtain a neutral clamp in a structure with an even number of levels (4,6,8...). This may prove to be a handicap in utility applications and in realizing a single leg operation. Nevertheless, such structures with even number of levels appear to be a potential candidate for drive applications [19]-[21].

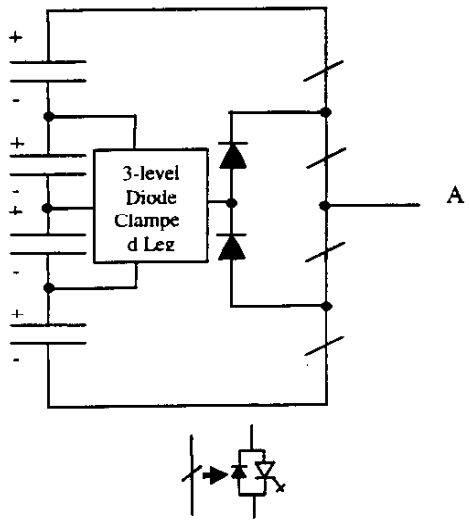


Fig. 2. Simplified schematic of one leg of a cascaded diode clamped multilevel inverter.

There exists an inherent problem of unbalanced capacitor voltage due to their series-connected nature. This demands a special attention and treatment to employ this approach in practical situations. Another disadvantage of this topology is that the required voltage blocking capability of the clamp diodes is proportional to the level for which they are used to employ clamping action. Hence, numerous series connected clamp diodes are needed at higher levels which is a typical scenario in utility applications. The original three-level power converter circuit proposed in [5] does not suffer from this problem because it can offer relatively easier solution for

capacitor voltage balancing. By this reason, the application spectrum for this particular topology has been increasingly growing. It may be noted that successful industrial implementation of the three-level inverters for high voltage and high power ac drive systems (several hundred kW ~ several MW) has been reported in [17], [22]-[26].

One more interesting configuration with cascaded diode clamped inverters has been investigated in [27]. The authors have added a three-level auxiliary diode clamped structure at the neutral point clamping node of the main three-level inverter (Fig. 2). This modification is reported to have enhanced the spectral performance of the original topology.

B. Multilevel Configurations with Bi-directional Switch Interconnections

An improvement in the spectral structure of output waveforms using multiple levels reported in [5] was reiterated in 1983 [6]. However the structure presented in the paper is topologically different as shown in Fig. 3. An access to the neutral point is obtained through a bi-directional switch. This bi-directional switch is synthesized using a back-to-back connection of thyristors. It may be noted that the required voltage blocking capability of the 'outer' devices is higher than that of the 'inner' devices. Therefore, this topology does not offer an advantage of reduced voltage stress. The application spectrum of this approach is restricted to low power applications where harmonic spectrum is the only concern.

In the early days of semiconductor development, thyristors were the only reliable available devices to realize high power switches, and considerable effort was spent towards the development of a commutation scheme for these devices. With the advent of high power Gate Turn–Off (GTO) devices, it is now possible to realize the same structure with modern high power devices such as Insulated Gate Bipolar Transistors (IGBTs). A three-level structure based on this configuration has been reported in [28]. However, the authors use the neutral point clamping only during the switching interval in order to reduce switching stress on the devices. Therefore they have named it as a "Quasi Three-Level Inverter".

Addition of resonant elements to the original topology of [6] leads to the development of soft-switching multilevel inverters. A three-level Auxiliary Resonant Commutated Pole (ARCP) version for multilevel inverters has been investigated in [29] whereas extensions of the Resonant DC Link (RDCL) are also possible. A realization of a three-level inverter drive using a single conventional VSI, a split dc bus and two bi-directional switches has been presented in [30]. An alternative rectifier topology using a transformer-coupled auxiliary circuit and a conventional six-pulse diode bridge rectifier has been discussed in [31]. Auxiliary soft-commutated three-level inverters have also been investigated in [32], [33].

A three-level rectifier topology, which uses fewer devices to realize bi-directional switches, has been reported in [34]. A similar approach, which replaces each bi-directional switch by a single device inside a diode bridge has been investigated and named the "Vienna Rectifier" topology [35].

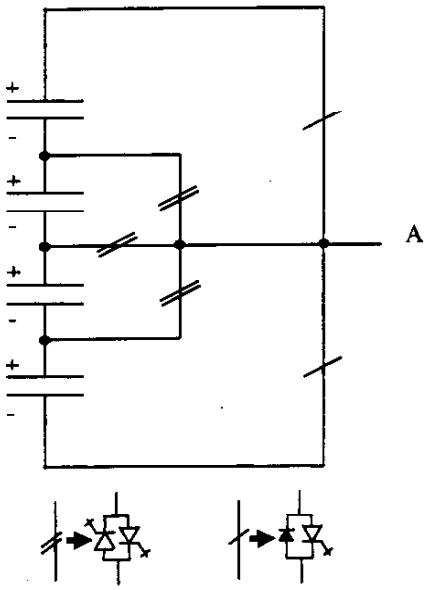


Fig. 3. Simplified schematic of one leg of a five-level bi-directional switch interconnected inverter.

C. Multilevel Configurations with Dedicated Capacitor Banks

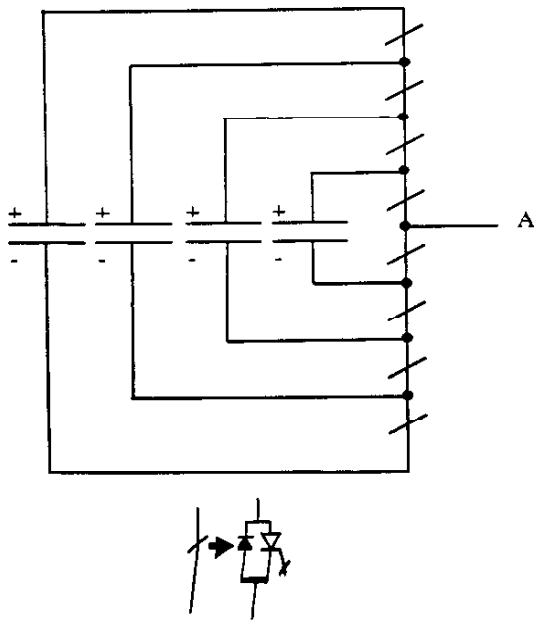


Fig. 4. Simplified schematic of one leg of a five-level flying capacitor inverter.

One of the disadvantages in using a diode clamped inverter is that the required voltage blocking capability of the

clamping diodes varies with the levels. This may result in the requirement of multiple diodes at the higher voltage levels. An alternative multilevel structure where the voltage across an open switch is constrained by clamping capacitors instead of clamping diodes has been proposed in 1992 [10]. A representative five-level structure is shown in Fig. 4. These inverters are commonly known as "Flying Capacitor Multilevel Inverters". Another advantage of this topology is that there is no unbalanced capacitor voltage problem because of independent voltage source structure. A problem associated with this approach is the requirement of complicated control strategy to regulate floating capacitor voltages. Also one needs more number of capacitor banks with increasing number of levels.

A hybrid approach which combines the advantages of diode clamped and flying capacitor topologies has been investigated in [36]. A simplified schematic of one leg is shown in Fig. 5.

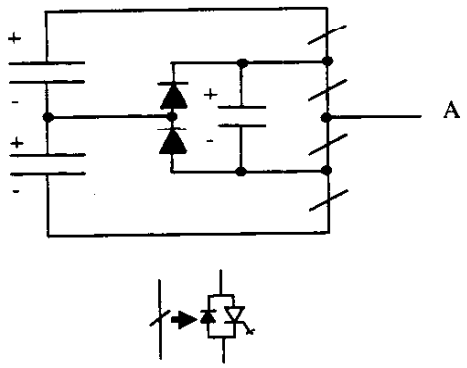


Fig. 5. Simplified schematic of one leg of a three-level hybrid diode clamped / flying capacitor inverter.

D. Multilevel Configurations with Multiple Three-Phase Inverters

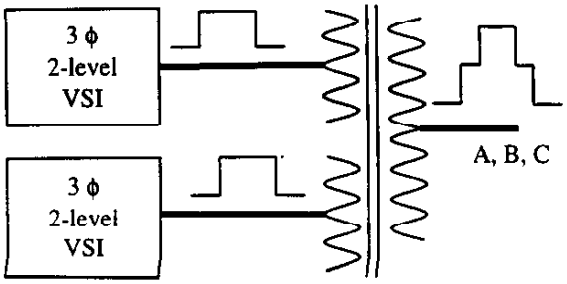


Fig. 6. Simplified block schematic of a five-level transformer coupled inverter.

Multiple low power three-phase inverters have been used in utility applications through multipulse converter configurations [37]. These converters achieve multilevel voltage output through phase shifting of multiple two-level waveforms which are added together vectorially using series-connected transformer windings (Fig. 6).

However, when the number of levels increases beyond three or five this approach becomes difficult to realize due to the requirement of increased number of multiple transformer windings. An alternative approach of combining three three-phase inverters to obtain a multilevel output has been discussed in [38]. The phase shifting is realized by using interconnecting reactances as shown in Fig. 7. In addition to the requirement of interconnecting reactances, this approach suffers from complicated control strategy. Moreover, this topology requires eighteen primary power devices but the reported line-line voltage output exhibits only five distinct levels. This is similar to the line-line output of a conventional three-level inverter which also has five distinct levels but employs only twelve primary power devices.

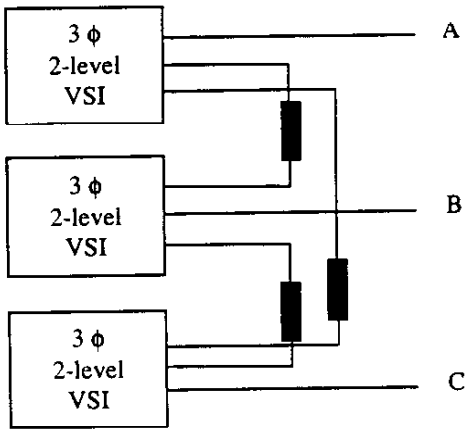


Fig. 7. Simplified block schematic of a multilevel inverter realized with three three-phase inverters and interconnecting reactances.

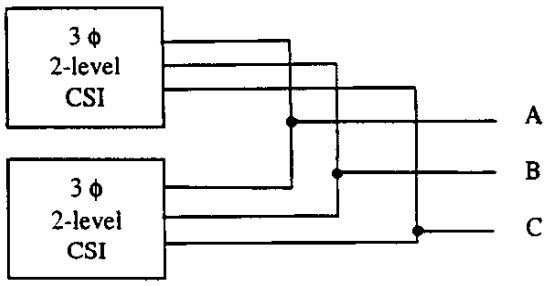


Fig. 8. Simplified block schematic of a five-level current source inverter.

It should be noted that it is not possible practically to combine multiple conventional three-phase VSIs without adding any extra interconnecting reactance / transformer

which are usually bulky and lossy. It is possible to do so with a Current Source Inverter (CSI) version. [39] has demonstrated that it is feasible to realize multilevel current waveforms by connecting together multiple three-phase CSIs (Fig. 8).

E. Multilevel Configurations with Cascaded Single Phase H-Bridge Inverters

Series connection of single phase H-bridge inverters with multiple dedicated dc buses to realize multilevel waveforms was probably first introduced in 1988 for plasma stabilization [7]. This modular approach has been subsequently extended for three-phase applications. [40]-[43] have presented topologies based on this approach for reactive power compensation and drive applications. In this approach, a number of full bridge single phase inverters with dedicated isolated dc bus capacitors / voltage sources is connected together in series to form a high voltage inverter for each phase of the system.

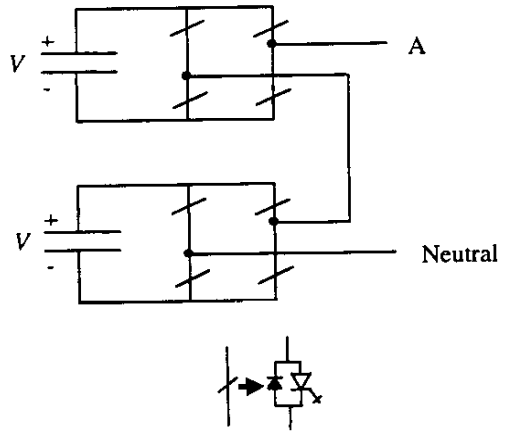


Fig. 9. Simplified schematic of one leg of a five-level H-bridge inverter.

Fig. 9 shows two such single phase H-bridge inverters connected in series to form one leg of the multilevel inverter. The remaining two phases have the same switch configuration and respective independent dc voltage sources. It may be observed that this inverter is capable of synthesizing five distinct voltage levels ($\pm 2V$, $\pm V$, 0) if all the dc bus voltages are equal to 'V'. Therefore the output voltage waveform resembles that to a five-level diode clamped inverter.

A primary advantage of this topology is that it provides flexibility for expansion of the number of levels easily without introducing undue complexity in the power circuit. Also extra clamping elements are not needed as in the former cases while requiring the same number of primary switches as in a diode clamped topology to achieve a given number of (odd) voltage levels. However this configuration requires multiple dedicated dc buses which makes it an expensive solution. On the other hand, since the dc voltage sources are independent, the problem of capacitor voltage balancing is eliminated. It may be noted that it is difficult to synthesize a rectifier-inverter combination based on this approach owing to modulation problems. Therefore the application spectrum of this topology is somewhat limited [2]. These circuits are more useful for utility applications like Static VAr Compensators (SVC) and active filters rather than high power ac drives.

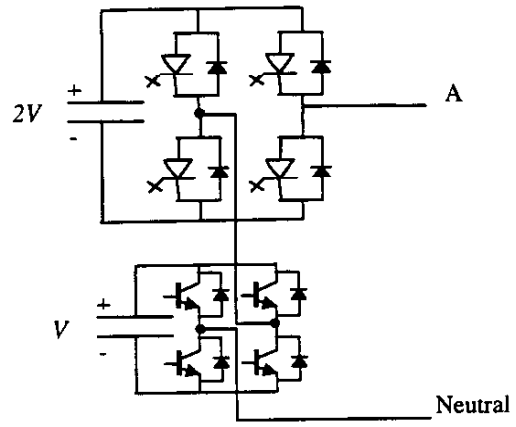


Fig. 10. Simplified schematic of one leg of a hybrid seven-level H-bridge inverter.

Conventional H-bridge topology having 'n' identical dc voltage sources per phase can offer $(2n + 1)$ distinct voltage levels at the phase output. It has been shown in [43] that the performance attributes of the output waveform in terms of number of levels can be further enhanced by using unequal dc voltage levels. The authors report that it is possible to achieve $(2^{n+1} - 1)$ distinct voltage levels with dc voltage levels varying in binary fashion (V, $2V$, $4V \ldots 2^{n-1}V$). A possible example of a topology based on this approach and employing two different types of devices, viz. IGBTs and GTO thyristors, is illustrated in Fig. 10.

A similar independent investigation has been reported in [44]. Here, the authors have also presented a hybrid version of four-level diode clamped configuration.

III. Review of Modulation Strategeies

A. Staircase Modulation Methods

Modulation strategies in multilevel inverters for utility system applications have been primarily restricted to synthesis of stepped waveforms [2]. Typical reference and output waveforms are illustrated in Fig. 11. This strategy can be interpreted as a quantization process in which an analog reference voltage is approximated by discrete levels of voltage available at the dc bus. This type of modulation does not demand high switching capability from the power devices and hence can be easily realized using GTO thyristors. The basic advantages of this strategy are its simplicity for hardware realization and minimization of switching frequency. However

it is fairly easy to note that the spectral performance is not good and a variable dc bus voltage is required to obtain variable voltage at the output. Hence, this type of strategy is primarily used in power distribution applications.

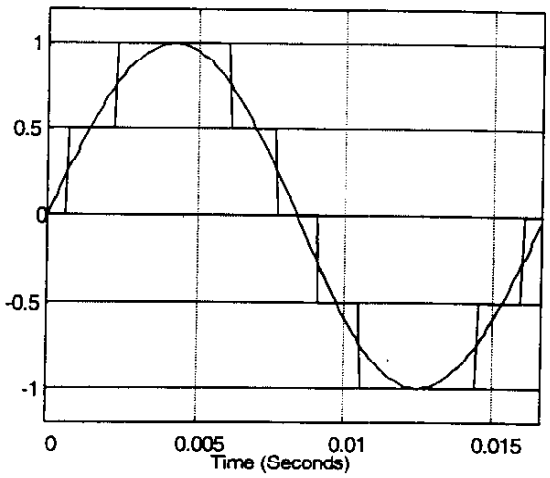


Fig 11. Typical output waveform of a stepped synthesis multilevel modulation for a sinusoidal reference.

In most utility applications and high power drive systems, it is desirable to keep the device switching as low as possible in order to minimize switching losses. For improved dc bus and device utilization, it is desirable to operate the inverter in the over-modulation region where the inverter is saturated. The m^{th} harmonic components of an n-level waveform for odd and even n are given by equations (1) and (2), respectively:

$$V_{m,n}^{rms}=\frac{2\sqrt{2}V_{dc}}{m(n-1)\pi}\sum_{k=1}^{\frac{N-1}{2}}\cos(m\alpha_k)\ ;\ m \text{ is odd} \qquad (1)$$

$$V_{m,n}^{rms}=\frac{2\sqrt{2}V_{dc}}{m(n-1)\pi}\left\{\frac{1}{2}+\sum_{k=1}^{\frac{N-1}{2}}\cos(m\alpha_k)\right\}\ ;\ m \text{ is odd} \qquad (2)$$

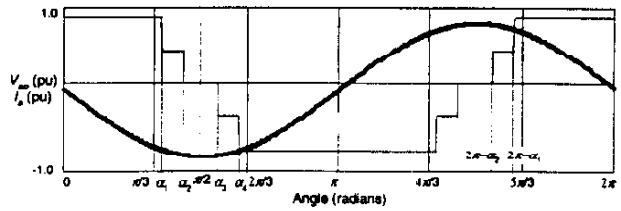


Fig. 12. Voltage (thin trace) and current (thick trace) waveforms of a five-level inverter.

The angles α_k are a function of the modulation depth and the number of levels and thus determine the harmonic content of the voltage waveform. At lower modulation depths, the switching angles are pre-calculated and stored in a look-up table. Fig. 12 shows the pole voltage and phase current waveform from a five-level inverter when the modulation depth is $1.0 < m_a < 1.33$ (where $m_a = v_{phpk}/v_{dc}/2$).

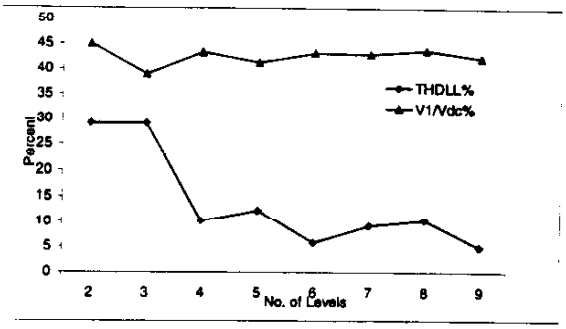


Fig. 13. Bus utilization and line voltage THD in a saturated multilevel inverter.

Fig. 13 shows the variation in bus utilization and line voltage THD with the number of levels. It is evident that diminishing returns quickly set in for greater than five levels. It has been further shown [2] that for an odd number of levels, independent control of the capacitor voltages can be accomplished by perturbing the angles α_k in a manner proportional to the capacitor voltage deviations. With even number of levels, control over the charge flowing through the center capacitor cannot be ensured for higher modulation depths [21]. Thus for SVC applications, low frequency switching schemes are not preferred at least when the diode clamped inverter topology is to be used. The essential features of the control scheme of any multilevel inverter-based static condenser can be represented as shown in Fig. 14.

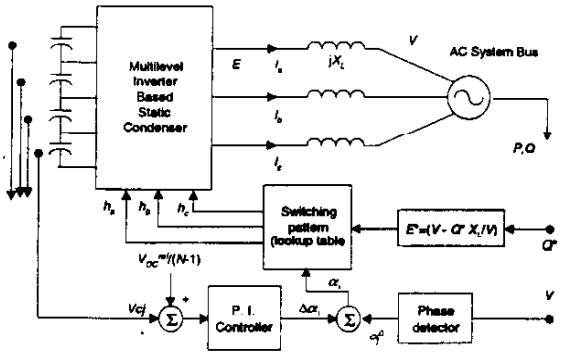


Fig. 14. Control scheme for multilevel inverter based static condenser system.

B. Harmonic Elimination Methods

Harmonic elimination methods for multilevel inverters can be designed based on similar strategies for conventional

VSIs. In these methods, notches are created on the stepped waveform at pre-calculated angles to eliminate specific harmonics. So they are also referred to as "Optimal" or "Pre-calculated" PWM methods. These calculations are usually done off-line and then the stored results are reproduced on-line by the modulator. Hence the working range of such a pre-calculation method is limited by the computing time and storage capabilities. In [45], a programmed PWM method for the selective elimination of lower order harmonics in the output voltage of NPC inverter has been discussed. Alternatively, optimization of the loss factor according to machine harmonic losses has mainly been investigated in [46].

C. Sub-harmonic Pulse Width Modulation (SPWM) Methods

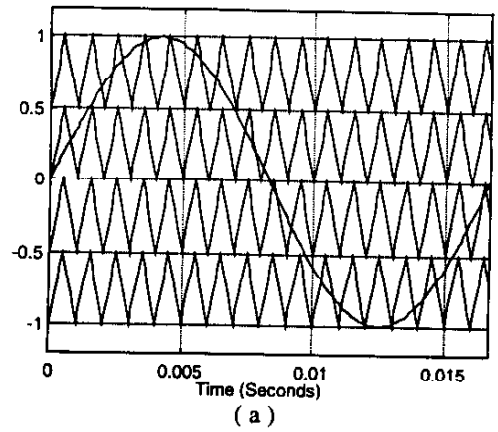
Sub-harmonic PWM (which is also commonly referred to as "Sinusoidal PWM") techniques are one of the most popular modulation methods in industrial applications and have been reviewed extensively. This method involves a comparison of the reference input, which basically is a sinusoidal waveform, against a triangular carrier waveform and detection of cross-over instances to determine switching events.

A good survey of carrier-based SPWM strategies is given in [47] for both, two and three-level inverters. These methods can be broadly classified into two categories based on the relative disposition of carrier and reference waveforms as follows :

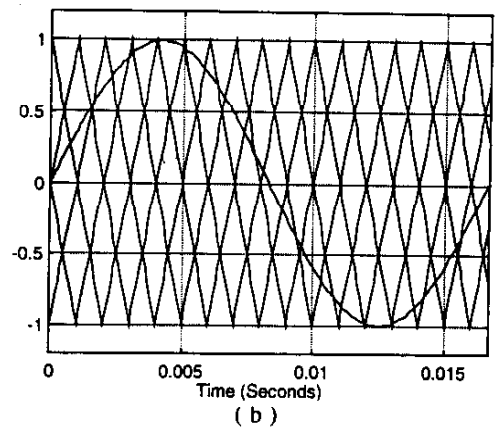
1) *Modulation strategies based on modified carrier waveforms:*

This class of modulation strategy is based on modification of carrier waveforms in order to synthesize sinusoidal outputs with better harmonic spectrum.

a) Carrier polarity variation method: [48] has presented a comparative evaluation of three possible dispositions of triangular carrier waveforms based on their relative polarities. Fig. 15(a), Type A, shows carriers with the same polarity. On the other hand, Fig. 15(b), Type B, illustrates the case where alternate carriers are flipped. In Fig. 15(c), Type C, all the carriers above zero level have same relative polarity but are in opposition with those below the zero level. Theoretical analysis is performed for three and five-level applications. Type B and C have a similar harmonic spectral characteristics. In these cases, no hamonics exist at the carrier frequency but odd-order harmonics exist in each side-band. For Type A, a harmonic exists at the carrier frequency and at odd-multiples of it and at even-numbered side-bands centered around odd harmonics of the carrier and at odd-numbered side-bands around non-existent even harmonics of the carrier. When the frequency ratio between the carrier and reference is high, there is no substantial difference in the spectral performance among these three methods.



(a)



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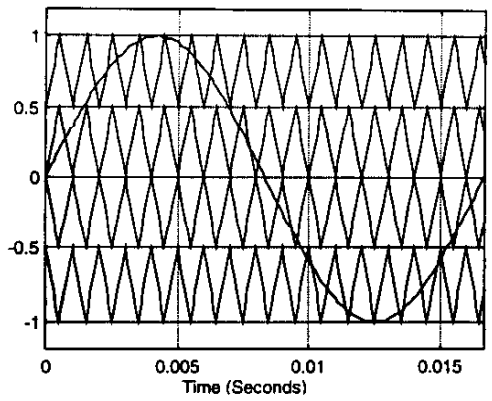

(c)

Fig. 15. Polarity variation of carrier waveforms for five-level inverters.(a) Type A. (b) Type B. (c) Type C.

b) Carrier phase variation method: A method involving phase shifting of the carrier waveform has been investigated in [49] for diode clamped and flying capacitor type three-level inverters. The basic method employs a trian-

gular carrier wave which is lagged / led by $\pi/2$ relative to the reference as shown in Fig. 16. The phase of the carrier is reversed every half cycle to preserve the quarter wave symmetry. In this case, the boundary between low and high modulation region falls at the modulation depth of around 57% as against 50% in the usual case.

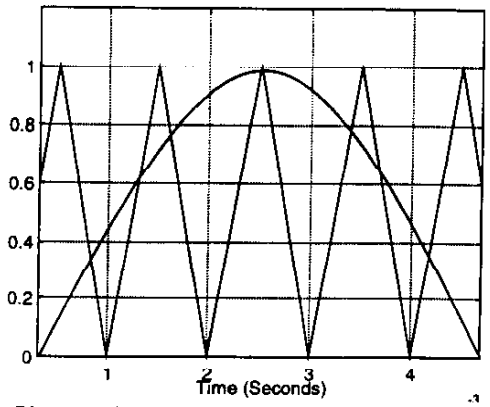

Fig. 16. Phase variation of carrier waveforms (only half cycle is illustrated).

2) Modulation strategies based on multiple reference waveforms:

This class of modulation strategy is based on employing multiple reference waveforms. It is also referred to as "Dipolar Modulation" [11]. The method uses a single triangular carrier wave and two sinusoidal reference waves to modulate three-level inverters as shown in Fig. 17. The two sinusoidal modulating waves are essentially obtained by adding positive and negative offsets to the conventional reference signal. These offsets may be uniform [11] or variable [50] in magnitude. The aim of this offsetting is to break each commutation between the outermost levels by forcing a passage of the PWM waveform through the intermediate voltage level. A primary advantage of this modulation strategy is that it does not encounter any minimum pulse width problem at lower modulation depths, which is normally a critical design issue in most of the basic modulation methods for multilevel inverters. From [47], we can also observe that this modulation scheme offers better performance than some other sub-harmonic PWM methods in terms of harmonic content at low (upto 40%) modulation depths.

One more interesting SPWM strategy based on uniform switching frequency over entire operating region has been reported in [51] for three-level inverters. The author does not adopt the synchronous modulation scheme usually employed to eliminate the sub-harmonics in SPWM. Along with the minimal torque ripple, this method is reported to be capable of maintaining the mean value of neutral point fluctuation voltage to almost zero in steady state. However, to maintain the balance under dynamic conditions with this method, one has to resort to non-adjacent state switching which puts unnecessary stress on the power devices and causes extra harmonics.

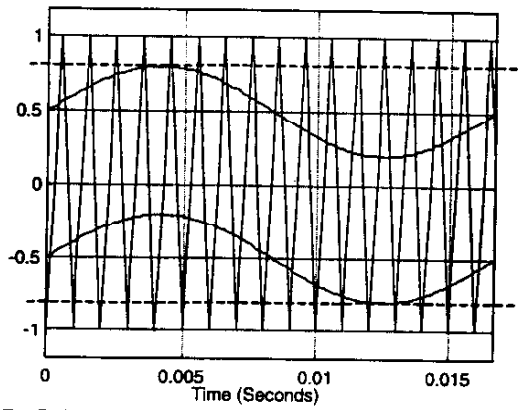

Fig. 17. Split reference and carrier waveforms for dipolar modulation.

D. Space Vector Modulation (SVM) Methods

Space vector based modulators which are widely used in control of conventional VSIs have been applied to multilevel power converters in [16], [52], [53]. The concept of space voltage vectors corresponding to various switching states has been applied to analyze the behavior of different states of a multilevel inverter and their impact on the capacitor voltage balancing. A typical space voltage vector representation of a three-level inverter is shown in Fig. 18. The instantaneous value of reference voltage vector is located in this vector space. Numbers 200-220 etc. in Fig. 18 refer to switching state of power converter and follow the notation as prescribed in [54].

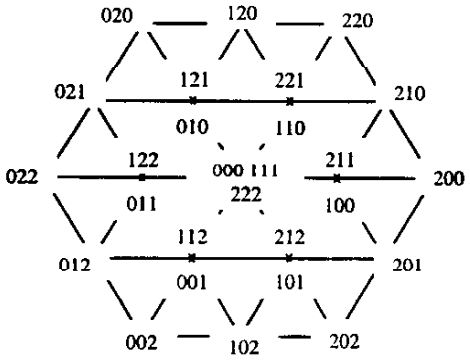

Fig. 18. Space vector representation of a three-level inverter.

One can realize any particular value on an average basis by using nearest three vectors which is the basic method to

obtain minimum harmonics and to maintain capacitor voltage balancing [16]. However, in reality, this does not guarantee balancing of capacitor voltages because of the non-ideal switching characteristics of power devices and so on. Hence it demands special measures to ensure capacitor voltage balancing [55] or employing a closed loop voltage control [52]. An alternative space vector approach can also be employed by constructing lookup tables based on the polarity of capacitor charging currents produced for all possible polarity values of the load current.

A prime issue in devising modulation schemes for multilevel inverters is to minimize harmonic content at the inverter output voltage while simultaneously maintaining instantaneous capacitor voltage balance. [56] has reported a tight control of capacitor voltage by removing specific third harmonic contributing states. Although this approach serves to maintain capacitor voltage balance, one has to handle extra switching stress on the devices and increased harmonic content. To overcome some of these reported problems, [55] has presented a strategy which ensures adjacent state switching, high spectral performance, low switching stress and capacitor voltage balancing on an instantaneous basis.

Current regulation for three-level inverters parallels the conventional case [57]. Referring to Fig. 19, for the shown orientations of the motor terminal voltage, $\bar{V}_{qds}$, the current error vector deviation $\Delta\bar{I}_{qds}$ and the current vector $\bar{I}_{qds}$, it can be seen that vectors $v(1)$, $v(7)$ or $v(8)$ form the nearest three vectors of the terminal voltage. Either $v(1)$ or $v(8)$ can be used to regulate the current, but $v(8)$ has no redundant states and is not used for regulating the current. In addition, $v(1)$ can be realized by switching states *(211)* or *(100)*. However, since $i_a > 0$, $i_b < 0$ and $i_c < 0$, state *(211)* produces a neutral current $i_n = -i_a < 0$ and state *(100)* produces a $i_n = i_a > 0$. Hence if the neutral voltage deviation $\Delta V_n > 0$, state *(211)* needs to be chosen, if $\Delta v_n < 0$, state *(100)* can be chosen. This method, when applied consistently, has been shown to work well for nearly all load conditions [54].

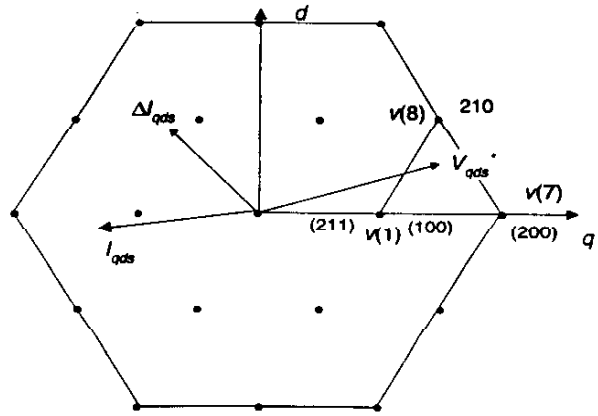

Fig. 19. Space vector modulation in a three-level inverter.

A typical design issue in employing SVM would be to ensure minimum pulse width for all selected states at any given time; taking into account the finite switching time needed by high power switching devices. Whenever the reference vector is close to a vertex / side of any triangle in the space vector region, the time allotted for the states corresponding to the remaining two / one vertices becomes small and can be smaller than the minimum allowable pulse width. [58]-[60] have attempted to solve this problem for very high power GTO three-level inverters. The narrow pulse width problem for such inverters is overcome by modifying the Nearest Three-Vector (NTV) approach to a Nearest Four-Vector approach (NFV) [59]. Although it seemingly solves the minimum pulse width problem, the penalty is imposed in switching stress and harmonics. [58] and [60] propose switching sequences based on NTV selection which ensure minimum pulse width for each state. The problem is treated in more detail in [60] than in [58], however, the switching sequence of [58] is better than [60] in terms of spectral performance.

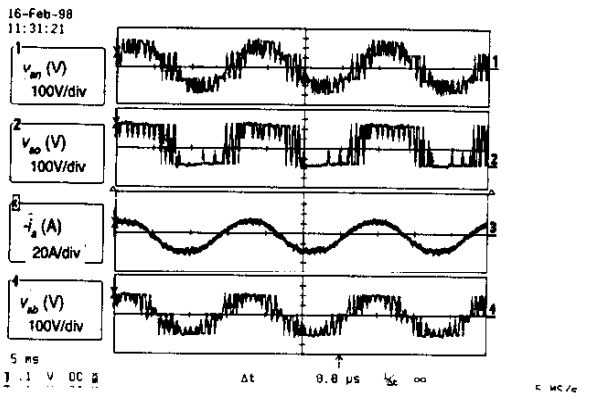

Fig. 20. Experimental SVM waveforms for a four-level inverter.

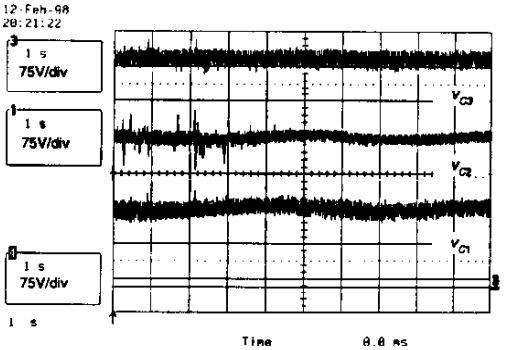

Fig. 21. Experimental four-level dc bus voltage waveforms.

Space vector PWM method, though very powerful in reducing current harmonics becomes computationally intensive as the number of levels increases. Fig. 20 shows the measured phase voltage, phase neutral voltage, line current and the line-

line voltage waveforms for a four-level inverter operating with a SVM scheme. Also, balanced dc bus voltages can be seen in Fig. 21 for the same inverter [61].

One more interesting strategy has been proposed [62] which is called "Fish Method" which deals with a graphical signature representing the integrated voltage vector in revolving co-ordinates.

E. Sigma Delta Modulation (SDM) Methods

The technique of SDM has been employed successfully as a tool to synthesize voltage waveforms in discrete pulse modulated systems [63], [64] such as the resonant link inverter. This SDM concept has been extended to synthesize multilevel waveforms [3]. This is achieved by replacing a binary quantizer in the forward path by a multilevel quantizer. It has been reported that the ratio between the quantizer gain and sampling frequency is near unity to ensure adjacent state switching and obtain best spectral performance. The multilevel SDM also operates to equalize integrals of the command and the output waveforms. A simulated five-level phase voltage output waveform is shown in Fig. 22.

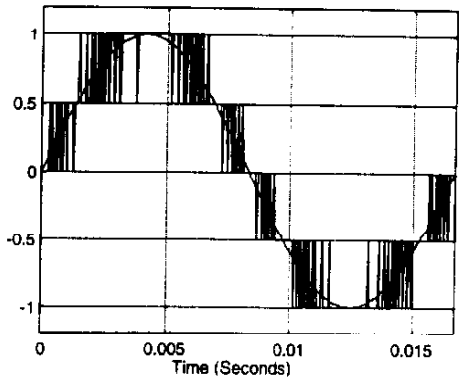

Fig. 22. Typical normalized output waveforms obtained by five-level sigma delta modulator.

F. Hybrid Modulation Methods

A modulation method that has been developed with a purpose of performing a certain task is often inhibited by some other disadvantage. There have been reported approaches which combine two or more methods in order to extract an optimized performance. [46] has reported a combination of dipolar modulation (symmetric and asymmetric) and precalculated harmonic elimination method to be employed at different modulation depths and frequency ratios. [65] gives an account of a modulation scheme which combines together dipolar modulation, unipolar modulation and one pulse modulation strategies. The authors have added partial dipolar modulation and overmodulation strategies to achieve smooth transition between the three fundamental modes. A hybrid modulation strategy composed of SVM with non-nearest state selection (for low modulation depths) and precalculated harmonic elimination (for medium and high modulation depths) has been investigated in [66] for GTO three-level inverters.

A hybrid modulation strategy has been presented in [43], [44] to control a hybrid multilevel inverter which is reported earlier in the topology review section. This hybrid multilevel inverter can be composed of a low voltage fast switching IGBT inverter and high voltage slow switching GTO thyristor inverter. Under the hybrid modulation strategy, the GTO inverter is modulated to switch only at fundamental frequency of the inverter output while the IGBT inverter is used to switch at a higher frequency. The effective spectral response of the output depends on the IGBT switching, while the overall voltage generation is decided by the voltage ratings of the GTO thyristors. A simulated phase voltage output is shown in Fig. 23. It may be seen that although the GTO inverter switching is stepped (Fig. 24), the overall waveform quality is mainly decided by the intermediate IGBT inverter switching (Fig. 25). The GTO inverter participates in synthesizing the required high voltage level (±3 kV) while the IGBT inverter (±1.5 kV) acts as a harmonic compensator.

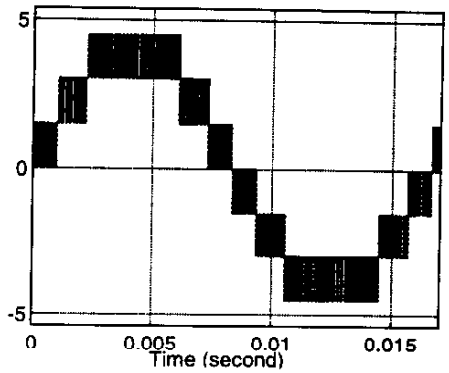

Fig. 23. Typical phase voltage waveform synthesized by the seven-level hybrid inverter topology.

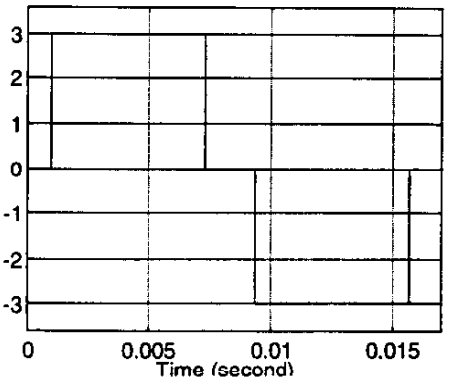

Fig. 24. Voltage waveform of a GTO inverter for the hybrid topology.

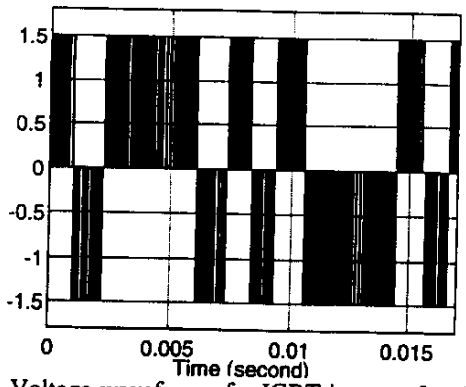

Fig. 25. Voltage waveform of a IGBT inverter for the hybrid topology.

G. Rectifier Modulation Methods

With growing regulations imposed by the utility industry, there has been a considerable amount of research towards developing a multilevel rectifier-inverter system. The issues in rectifier modulation are ensuring unity power factor and maintaining capacitor voltage balancing at any given time.

As mentioned in the review of topologies, bi-directional switch controlled three-level rectifiers have been reported in [34], [35], [67], [68]. For these active multilevel rectifiers, SVM techniques have been employed which concurrently regulate input currents and control the neutral voltage drift in three-level rectifiers. [55] also reports a space vector based method to ensure a instantaneous capacitor voltage balancing and unity power factor control in a NPC three-level system.

Similar results have been reported for an active four-level rectifier using a variant of the hysteresis current control scheme [69]. The authors have extended the ordinary hysteresis controller to a double band hysteresis controller. The inner band represents the current controller while the outer band represents the capacitor voltage balancing. The authors demonstrate theoretically that one is able to achieve unity power factor and instantaneous capacitor voltage balancing simultaneously in a four-level system. It may be noted that the penalty imposed is in loosing the advantage of adjacent state switching.

[18] has reported a feasible strategy for a GTO three-level rectifier. This strategy is complementary to their inverter modulation strategy [58] which was discussed earlier. [70]-[72] also report alternative modulation schemes for three-level rectifiers. [70] describes an implementation of selective harmonic elimination method in order to remove the lower order harmonics for a GTO rectifier. This scheme is based on synchronous PWM using tabulated pulse patterns. A model of a three-level rectifier is built and state equations are obtained in [71]. These are then used to implement a parameter insensitive linear quadratic integral regulator which is suitable for multi-input multi-output systems. The neutral point current is treated as one of the inputs along with the feedback voltage input. The strategy used in [72] is based on the dipolar PWM scheme which controls the neutral point voltage by adjusting the dead time.

IV. Conclusions

From a concept originating in 1980, the "teenage" years of the multilevel converter principle has produced a rapid maturing of this technology both as a new conceptual extension of the classical two-level inverter but also in the marketplace as a preferred embodiment for medium voltage applications. The authors contend that the prospects for this technology are very bright and we will witness an ever widening field of applications in the next decade.

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