Performance Improvement of Half Controlled Three Phase PWM Boost Rectifier

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Abstract— **The potential of the half controlled three phase pulse-width modulated (PWM) boost rectifier is investigated based on theoretical analysis, simulations and experiments. The main advantages of this rectifier are 1) a simpler and economical system compared to a full controlled PWM rectifier (reduced controlled switch count, single power supply for gate drives, and shoot-through free leg structure) and 2) better performance compared to a diode rectifier (actively controllable dc link voltage and lower input current total harmonic distortion (THD)). In particular, it is shown in this paper that input current THD of this rectifier can be reduced by intentionally introducing a lagging power factor current command. Several issues for further performance improvement are pointed out for future work.**

I. Introduction

The diode rectifier is one of the most commonly used front end circuits for power conversion systems. Although it is a simple and economical choice, its performance is accordingly poor, since it results in high input current total harmonic distortion (THD) and provides no control on the dc link voltage. The full controlled pulse-width modulated (PWM) rectifier has better performance [1], [2], and some variations of it have been reported [3], [4]. It is however difficult to justify its high cost for low power applications.

One of the alternatives to realize a cost effective solution is discontinuous current mode diode rectifier which has a single controlled switch on the dc link [5], [6]. The switch has to carry a large peak current due to the discontinuous conduction mode of operation, but it can provide satisfactory performance in applications where the power rating is limited to about $6 \sim 8$ [kW].

Another possible choice is to use the half controlled rectifier. Two typical topologies for three phase applications are shown in Fig. 1 and Fig. 2. The half controlled buck topology is analogous to the half controlled thyristor rectifier where the thyristors are replaced with gate turn-off switches such as insulated gate bipolar transistors (IGBT's). This buck topology is beyond the scope of this paper.

It has been reported that the half controlled boost topology offers large input current THD [7]. However, the potential of this rectifier has not yet been fully investigated. The features of the half controlled three phase PWM boost rectifier can be categorized into two groups - a) ones compared to full controlled PWM boost rectifiers and b) ones compared to diode rectifiers. The former are

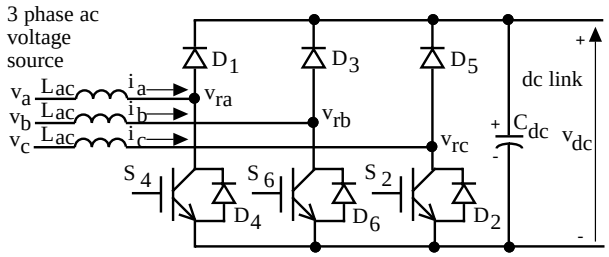

Fig. 1. Half controlled three phase PWM boost rectifier

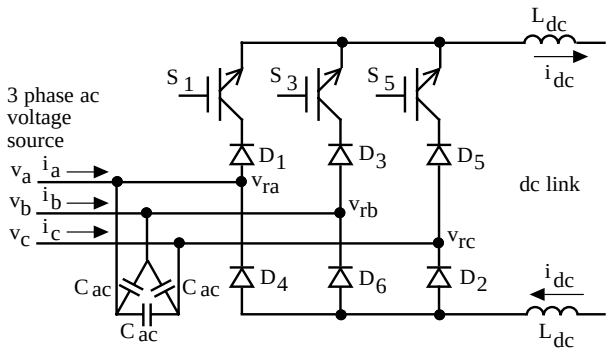

Fig. 2. Half controlled three phase PWM buck rectifier

itemized as follows:

a) Simpler structure compared to full controlled PWM rectifier;

i) three controlled switches and gate drives;

ii) single power supply for three gate drives;

iii) shoot through free leg structure;

Item a)-i) is self explanatory from Fig. 1. Item a)-ii) comes from the common emitter structure in three legs. Item a)-iii) results from the fact that one of two switches in a leg is a diode.

It may be noted that the half controlled boost rectifier topology does not have power regenerating capability. This disadvantage is incurred at the cost of obtaining shoot through free leg structure by eliminating one of controlled switches in a leg.

The features compared to the diode rectifiers are itemized as follows:

b) Better performance compared to diode rectifier;

i) actively controlled dc link voltage;

ii) lower input current THD;

Item b)-i) comes from utilization of controlled switches in each leg.

As for item b)-ii), one would intuitively expect lower input current THD than that of diode rectifiers because the

half controlled rectifier has actively controlled switches which can be used for input current control. This is however not always true as shown in the following sections.

The main focus of this project is to analyze the circuit behavior of the half controlled three phase PWM boost rectifier and causes of its input current distortion, and reduce it to a reasonable level.

Topologically, further variations of controlled switches and diodes combination are possible. For example, one can obtain similar configuration to Fig. 1 by putting the upper three controlled switches and eliminating lower three controlled switches. However, in order to take advantage of emitter common structure, the topology shown in Fig. 1 is the focus in this paper. The other combinations of controlled switches and diodes are not taken into account here, because they do not produce identical current waveforms in all the three phases.

In the following sections, theoretical analysis, circuit simulation and experimental results are presented, where all the notations representing voltage, current, and switching devices correspond to those in Fig. 1 unless otherwise specified.

II. Theoretical Analysis

Throughout the theoretical analysis presented in this section, the following assumptions are made:

1) hysteresis current regulator is used for input current control;

2) switching frequency component is negligible (local time averaged analysis is applicable);

3) all the power loss components are negligible;

4) dc link voltage is kept sufficiently high so that the peak of sum of ac source voltage and ac side inductance voltage drop is less than dc link voltage, that is approximately

$$V_{dc} > \sqrt{2}\sqrt{3}[V_\phi^2 + (\omega L_{ac} I_\phi)^2]^{\frac{1}{2}} \tag{1}$$

where V_ϕ and I_ϕ are phase voltage and current, respectively, in rms.

It has been reported that the half controlled PWM boost rectifier has low frequency input current distortion even in the *single phase* case [8]. This is caused by its incapability to achieve four quadrant operation on instantaneous basis, i.e. the half controlled *single phase* PWM boost rectifier can not synthesize rectifier terminal voltage whose polarity is opposite to input current (2nd and 4th quadrants). This leads to distorted input current waveform at the beginning of every half cycle [8].

This is not the case for the half controlled *three phase* topology. Fig. 3 shows ac quantities for unity power factor and sinusoidal input current operation, where the asterisks represent *desired* quantities. The ac voltages are assumed to be measured with respect to the neutral point of three phase voltage source.

Looking at the beginning of sector 6 for example, since rectifier terminal voltage v_{ra} must be lagging behind i_a^* by angle ϕ specified in the figure, a small negative rectifier terminal voltage v_{ra}^* has to be synthesized with positive phase current i_a. This can be done by utilizing the most negative rectifier terminal voltage v_{rb} and duty ratio control of switch S_4. The half controlled three phase topology can successfully synthesize sinusoidal *positive half cycle* current based on the same operating principle as that of dc-dc boost converter, as long as (2), which is obtained with a geometrical inspection, is satisfied.

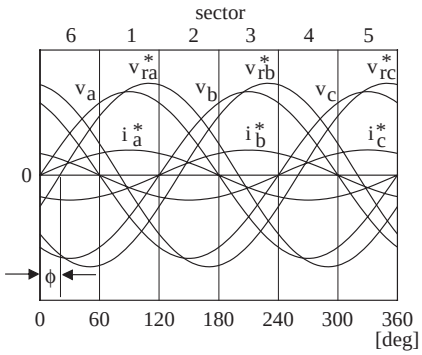

Fig. 3. Voltage and current waveforms of three phase PWM rectifier for unity power factor and sinusoidal input current operation

$$\frac{\sqrt{3}}{2} V_\phi - \frac{3}{2}\omega L_{ac} I_\phi^* > 0 \tag{2}$$

The condition of (2) is relaxed if one intentionally introduces a small lagging current command. If input current becomes in phase with rectifier terminal voltage, no such condition as (2) is necessary because the polarity of input current and rectifier terminal voltage is always the same (1st and 3rd quadrants).

It is interesting to notice that if one introduces an intentional lagging current command such that only 1st and 3rd quadrant operation is needed, then the abovementioned low frequency current distortion in half controlled *single phase* topology can be eliminated at the cost of a small lagging fundamental power factor. This issue will be reported by the authors in a future paper.

For negative half cycle current, the circuit behavior is quite different. The situation can be described with the transition from sector 2 to sector 3 in Fig. 3 for phase a without losing generality. Well controlled positive half cycle current of phase a is now entering into the negative half cycle. The only way for i_a to become negative is to make diode D_4 conduct. It is, however, impossible for D_4 to immediately start conducting because D_4 is reverse biased by the most negative phase, c. A clearer picture can be obtained by three phase vector diagrams as shown in Fig. 4 which illustrate transition from sector 2 to sector 3. Physical quantities of voltages and currents can be read from projection of vectors on the horizontal axis.

If only one phase current is in negative half cycle, Fig. 4 (a), two positive currents, i_a and i_b, are well controlled and the negative current, i_c, is automatically determined by Kirchhoff's current law. Then, all the three phase currents are well controlled as

$$i_a = \sqrt{2} I_\phi^* \sin(\omega t - \theta^*) \tag{3}$$

$$i_b = \sqrt{2} I_\phi^* \sin(\omega t - \theta^* - 120^\circ) \tag{4}$$

$$i_c = \sqrt{2} I_\phi^* \sin(\omega t - \theta^* + 120^\circ) \tag{5}$$

where θ^* is lagging angle of current command and $\theta^* = 0$ for the time being. This mode is called the *fully controlled mode* in the following explanation.

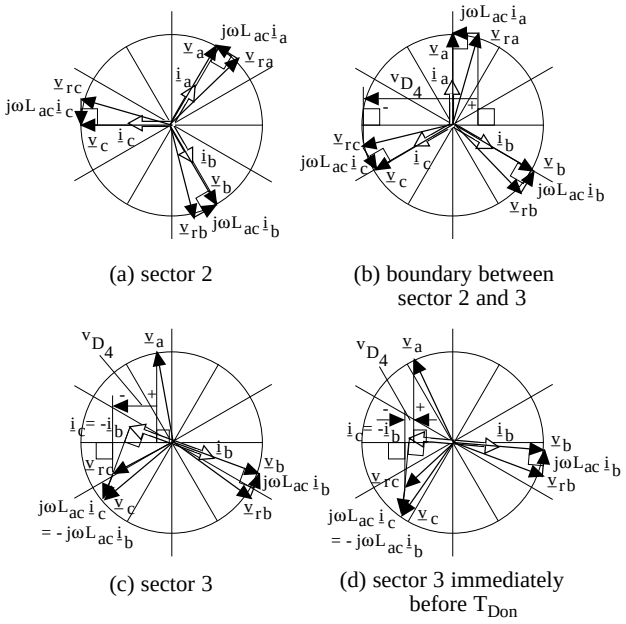

Fig. 4. Three phase vector diagrams of half controlled three phase PWM boost rectifier for unity power factor current command operation

On the boundary between sector 2 and sector 3, Fig. 4 (b), i_a tries to reverse from positive to negative. It is however impossible for anti-parallel diode D_4 to immediately conduct because it is reverse biased. This reverse voltage is expressed in the figure as V_{D4}, which is difference between the projection of two rectifier terminal voltage vectors, $\underline{v}_{ra}$ and $\underline{v}_{rc}$, on the horizontal axis. Until D_4 is forward biased, phase a carries no current as shown in Fig. 4 (c) and (d). The three phase currents in this situation are expressed as

$$i_a = 0 \tag{6}$$

$$i_b = \sqrt{2} I_\phi^* \sin(\omega t - \theta^* - 120^\circ) \tag{7}$$

$$i_c = -i_b \tag{8}$$

This mode is called the *incoming negative current zero mode*.

After D_4 is forward biased, current sharing between the two negative phases, a and c, is determined in passive fashion because no active switch is effective in these two phases. Analytical expression of this case can be obtained in the same manner as in the analysis of commutation overlap period in a diode or thyristor rectifier, as follows:

$$\begin{aligned} i_a = {} & \frac{\sqrt{3}V_\phi}{\sqrt{2}\omega L_{ac}}[\cos(\omega t + 150^\circ) - \cos(\omega T_{D\mathrm{on}} + 150^\circ)] \\ & - \frac{I_\phi^*}{\sqrt{2}}[\sin(\omega t - \theta^* - 120^\circ) - \sin(\omega T_{D\mathrm{on}} - \theta^* - 120^\circ)] \end{aligned} \tag{9}$$

$$i_b = \sqrt{2} I_\phi^* \sin(\omega t - \theta^* - 120^o) \tag{10}$$

$$\begin{aligned} i_c &= -i_a - i_b \\ &= -\frac{\sqrt{3}V_\phi}{\sqrt{2}\omega L_{ac}}[\cos(\omega t + 150^\circ) - \cos(\omega T_{D\mathrm{on}} + 150^\circ)] \\ &\quad - \frac{I_\phi^*}{\sqrt{2}}[\sin(\omega t - \theta^* - 120^\circ) + \sin(\omega T_{D\mathrm{on}} - \theta^* - 120^\circ)] \end{aligned} \tag{11}$$

where $T_{D\mathrm{on}}$ is the instance at which diode D_4 starts conducting measured from the time origin of v_a, i.e. positive zero-crossing point of v_a. This mode is called the *passive commutation mode*. After this mode, the circuit has two possible behaviors.

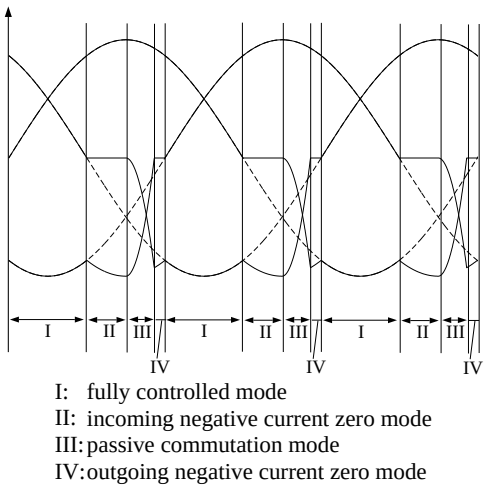

Fig. 5. Operating modes of half controlled three phase PWM boost rectifier

If i_c reaches zero before i_c^* becomes positive, the three phase current expressions are

$$i_a = -i_b \tag{12}$$

$$i_b = \sqrt{2} I_\phi^* \sin(\omega t - \theta^* - 120^\circ) \tag{13}$$

$$i_c = 0 \tag{14}$$

In this mode, negative current is completely taken over by i_a from i_c. This point is clear by comparing (12) $\sim$ (14) with (6) $\sim$ (8). This mode is called the *outgoing negative current zero mode*. After this mode, the circuit behavior returns to the *fully controlled mode* expressed by (3) $\sim$ (5) when i_c^* becomes positive.

If i_c reaches zero after i_c^* becomes positive, the *passive commutation mode* expressed by (9) $\sim$ (11) continues until i_c rejoins i_c^*. Then, the circuit behavior returns to the *fully controlled mode* expressed by (3) $\sim$ (5), and the *outgoing negative current zero mode* does not take place. In this case, a certain portion of positive half cycle current is distorted by invasion of the *passive commutation mode*.

Fig. 5 shows a simplified sketch of the current waveforms. Each 120 [deg] can be divided into mode I $\sim$ IV described above. Fig. 6 shows analytical input current waveforms and spectrum calculated based on (3) $\sim$ (14) with *MATLAB*, where it is assumed that rms line to line voltage $V_{ll} = 230[V]$, $I_\phi^* = 23.5[A]$ for $\theta^* = 0$ with 9 [kW] power transfer, and $L_{ac} = 3.0[mH]$. In this example, a large input current THD, 27.0 [%], is observed. One can also recognize a certain amount of even harmonics due to asymmetrical current waveform between positive and negative half cycles. The *outgoing negative current zero mode* is excluded and the *passive commutation mode* enters into the beginning of positive half cycle. It is dependent on ac side inductance and input current whether or not the *outgoing negative current zero mode* takes place.

In PWM rectifiers, unity power factor operation and command are always desired and used [1] $\sim$ [4]. It is however possible to reduce the input current THD observed

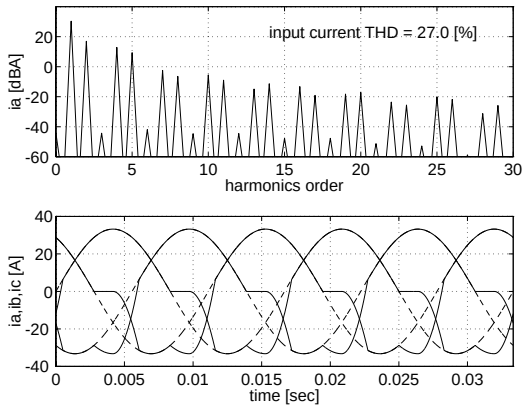

Fig. 6. Input current waveforms and spectrum based on theoretical analysis for unity power factor current command operation, θ^* =0 [deg], V_{ll} =230 [V], I_ϕ^* =23.5 [A], P_{out} =9 [kW], L_{ac} =3.0 [mH], input current THD=27.0 [%]

above by intentionally introducing a small lagging angle into the current command, i.e. $\theta^* > 0$ in (3) $\sim$ (14).

Fig. 7 shows ac quantities for 20 [deg] lagging power factor operation. In this example, the operating region in which the polarities of rectifier input terminal voltage and input current are opposite (2nd and 4th quadrants) is at the end of each half cycle. The condition with which one can guarantee well controlled sinusoidal *positive half cycle* current is obtained with a geometrical inspection as

$$V_\phi \cos(30^\circ + \theta^*) + \tfrac{3}{2}\omega L_{ac} I_\phi^* - V_\phi \sin\theta^* > 0 \qquad (15)$$

Fig. 8 shows three phase vector diagrams illustrating the transition from sector 2 to sector 3 in Fig. 7. Fig. 8 (a) shows three phase vectors towards the end of sector 2. Just after entering sector 3, active switch S_4 is still active until i_a becomes zero, because i_a is in positive half cycle. When i_a reaches zero, Fig. 8 (b), phase a loses control. However, the reverse bias across D_4, i.e. V_{D4} in Fig. 8 (b), is smaller than that of unity power factor current command operation shown in Fig. 4 (b). Fig. 8 (c) and (d) show vector diagrams for an *incoming negative current zero mode* and for the instance at which D_4 turns on, respectively. Comparing Fig. 8 (b) $\sim$ (d) with Fig. 4 (b) $\sim$ (d), one can recognize that the period during which D_4 can not conduct is shorter in Fig. 8, about 10 [deg], than in Fig. 4, about 30 [deg].

Fig. 9 shows analytical input current waveforms and spectrum calculated based on (3) $\sim$ (14) with *MATLAB* for θ^*=20 [deg] with the same V_{ll}, P_{out} ($I_\phi^* = 24.2[A]$), and L_{ac} as in Fig. 6. In this example, *outgoing negative current zero mode* is observed. The input current THD is decreased down to 12.1 [%]. Although a certain amount of even harmonics are still present, they are also smaller than those of Fig. 6.

The solid curves in Fig. 10 and Fig. 11 show input current THD vs. current command lagging angle characteristics with ac side inductance L_{ac} and dc output current I_{dc} as parameters, respectively, calculated with *MATLAB* based on (3) $\sim$ (14), where 600 [V] dc link voltage and 9 [kW] rated power are assumed. Then, 3.0 [mH] of L_{ac} corresponds to about 0.2 [pu].

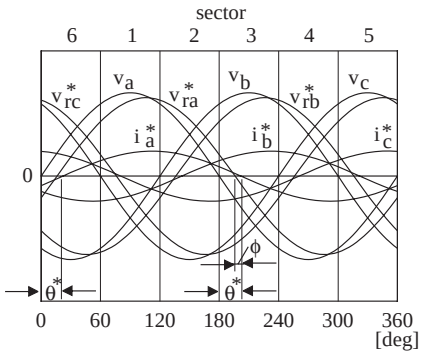

Fig. 7. Voltage and current waveforms of three phase PWM rectifier for 20 [deg] lagging current operation

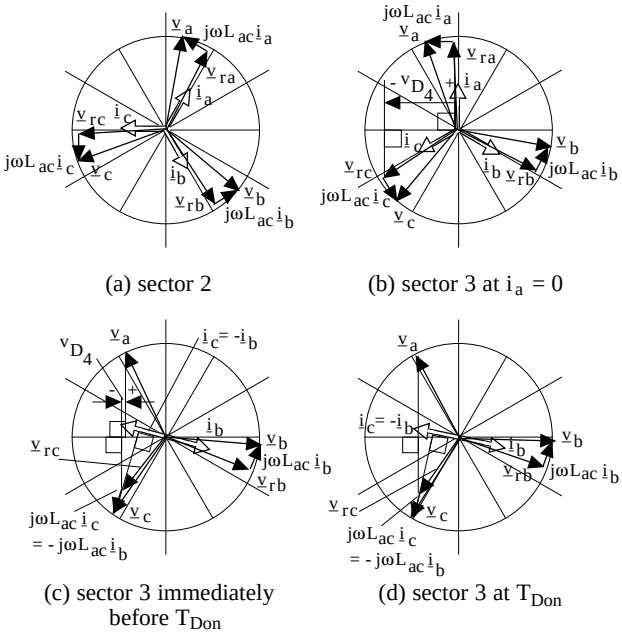

Fig. 8. Three phase vector diagrams of half controlled three phase PWM boost rectifier for 20 [deg] lagging current command operation

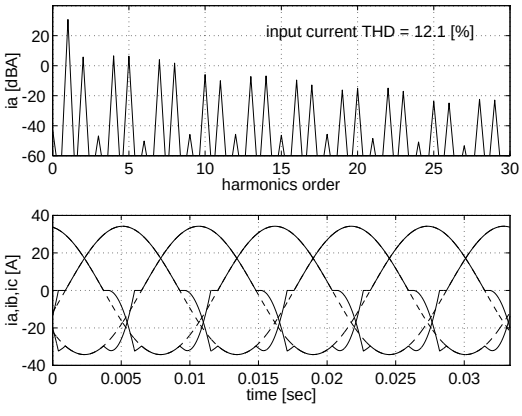

Fig. 9. Input current waveforms and spectrum based on theoretical analysis for 20 [deg] lagging current command operation, θ^* =20 [deg], V_{ll} =230 [V], I_ϕ^* =24.2 [A], P_{out} =9 [kW], L_{ac} =3.0 [mH], input current THD =12.1 [%]

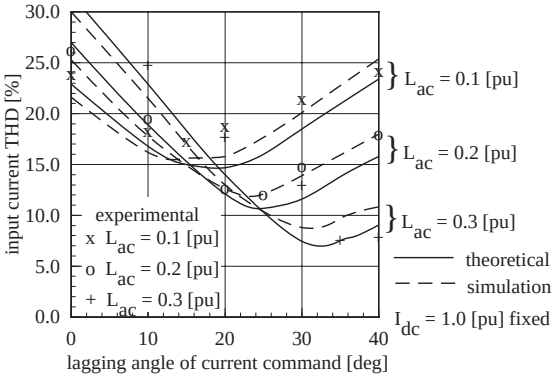

Fig. 10. Input current THD vs. current command lagging angle characteristics with L_{ac} as a parameter

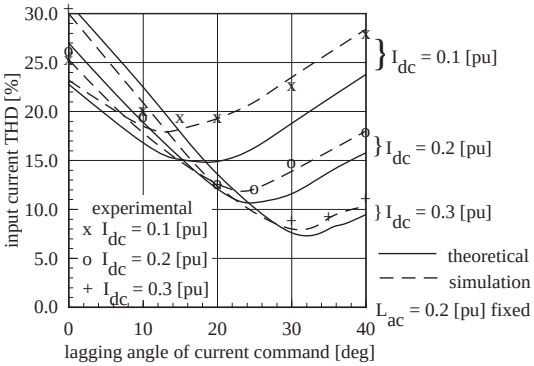

Fig. 11. Input current THD vs. current command lagging angle characteristics with I_{dc} as a parameter

It may be seen from these figures that the input current THD is dependent on ac side inductance and operating point. These results suggest that one of possible control principles is to set up lagging current command such that the rectifier traces the trajectory of minimum input current THD.

III. Simulation Results

Fig. 12 and Fig. 13 show simulation results computed with $SABER$ for the same operating conditions as those of Fig. 6 and Fig. 9, respectively. Characteristics of input current THD vs. current command lagging angle obtained from $SABER$ simulation are shown as the dashed curves in Fig. 10 and Fig. 11. They are in reasonably good agreement with those of the theoretical analysis. The discrepancy between the circuit simulation and theoretical results mainly arises from lossy components modeled in the $SABER$ simulation such as resistance in ac side inductors, dc link capacitor equivalent series resistance (ESR), and voltage drops across semiconductor devices.

IV. Experimental Results

Fig. 14 shows input current waveforms and spectrum obtained from a hardware experiment for the same operating condition as those of Fig. 6 and Fig. 12. Fig. 15 shows those for 25 [deg] lagging current command operation. The plots shown as 'x', 'o' and '+' in Fig. 10 and Fig. 11 are measured points obtained in hardware experiments. The theoretical analysis and simulation results presented in the preceding sections are verified by the experimental results.

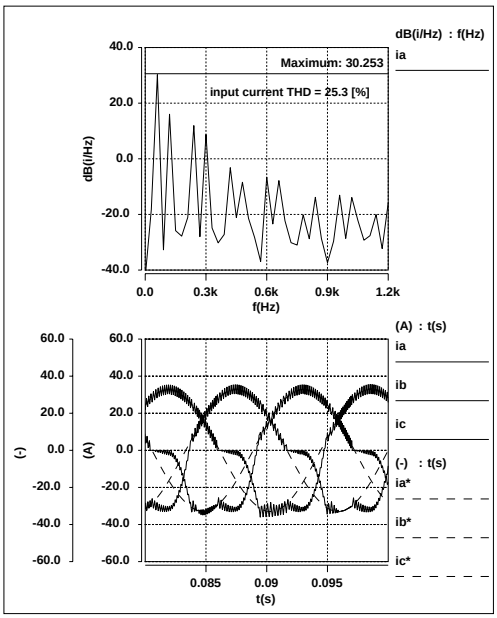

Fig. 12. Input current waveforms and spectrum simulated with $SABER$ for unity power factor current command operation, θ^* =0 [deg], V_{ll} =230 [V], V_{dc} =600 [V], I_{dc} =15 [A], P_{out} =9 [kW], L_{ac} =3.0 [mH], input current THD =25.3 [%]

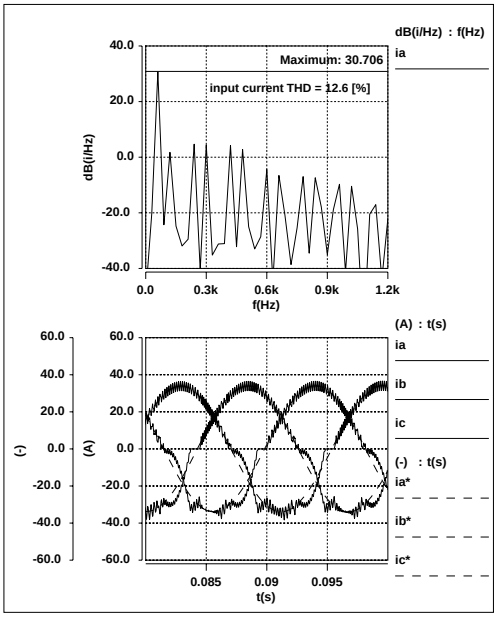

Fig. 13. Input current waveforms and spectrum simulated with $SABER$ for 20 [deg] lagging current command operation, θ^* =20 [deg], V_{ll} =230 [V], V_{dc} =600 [V], I_{dc} =15 [A], P_{out} =9 [kW], L_{ac} =3.0 [mH], input current THD =12.6 [%]

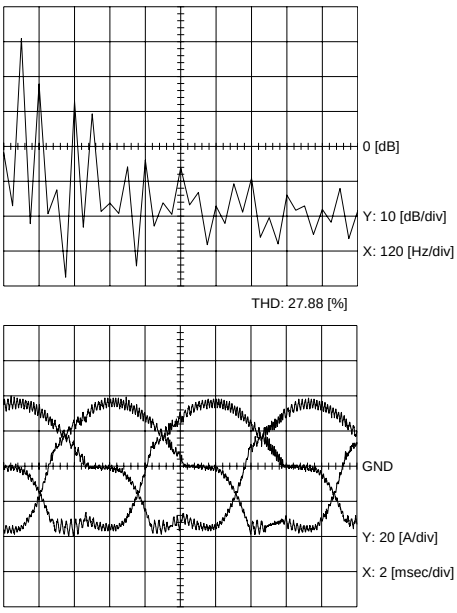

Fig. 14. Experimental input current waveforms and spectrum for unity power factor current command operation, θ^* =0 [deg], V_{ll} =230 [V], V_{dc} =600 [V], I_{dc} =15 [A], P_{out} =9 [kW], L_{ac} =3.1 [mH], input current THD =27.9 [%]

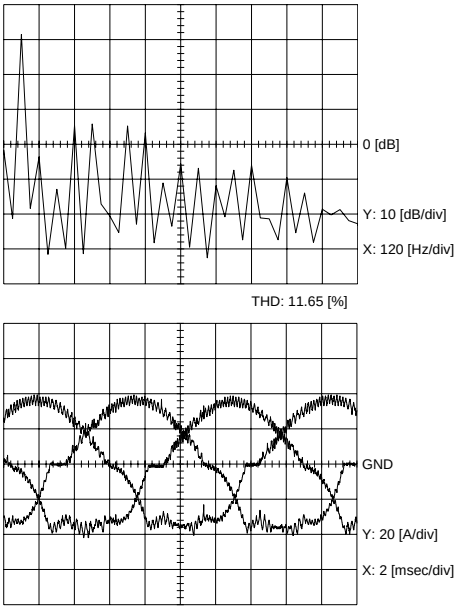

Fig. 15. Experimental input current waveforms and spectrum for 25 [deg] lagging current command operation, θ^* =25 [deg], V_{ll} =230 [V], V_{dc} =600 [V], I_{dc} =15 [A], P_{out} =9 [kW], L_{ac} =3.1 [mH], input current THD =11.7 [%]

V. Scope for Future Work

The input current THD reduction presented in this paper was obtained at the cost of lagging fundamental power factor. One might compensate this effect by placing a three phase capacitor between the utility input terminals and ac side three phase inductors. In this case, special care should be taken to avoid unwanted L-C resonance.

It is evident that the even harmonics observed in the preceding sections might excite undesirable resonance. Since the positive half cycle of input currents is reasonably under control, one would be able to reduce the even harmonics by controlling positive half cycle waveforms to mimic negative half cycle waveforms so that the half wave symmetry can be maintained.

As shown in Fig. 11, the input current THD reduction effect is highly operating point dependent. In particular, minimum input current THD obtainable by this scheme increases as the load current decreases. One might mitigate this problem by switching the control scheme from PWM current control to simultaneous switching of all the three controlled switches with a fixed duty ratio for discontinuous current mode of operation. This operation is an equivalent to that of the discontinuous current mode diode rectifier [5], [6]. Since a half controlled three phase boost rectifier has three controlled switches in parallel and the discontinuous mode should be applied only to light load condition, the switching devices do not have to carry large peak current.

VI. Conclusions

The potential of the half controlled three phase PWM boost rectifier has been investigated. The circuit behavior and causes of input current distortion have been analyzed by theoretical approach. The analytical results have been checked by detailed circuit simulations and experimental results. Through this process, it has been shown that the input current THD can be decreased by intentionally introducing a lagging power factor current command. Since this effect depends on ac side inductance value and operating point, quantitative data have been presented with various values of L_{ac} and I_{dc} as parameters. Several issues for further performance improvement have been pointed out for future work.

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Errata

Fig. 11

Replace I_{dc} =0.1[pu] by I_{dc} =0.5[pu]
Replace I_{dc} =0.2[pu] by I_{dc} =1.0[pu]
Replace I_{dc} =0.3[pu] by I_{dc} =1.5[pu]
Replace x I_{dc} =0.1[pu] by x I_{dc} =0.5[pu]
Replace o I_{dc} =0.2[pu] by o I_{dc} =1.0[pu]
Replace + I_{dc} =0.3[pu] by + I_{dc} =1.5[pu]