An Active Gate Drive with Three-Stage Control and Fast Protection for High Power IGBTs

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Abstract

Active gate drive and fault protection technology can be used to obtain high performance switching and fault protection characteristics in IGBTs. This paper presents a three-stage active turn-on and turn-off gate driver integrated with a fast fault current limiting circuit. The proposed three-stage active gate drive technique is verified to be able to operate under the wide range of temperature conditions experienced by the devices. The integrated fast fault protection circuit allows the active gate drive to operate at a higher on-state gate voltage, which leads to reduction of the conduction loss. Also, due to the fault management strategy the active drive circuit can considerably improve the fault endurance capability of the device.

Keywords

IGBTs, Active gate drive, Short circuit protection, Gate drive circuit, Device characterization

Introduction

The gate drive circuit in a power converter is a critical component, which can affect its performance and reliability. Today it is possible to build Mega-watt power converters using high voltage IGBTs (HVIGBTs) [1], [2]. Limitations of the HVIGBTs available today include the di/dt magnitude during switching due to the reverse recovery characteristics of the free-wheeling diode during turn-on and the over-voltage generated during turn-off due to the parasitic inductance in the module and bus structure in these high voltage IGBT power converters [3].

To overcome limitations of conventional gate drive (CGD) circuits that uses fixed gate resistors, several active gate drive (AGD) circuits have been proposed and widely studied [4]-[6]. The AGDs improve the switching characteristics by reducing the turn-on and turn-off stresses, which can lead to improved utilization of the IGBT in the power converter. Circuits that improve the switching performance under normal conditions can result in degraded performance under fault conditions. Traditionally, fault current limiting circuits (FCLCs) for IGBTs have been studied to improve the fault endurance capability [6]-[8]. An integrated approach to improve switching and fault characteristics is important in gate drive design. This paper focuses on the three-stage active gate drive technique [9] and shows how this technique can be extended to include short circuit protection in IGBTs.

Three-Stage Active Gate Drive Scheme

To obtain optimized behavior for the high power IGBTs, this paper investigates the three-stage active gate drive technique integrated with a fault current limiting circuit, which has the following characteristics:

- Turn-on is optimized by reducing the delay time, controlling the turn-on di/dt and the associated reverse recovery effects, lowering the tail voltage and the associated tail voltage loss, and reducing the overall turn-on time.
- Turn-off is optimized by reducing the delay time, controlling the over-voltage, reducing the turn-off loss due to improved dv/dt characteristics, and reducing the total turn-off time.
- Lower conduction loss in the IGBT is obtained by using a higher on-state gate voltage. Both the initial peak fault current and the clamped fault current can be lowered by the use of fast clamped fault protection.

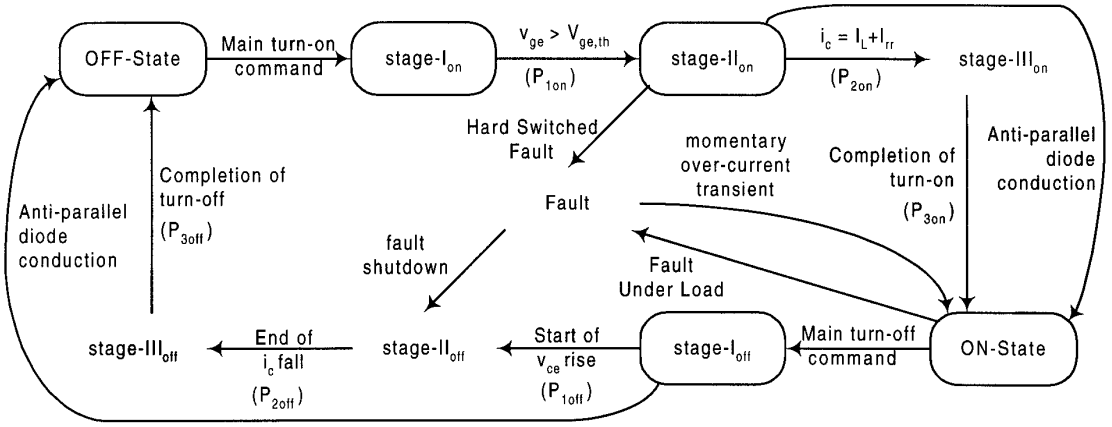

Fig. 1: The state transition diagram of the three-stage active gate drive circuit.

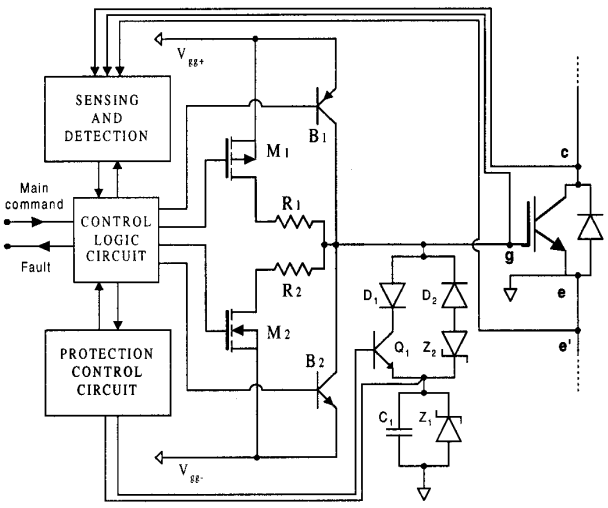

Fig. 2: Schematic of the three-stage active gate drive and protection circuit.

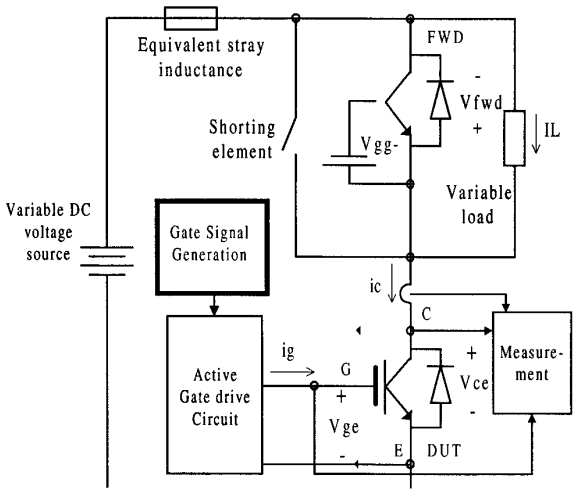

Fig. 3: The experimental setup used for investigating the gate drive circuit.

- Soft turn-off is provided after over-current and short current faults to limit the peak collector voltage.

The proposed active gate drive circuit uses a three-stage control technique for turn-on and turn-off. It is based on applying appropriate gate control during the different stages of the switching transient of an IGBT [10], [11]. The state transition diagram for the three-stage active gate drive with the protection circuit is shown in Fig. 1. During an IGBT turn-on switching transient stage-I would correspond to the delay time, stage-II to the current rise time, and stage-III would correspond to the voltage fall and the time required for the gate voltage to reach the positive gate bias voltage level (V_{gg+}) from the Miller plateau. The active gate control during the first stage is designed to minimize the delay time. The second stage controls the di/dt and dv/dt during switching. The third stage results in the IGBT rapidly reaching its final steady state. If the freewheeling diode is conducting the load current during turn-on, then the current rise duration is zero. Under these conditions in the three-stage active gate drive, the rapid charging action of the gate in stage-I up to IGBT's gate threshold voltage is followed by stage-II where the gate is slowly charged to V_{gg+}. If the free-wheeling diode is conducting during the turn-off command of the IGBT, there is no rise in the collector voltage after the turn-off delay time. Hence, the three-stage AGD continues in stage-I rapidly discharging the gate and reaching the off-state gate bias voltage (V_{gg-}). The protection circuit against a short circuit fault situation is based on a combination of de-saturation voltage detection and monitoring the voltage, $v_{ee'}$, between the Kelvin and power emitter terminals of the device. The de-saturation detection is enabled from the end of stage-

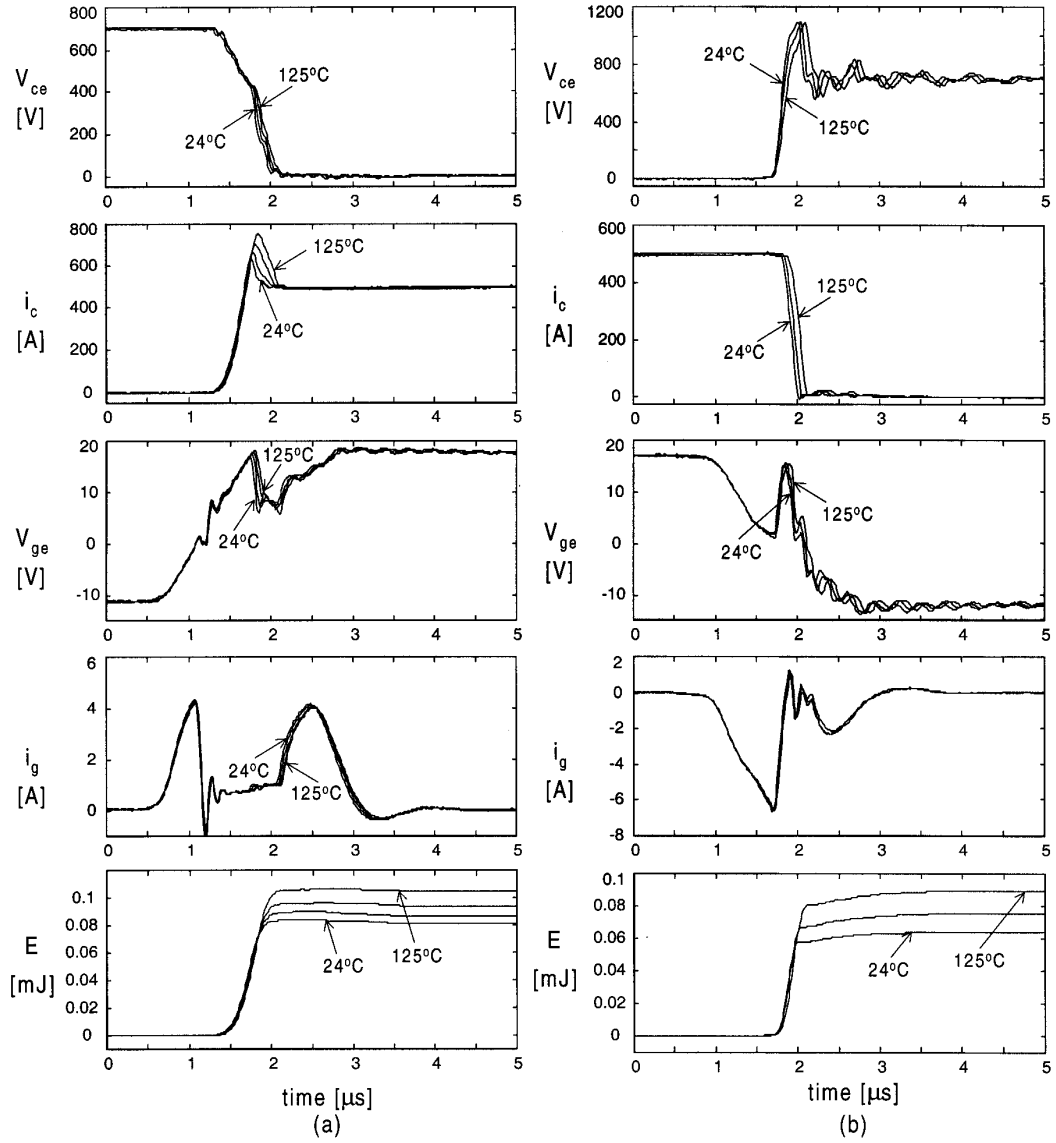

Fig. 4: Switching waveforms of an IGBT with the three-stage active gate drive showing collector voltage and current, gate voltage and current, and switching energy as temperature is varied from 24°C to 125°C. (a) Turn-on with T = 24, 60, 100, and 125°C. (b) Turn-off with T = 24, 60, and 125°C. The operating conditions are V_{dc} = 750V and I_L = 500A, V_{gg+} = 18V, V_{gg-} = -12V.

III of the active turn-on and the monitoring of $v_{ce'}$ is enabled from the start of current rise in the IGBT. The reduced total turn-on duration of the AGD results in a wider duration in which faults can be monitored in the three-stage active gate drive.

Implementation and Testing

A simplified schematic of the three-stage active gate drive integrated with the protection circuit is shown in Fig. 2. The gate amplifier has MOSFETs and BJTs, which are used in parallel to provide the gate current at both turn-on and turn-off switching operation. The use of MOSFETs, M_1 and M_2, in the gate drive allows one to easily obtain the peak gate current required during stages-I and III, for fast switching in high power IGBTs. Resistors R_1 and R_2 are small and are sized only to provide damping in the gate circuit. Also, one can fully utilize the gate power supply voltage and operate rail-to-rail by using a MOSFET. The BJTs, B_1 and B_2, allow gate current control during stage-II of the switching transient. During short circuit a combination of capacitor C_1 and zener Z_1 is used to reduce the gate voltage, for fault current limiting. The capacitor

rapidly discharges the gate after the fault and the zener is used to clamp the gate voltage after the fault.

A leg of a hard switched voltage source inverter circuit is used to validate the integrated active gate drive and protection circuit. The schematic of the test setup is shown in Fig. 3. A low inductance co-axial current transformer is used to measure the device current, which limits the overall parasitic inductance on the dc bus to less than 80nH. A two-pulse method is used to drive the IGBT with an inductor as the load. The controlled time duration for the first pulse is for obtaining the desired load current, which would be the initial value at turn-on of the second pulse. In case of the fault test a short circuit is applied across the upper device before applying the gate pulse to the device under test (DUT), which is the lower IGBT in the test setup. Both the upper and lower device are mounted on a hot plate and the temperature can be varied from room temperature to the maximum temperature specified by the datasheets. The test carried out in [9] used Powerex PT IGBT modules (CM600HA-24H 1200V, 600A). The tests conducted with Semikron NPT IGBT modules, (SKM500G123DS 1200V, 510A) are the results reported in this paper.

Active Turn-on

The active turn-on sequence is controlled to optimize a number of objectives. The turn-on is initiated by switching M_1 on and biasing B_1 in the active region. The turn-on delay and overall switching time is minimized by the peak current provided by M_1. Once the gate voltage reaches the threshold voltage M_1 is turned off. The gate current is now provided by B_1, which is biased in the active region to provide a controlled gate current. The turn-on di/dt is controlled to reduce the magnitude of the reverse recovery current. Stage-III is initiated by detecting the change in di/dt at the end of current rise, which corresponds to the snap-off of the free-wheeling diode in the hard-switched voltage source power converter. The rate of change of collector current is detected in the three-stage active gate drive by sensing the voltage between the Kelvin and power emitter of the IGBT module. After the snap-off of the free-wheeling diode, M_1 is turned on again. The gate Miller plateau duration is reduced by injecting additional current into the gate during turn-on stage-III. The switching loss is lowered by reducing the tail voltage by shortening the Miller plateau duration. This also reduces the total turn-on switching duration. Fig. 4(a) shows collector voltage and current, gate voltage and current, and the switching energy during the three-stage turn-on switching transient. If the IGBT is turning on into a fault situation, stage-II controls the turn-on di/dt, which limits the peak fault current. In this case, the protection circuit is activated, which limits the fault current level by reducing the gate voltage. The stage-III of turn-on is activated only if the dc bus voltage falls below a preset threshold voltage. Under fault conditions the current continues to rise without a snap off of the reverse recovery diode and the collector voltage does not settle to the on-state saturation value. This results in stage-III of turn-on to be inhibited in the gate drive circuit. This in turn prevents rapid rise in collector current during the turn-on operation under short circuit fault conditions.

Active Turn-off

When the IGBT is in the on-state, the turn-off command is typically given by the PWM controller in the power converter. The exception is the situation of fault turn-off when this command can either be given by the system controller in response to the fault signal or be internally generated by the gate drive if the fault condition continues beyond the fault endurance duration of the IGBT. A three-stage approach is used for normal turn-off to obtain minimal delay and switching loss while limiting the peak collector voltage. Fig. 4(b) shows the collector voltage and current, and gate voltage and current during a three-stage turn-off switching of the IGBT. The activation of stage-II of active turn-off is implemented by monitoring at the de-saturation of the collector voltage. In case of fault situations, the collector voltage is already de-saturated with the collector voltage close to the dc bus voltage. This eliminates stage-I of turn-off and the gate drive proceeds directly to stage-II. The reduced gate current during stage-II of the active turn-off provides soft shut-down of the IGBT. Hence, both fault turn-off and nominal turn-off follow the same strategy without conflict.

Temperature Variation

The adaptation of the three-stage AGD with temperature variation of the IGBT and freewheeling diode has to be validated in the range from 24°C to 125°C, which is a typical temperature range experienced by these devices in power converters. The current rise in the IGBT starts when the gate voltage goes above the threshold voltage. Hence, the transition point from stage-I to stage-II (P_{Ion}) depends on the operating temperature. The threshold voltage of the MOS gate decreases with increasing temperature [12]. If fixed timing is used to decide the P_{Ion} transition, the maximum operating temperature should be used to tune the gate drive for turn-on. The turn-on di/dt depends on the rate of charging of the gate capacitance and the transconductance of the

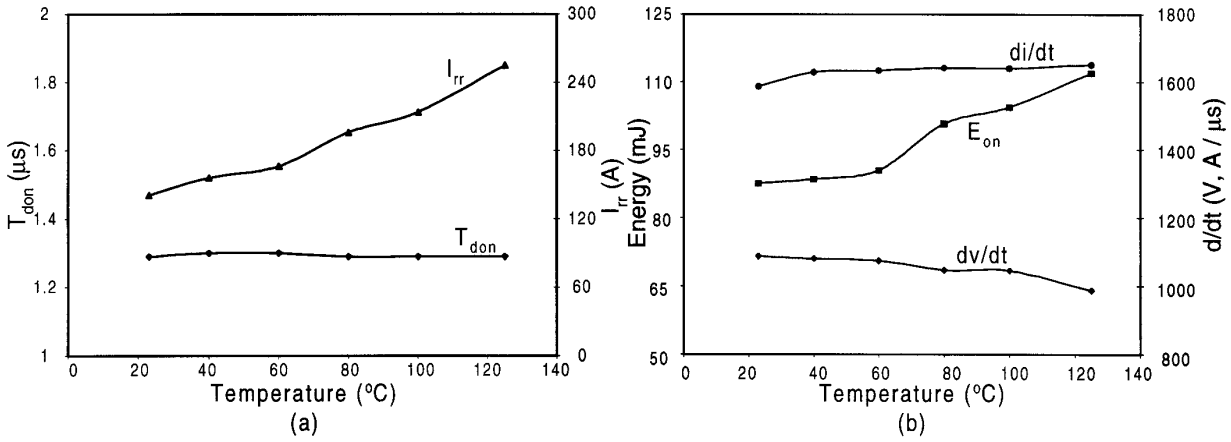

Fig. 5: Effect of temperature on the IGBT and freewheeling diode at turn-on. (a) The variation of reverse recovery and turn-on delay time. (b) Variation of di/dt, dv/dt, and switching energy at turn-on. The measurements are carried out on the Semikron IGBT under operating conditions of V_{dc} = 750V and I_L = 500A, V_{gg+} = 18V, V_{gg-} = -12V.

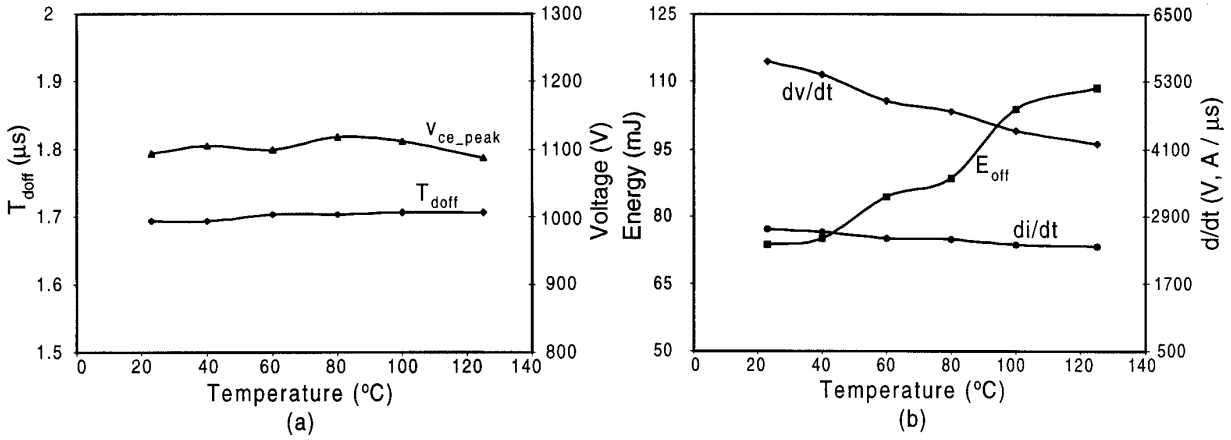

Fig. 6: Effect of temperature on the IGBT and freewheeling diode at turn-off. (a) The variation of peak voltage and delay time at turn-off. (b) Variation of dv/dt, di/dt, and switching energy at turn-off. The measurements are made using the Semikron IGBT under operating conditions of V_{dc} = 750V and I_L = 500A, V_{gg+} = 18V, V_{gg-} = -12V.

MOS channel of the IGBT. The reduction in mobility with increasing temperature adversely affects the transconductance of MOS gate.

The stored charge in the diode increases with temperature. This results in larger reverse recovery current and current rise duration during turn-on. The decision of the transition from stage-II to stage-III (P_{2on}) is based on sensing the current rise duration. Hence, the three-stage active gate drive adjusts the duration of stage-II, which adapts to the effect of temperature on the diode reverse recovery as can be seen in Fig. 4(a).

Figs. 5(a) and (b) shows the trends obtained using the test setup for the IGBT and the freewheeling diode with the three-stage AGD at turn-on. The measurements indicate that there is no significant effect of the variation of threshold voltage or transconductance with temperature on the three-stage AGD. However, there is a substantial change in the reverse recovery current with temperature. This leads to larger turn-on loss at a higher temperature.

As the temperature of an IGBT increases the minority carrier lifetime in the drift region has been found to increase [12]. This not only slows down the recombination process but it increases the internal pnp transistor gain of the IGBT. Both these phenomena causes an increase in the turn-off time with temperature.

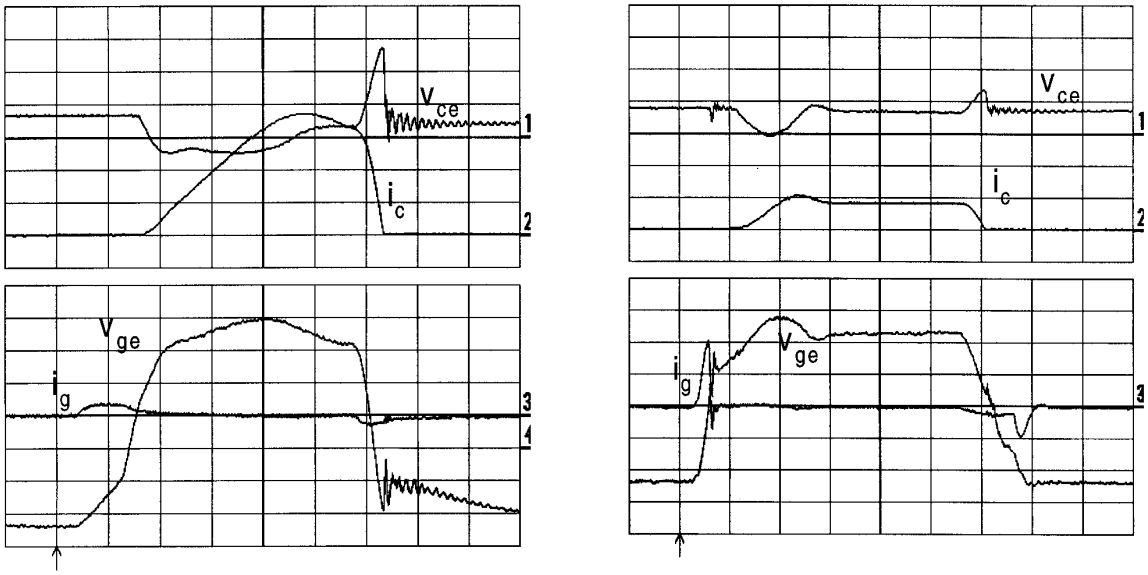

Fig. 7: Short circuit protection test carried out with the Semikron IGBT module (a) CGD without fault current limiting protection and Rg = 33Ω (b) AGD with fault current limiting protection. Ch1. V_{ce}: 200V/div, Ch2. I_c: 1000A/div, Ch3. I_g: 2A/div, Ch4. V_{ge}: 5V/div, time: 2ms/div. V_{dc} = 750V, V_{gg+} = 18V, V_{gg-} = -12V.

The reduction of threshold voltage and transconductance can manifest itself as an increase in the turn-off delay time with temperature. This can affect the transition from stage-I to stage-II (P_{1off} control point) in the AGD. The P_{1off} transition in the three-stage AGD is based on the rise in collector voltage at turn-off. This compensates for the variation of turn-off delay time with temperature. The small increase in T_{doff} with temperature can be seen from Figs. 4(b) and 6(a). The turn-off dv/dt is reduced at higher temperature for a given current level because of the larger stored charge in the IGBT drift region. The reduction of turn-off dv/dt and di/dt with temperature leads to higher turn-off switching energy loss as can be seen from Fig. 6(b). The re-turn-on of the gate during active turn-off result is larger stored charge, resulting in a larger current tail at higher temperature. Hence, the turn-off switching energy with temperature increases more rapidly in an AGD compared to a conventional gate drive.

Fault Handling

Detection of the fault is performed by using a combination of de-saturation detection and estimation of the device current level using the voltage between the Kelvin and power emitter terminals of the IGBT. The transition from the controlled current rise in the IGBT to the turn-on steady state is performed only if no fault signal is detected. If there is a short circuit condition at turn-on, the protection circuit reduces the gate voltage and limits the fault current level, thus reducing the power dissipation during a fault. This allows one to use a higher on-state gate voltage for the device, which would result in a lower conduction voltage drop in the device. The main control circuit of the power converter is given the fault signal, and the gate drive turns off within the short circuit endurance time of the IGBT. The short circuit protection has to be co-ordinated with over-temperature protection to prevent failure due to repeated operation under fault conditions.

The power converters capability to ride through and survive an over-current or short circuit fault can be enhanced using a gate drive that can limit the fault currents. The use of a higher gate voltage can be dangerous under short circuit and over-current conditions because the resulting higher fault current can lead to large power dissipation and can destroy the IGBT. It has been shown in [7] that a combination of a capacitor and zener based FCLC can be effective in limiting both the peak and clamped fault current levels. The method of lowering the gate voltage under fault conditions instead to direct turn-off prevents inductive turn-off failure that can occur under peak fault current level [13], [14]. The fault current has to be turned off softly to prevent large over-voltage of the IGBT.

Figs. 7(a) and (b) illustrate the cases of short circuit fault occurrence with a conventional gate drive without the FCLC and the three-stage active gate drive with the FCLC respectively. The gate drive transits from stage-II of turn-on to a fault state to prevent large currents under fault conditions. A soft turn-off is required in case of over-current or short circuit shutdown to prevent large over-voltage that can damage the IGBT. This is achieved by preventing the activation of turn-off stage-I and moving directly to stage-II of the three-stage active turn-off. It can be seen from Fig. 7 that the fault turn-off in the conventional gate drive uses a large gate resistance (33Ω) but the turn-off over-voltage is much higher compared to the three-stage AGD.

Conclusions

This paper has discussed issues in the design of a three-stage AGD and its different modes of operation and validates its operation under a wide temperature range of the IGBT and freewheeling diode. The gate drive adapts itself to a wide range of operating conditions. The operation of the gate drive has been tested with IGBT modules from several manufacturers. The three-stage AGD has been integrated with the fast fault current limiting technique to protect the IGBT under fault conditions. Such characteristics are especially important for the high voltage IGBTs that are available today.

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