An Auxiliary Zero State Synthesizer to Reduce Common Mode Voltage in Three-Phase Inverters

Madhav D. Manjrekar Thomas A. Lipo

Department of Electrical and Computer Engineering
University of Wisconsin – Madison
1415 Engineering Drive
Madison, WI 53706, USA

***Abstract*- Common mode voltage produced by the modulation of three-phase power inverters creates significant amount of common mode conducted current in motor drives. As an alternative to inserting a large common mode choke to attenuate this common mode current, a modification to the inverter topology and the modulation strategy is proposed that can eliminate zero state components in common mode voltage produced by the inverter. With the proposed modification, it is observed that the inverter generates substantially low common mode voltage, thereby resulting in reduction of common mode current by several orders of magnitude. The topological structure, operating principles and performance characteristics are presented. A comparative evaluation of various alternatives studied in the literature to mitigate electromagnetic interference is also presented in the paper.**

I. INTRODUCTION

Electromagnetic Interference (EMI) has come a long way from the "black magic" approach of the early sixties to an almost exact science, with its analytical methods, measurement techniques, global standardization, modeling & simulation capabilities and development of effective mitigation tools [1], [2]. Historically, EMI first emerged as a serious problem in telecommunications, and ever since, it has been found to have affected areas much beyond the scope of telecommunications technology. In the first half of this century, electromagnetic disturbance sources were limited to motor-driven machinery and switching apparatus. But with the proliferation of power semiconductor technology and rapid spread of power electronic systems, interference related problems concerned with power equipment have increased significantly in intensity and frequency of occurrence [1].

In the broadest sense of its meaning, EMI can be pointed out as the principal culprit in almost any failure related to a normally working power conversion equipment which is not initiated by manufacturing defect or aging [2]. However, some of the primary problems that drew the attention of researchers worldwide to this field were ground currents and false tripping of the protection circuitry [3], reflected waves, overvoltages and associated insulation failures [4] and machine shaft voltages with the corresponding bearing currents and failures [5].

Generally, electromagnetic disturbance can be classified on the basis of either character (random, impulse or transient) or means of propagation (conducted EMI or radiated EMI). EMI has also been classified according to its frequency content and standards are developed to establish the acceptable levels of emission and susceptibility based on the frequency information [6], [7]. Conducted EMI is further divided into two modes: differential mode and common mode. Differential mode interference is that component which exists between two supply or output lines. Normally, the power/information transfer is carried on differential basis. Hence any existing component apart from the desired power/information components can be theoretically regarded as differential mode EMI. Common mode interference is that component which is present on all supply or output lines with respect to the common ground plane. With exception of a few special cases, it is desirable to have the common mode potential of all the conductors to be zero. This is because of the fact that a stray capacitance is almost always present between any conductor and the common ground. Thus a dynamic, non-zero common mode voltage results into a common mode current flowing into the ground. Because of the capacitive coupling, this problem exacerbates with higher dv/dt which can be attributed to higher switching speeds, which in practice, is desirable to improve the performance of Pulse Width Modulation (PWM).

This paper deals with the common mode voltage present at the output lines of a conventional three-phase Voltage Source Inverter (VSI). Common mode voltage produced by the modulation of three-phase power inverters creates significant amount of common mode conducted current in motor drives [5]. Whereas the ideal model of a motor drive has an infinite common mode impedance, in reality, the common mode impedance due to capacitive coupling through the machine to earth ground can be relatively small at modulation frequency creating significant common mode current. This current contributes to several unwanted problems such as coupling to nearby systems creating EMI, damaging the machine bearings and bearing lubrication and heating the conduit carrying the three-phase conductors [5].

As an alternative to inserting a large common mode choke to attenuate this common mode current, a modification to the inverter topology and the modulation strategy is presented that can eliminate zero state components in common mode voltage produced by the inverter. With the

0-7803-5589-X/99/$10.00 (c) 1999

proposed Auxiliary Zero State Synthesizer (AZSS), it is observed that the inverter generates substantially low common mode voltage, thereby resulting in reduction of common mode current by several orders of magnitude.

The following section of this paper presents a comparative evaluation of various alternatives studied in the literature to mitigate common mode voltage in three-phase inverters. This is followed by a description of the proposed AZSS. A brief analysis of modulation issues for AZSS is included in section IV. Section V presents simulation results confirming the efficacy of this approach. The paper concludes with a discussion of pros and cons of AZSS and few comments about the scope for further research.

II. Review Of Common Mode EMI Mitigation Techniques

The most basic solution to mitigate electromagnetic disturbance is to use simple L–C filters. Simplified schematics of such one-stage filters are shown in Figures 1 and 2. These are basic filter configurations and several variations (multistage, π–type, T–type) have been reported in literature [1].

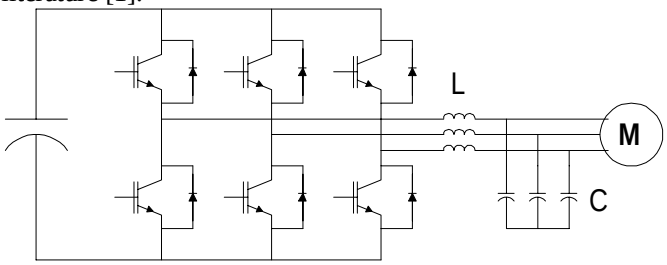


Figure 1. Simplified schematic of a VSI with differential mode L–C filter.

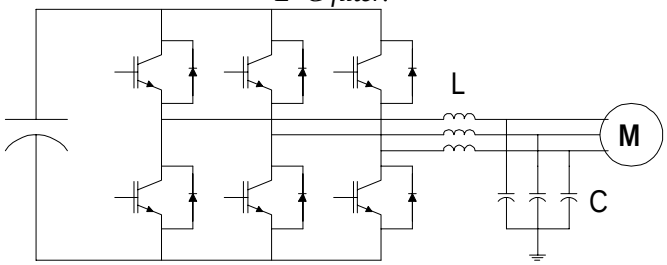


Figure 2. Simplified schematic of a VSI with common mode L–C filter.

The values of L and C are designed according to the required insertion loss of the filter for a given power rating of the inverter. One of the most difficult problems in designing these filters is staying within reactance limitations while providing a high insertion loss. It may be observed from Figures 1 and 2 that, the equivalent value of inductance for differential mode (line-line) EMI is far more than that for common mode (line-ground) EMI. Furthermore, because of the size limitations, the inductance of an air core solenoid coil arrangement is not more than 100 μH, while the value of capacitance is limited by safety and shock hazards to a few nanofarads [1]. Hence, with these given limitations on the values of L and C, one is not able to get the required attenuation with simple L–C filters.

To overcome this design problem, common mode choke coils with magnetic cores were developed that exhibit small impedance for differential mode components and relatively high impedance for common mode components [1]. Because of the high common mode inductance of common mode choke coils, the L–C product can be increased even if the value of the Y–connected capacitors is limited. A basic configuration is shown in Figure 3.

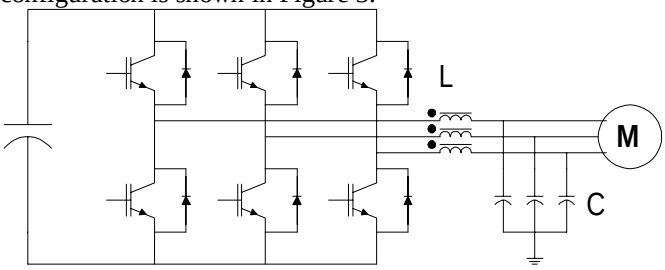


Figure 3. Simplified schematic of a VSI with common mode choke L–C filter.

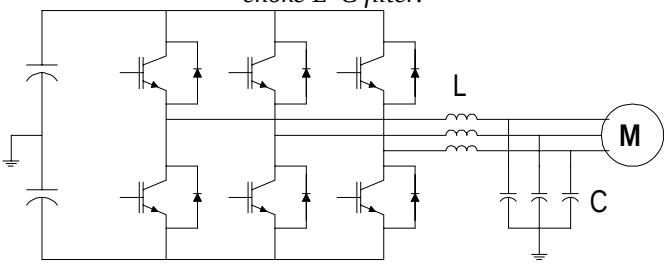


Figure 4. Simplified schematic of a VSI with differential/common mode L–C filter.

A combination of the conventional differential and common mode L–C filter (Figures 1 and 2) has been reported in [8]. A simplified schematic of this configuration is shown in Figure 4. It may be observed that this topology uses a split dc bus with the center point tied to earth ground. By doing so, it is possible to obtain a handle on differential as well as common mode EMI simultaneously. It has been reported that, such a configuration reduces both, differential and common mode dv/dt, thereby reducing motor terminal overvoltages, leakage current to ground and induced shaft voltages.

It has been claimed in reference [9] that introduction of conventional common mode choke is not effective to reduce the rms and average values of the leakage currents, although it serves the purpose of attenuating the peak values. The authors have proposed to use a common mode transformer to solve this problem. A simplified schematic of such a solution is shown in Figure 5. As may be seen from Figure 5, common mode transformer is basically an addition of another isolated winding, the terminals of which are shorted by a damping resistor, to the conventional common mode choke (Figure 3). The terminology "common mode transformer" is somewhat confusing and perhaps used to relate with the "common mode choke". Like the common mode choke, the common mode transformer does not play any role to attenuate the differential

mode EMI. However, it acts as a damping resistor for the common mode voltage and current, thereby damping the oscillations in leakage currents. It is shown theoretically and experimentally that the common mode transformer is capable of reducing the rms value of leakage current to 25%, while using a smaller core than that used in a conventional common mode choke.

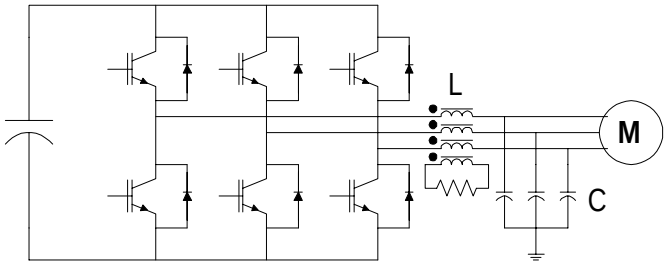


Figure 5. Simplified schematic of a VSI with common mode transformer L–C filter.

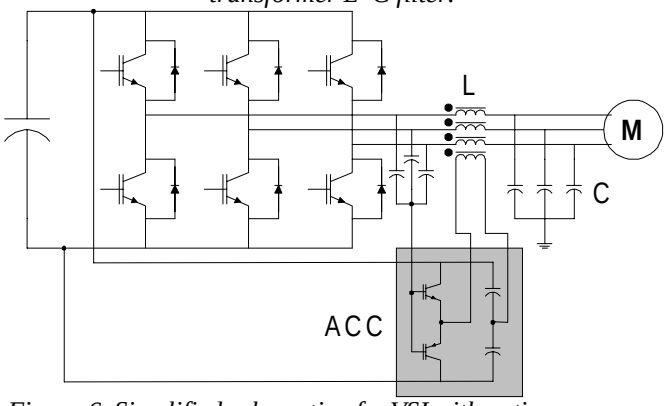


Figure 6. Simplified schematic of a VSI with active common-noise canceler.

Although the common mode transformer can damp the oscillatory ground currents, a small amount of aperiodic residual ground current still remains uncompensated owing to the passive nature of the solution. An active common–noise canceler (ACC) has been proposed in [10] to eliminate the common mode voltage produced by a PWM inverter. A simplified schematic of this circuit is shown in Figure 6. The ACC superimposes a compensating voltage on the inverter output. The compensating voltage applied by the ACC has the same amplitude as, but opposite polarity to the common mode voltage produced by the PWM inverter. As a result, the common mode voltage applied to the load can be canceled completely.

All the techniques discussed so far are variations of EMI compensation or cancellation techniques. These solutions either cancel the common mode voltage by auxiliary voltage generation or offer high impedance to prevent the common mode currents from flowing into the load or provide an alternative low impedance path to shunt the common mode current from the load. Reference [11] addresses the issues of common mode voltage generation due to the topological structure and modulation procedures. A well-known rule to minimize the common mode voltages/currents is "Circuit Balancing" [12]. However, the conventional three-phase, three-wire, two-level inverter is asymmetric in this respect, thereby becoming a direct cause of common mode voltages. A four-leg system as shown in Figure 7 has been presented in [11] to make the circuit symmetric about the ground potential. Such a configuration enables half the legs to be connected to the positive dc rail and half to be connected to the negative dc rail at all time. This maintains the common mode voltage to be identically equal to zero.

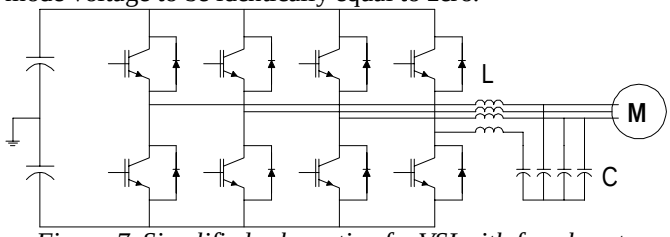


Figure 7. Simplified schematic of a VSI with four legs to impose symmetrical switching.

A sine triangle PWM technique that is used to control this four-leg inverter employs three carrier waves phase displaced by 120°. However, the modulation index has to be limited to 0.66 p.u. in this process in order to avoid the zero states where all the upper switches or all the lower switches are required to be closed. This not only affects the dc bus utilization, but also distorts the differential mode voltage. As an alternative strategy, modified space vector control scheme has been presented in [13]. Under this modulation, the zero state is realized on an average basis by alternate switching of two vectors that are adjacent to the original two active states used in the conventional space vector modulation. The authors also explore a more generalized four-dimensional modulation scheme on similar lines in [13]. Although these strategies demand no limitation on the modulation index, they do not comply with adjacent state switching, thereby imposing serious penalty on switching losses and harmonic distortion. This incapability to synthesize zero states without generating common mode voltage in four-leg topology was the principal motivation in the development of the auxiliary zero state synthesizer as explained in the following section.

III. The Auxiliary Zero State Synthesizer (AZSS)

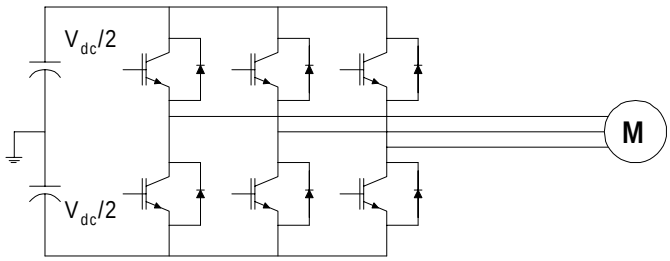
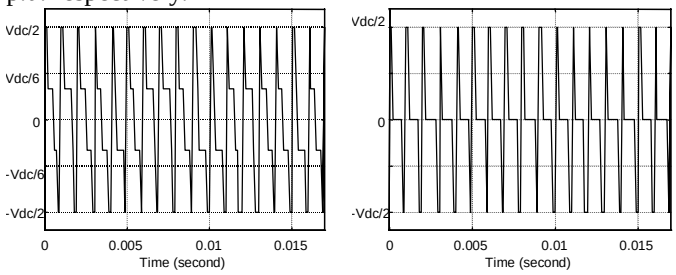


Figure 8. Simplified schematic of a conventional voltage source inverter.

Figure 8 shows a simplified schematic of the conventional VSI. The switching of the power devices is accomplished by employing any traditional pulse width modulation strategy. Split dc bus with a grounded center-

point is shown in this figure to demonstrate the reference for common mode voltage at load terminals. All the voltage measurements in this paper are done with reference to this point unless stated otherwise. Figures 9 and 10 show typical waveforms of the operation at modulation index 0.8 and 0.2 p.u. respectively.



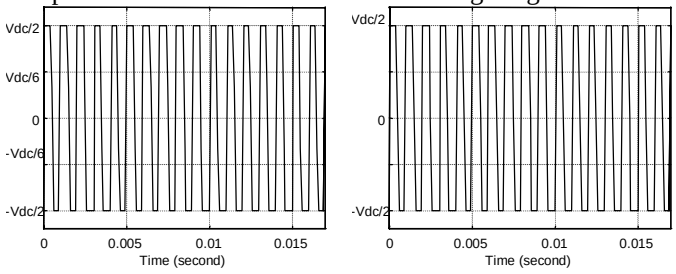
Common Mode Voltage *Zero State Synthesis*

Figure 9. Typical waveforms for a VSI at M.I. = 0.8 p.u.

From Figure 9 it is clear that the common mode voltage exhibits discrete steps of $\pm V_{dc}/6$ and $\pm V_{dc}/2$ which is a well-known phenomenon [12]. To simplify the analysis, the common mode voltage may be considered to be as contributed by two factors:

1. Asymmetrical switching synthesizing active states: This is due to 001, 010, 011... states [14] (Figure 14) where two upper/lower and one lower/upper switches are conducting simultaneously. This factor contributes to the synthesis of $\pm V_{dc}/6$ steps in the common mode voltage.
2. Asymmetrical switching synthesizing zero (null) states: The latter part is because of the zero state (000, 111) [14] (Figure 14) synthesis. This is when all the upper or lower switches are conducting which causes the common mode voltage to reach the peaks ($\pm V_{dc}/2$).

It may be observed that the frequency of synthesis of zero states is significantly high and can be said to be a dominant factor in the common mode EMI. This situation worsens when the converter is synthesizing a voltage with a small modulation index as illustrated in Figure 10. As may be seen from Figure 10, the common mode voltage is virtually composed of zero states when a small voltage is generated.



Common Mode Voltage *Zero State Synthesis*

Figure 10. Typical waveforms for a VSI at M.I. = 0.2 p.u.

As explained in the last section, Julian et al. [11] have proposed a solution of introducing a fourth leg and thus imposing symmetric switching conditions on the converter. This nullifies the effects of the first factor as mentioned earlier. But the solution presented in their paper falls short of compensating for the common mode voltage arising due to the zero states. Hence the authors do not permit zero states in the modulation which adversely affects bus utilization and adjacent state switching conditions [13].

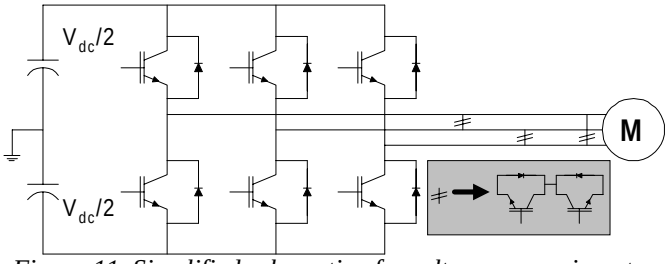


Figure 11. Simplified schematic of a voltage source inverter to synthesize alternative zero state.

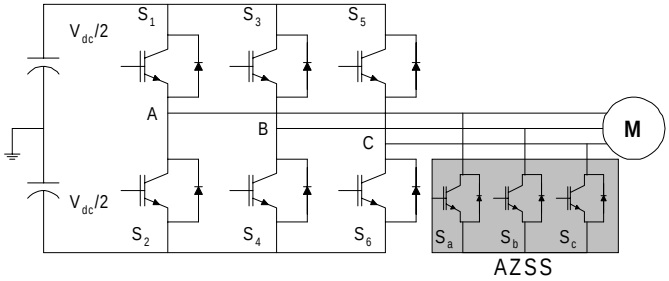
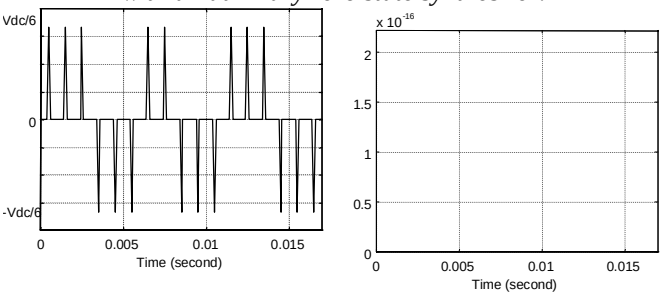


Figure 12. Simplified schematic of a voltage source inverter with an auxiliary zero state synthesizer.



Common Mode Voltage *Zero State Synthesis*

Figure 13. Typical waveforms for a VSI with AZSS at M.I. = 0.2 p.u.

As an alternative, an auxiliary circuit composed of three bi-directional switches may be used at the output terminals to synthesize zero states as shown in Figure 11. A single phase version of this approach has been proposed in [12] and investigated in detail in [15]. But, one needs six power devices to realize three bi-directional switches connected between line to line, which is an expensive and rather impractical solution. However it is possible to realize a bi-directional path between any two of three phases with only three devices as shown in Figure 12. Now one can use this three-switch module to synthesize zero state by closing all the three switches in the module and opening all the six switches in the inverter bridge. It may be noted that this strategy does not contribute to the common mode voltage as all the output terminals are floating. The corresponding voltage waveforms are shown in Figure 13, which on comparison with Figure 10, confirm that the common mode voltage has been substantially reduced.

It may be noted that the proposed AZSS consists of three devices with emitters tied together. It is also possible to build a complementary AZSS with three devices by tying their collectors. However, the gate drivers with the presented AZSS (Figure 12) require only one supply for all three devices owing to the common emitter configuration. The complementary AZSS would need three isolated supplies for gate drivers, and hence would be more expensive.

IV. Modulation Strategies

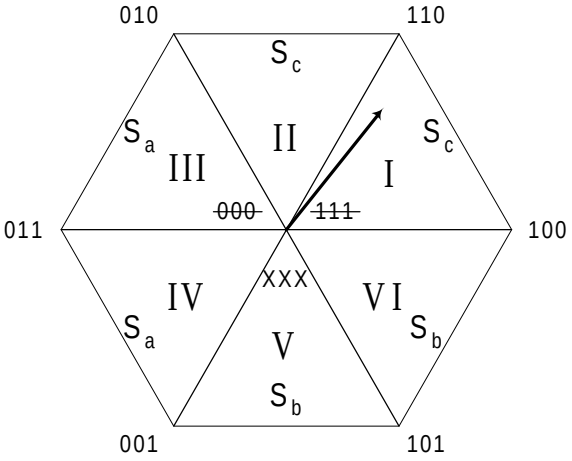


Figure 14. Vector space of a VSI with an AZSS.

Although economically attractive, the auxiliary circuit offers lesser degrees of freedom to control the switches to synthesize zero states. This requires careful design of a modulation strategy for the AZSS. A primary concern about defining such a scheme is to avoid a possible short circuit path when an upper device in the bridge and an AZSS switch is closed simultaneously at any phase leg. This connects the upper dc rail to the remaining two phase legs and may lead to a diametric shoot-through fault if any one of the lower switches in the bridge are closed. A simple solution to avoid such a scenario at transition from an active state to the zero state is to open all the active switches in the bridge, wait for a suitable blanking time and then close the switches in AZSS. Similarly, transition from the zero state to an active state can be accomplished by opening all the switches in AZSS, waiting for a suitable blanking time and then closing the desired active devices in the bridge. This strategy would ensure prevention of a possible short circuit across the dc bus. However a problem associated with this scheme is that, the modulation does not account for the current polarity [15]. Hence, once all the devices in the bridge are opened, the antiparallel diodes start conducting according to the polarity of the current in each phase. This may lead to connection of the phases to an undesired dc potential thereby losing volt-seconds and increasing differential voltage distortion. An alternative modulation scheme based on Space Vector Modulation (SVM) [14] is under investigation and will be reported in detail in near future. Presently, a brief account of such a scheme is given as follows:

Table I. Conventional Space Vector Modulation

State	000	100	110	100	000
Inverter Switches	S_2 S_4 S_6	S_1 S_4 S_6	S_1 S_3 S_6	S_1 S_4 S_6	S_2 S_4 S_6

Table II. Space Vector Modulation with AZSS

State	XXX	100	110	100	XXX
Inverter Switches		S_1 S_6	S_1 S_3 S_6	S_1 S_6	
AZSS Switches	S_a S_b S_c	 S_b S_c	 S_c	 S_b S_c	S_a S_b S_c

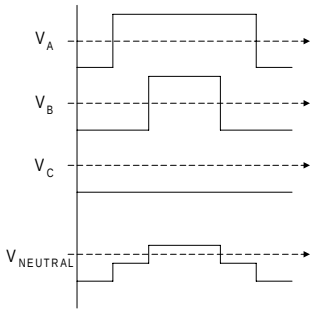


Figure 15. Waveforms with conventional SVM.

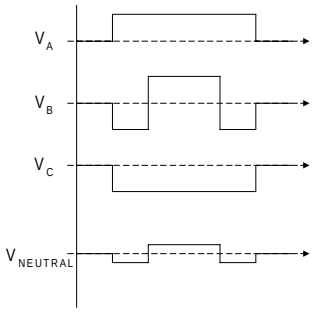


Figure 16. Waveforms with AZSS.

A voltage vector in Sector I as shown in Figure 14 is used as a candidate vector. Upon obtaining a suitable modulation strategy for this sector, it is fairly easy to extend it for the remaining sectors. The numbers 100, 110 … represent the states of the inverter switches and follow the conventional SVM terminology [14]. It may be noted that the zero states 000 and 111 have been cancelled in Figure 14 to represent not-allowed states. Instead, the zero state is synthesized by floating all the three phases, which is represented by state XXX in the figure.

Now the conventional modulation scheme to realize the given vector in Sector I is presented in Table I and the corresponding schematic waveforms are shown in Figure 15. The states are switched from 000↔100↔110. Table II summarizes the modulation strategy employed for the inverter with AZSS. The states are switched from XXX↔100↔110. State 100 is realized by closing switches S_1 and S_6 in the bridge with a bidirectional switch between phases B and C. So also, switch S_c is always closed in this sector and need not be switched at all. It may be noted that each one of three switches in AZSS can be closed for two sectors as shown in Figure 14. The schematic waveforms obtained through this strategy are shown in Figure 16. They show that the common mode voltage resulting from the zero state has been eliminated.

V. Simulation Results

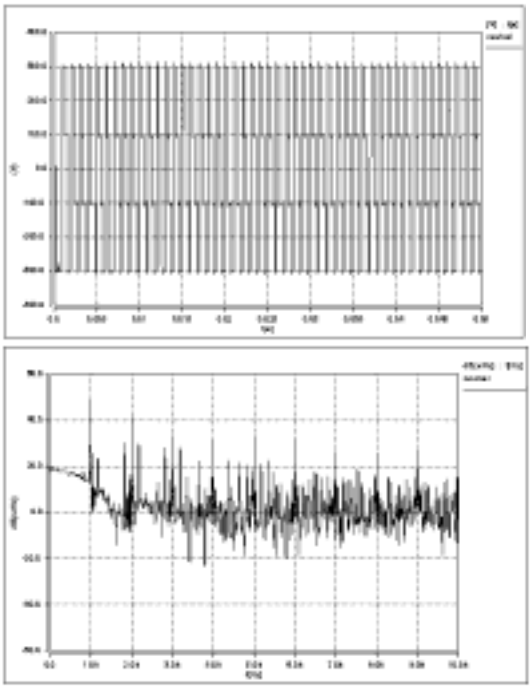


Figure 17. Time and frequency domain waveforms of the neutral voltage without AZSS at M.I. = 0.5 p.u.

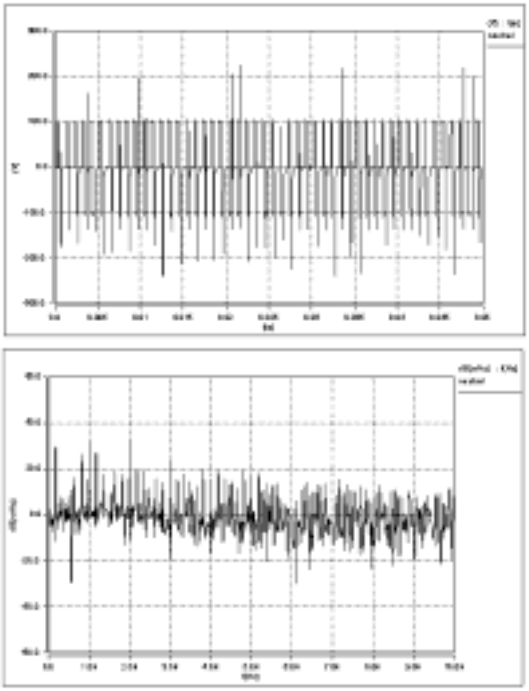


Figure 18. Time and frequency domain waveforms of the neutral voltage with AZSS at M.I. = 0.5 p.u.

A circuit simulation of a three-phase inverter with AZSS was done in Saber. A conventional sinusoidal PWM (f_s = 1 kHz) was used to modulate the active switches in the bridge supplied from 600 V dc bus. The presence of zero states was detected by logic circuitry whereupon, all the active switches in the bridge were opened and the AZSS switches were closed to synthesize zero state. The neutral voltage without and with AZSS at M.I. = 0.5 p.u. is presented in Figures 17-18 which shows the corresponding attenuation with AZSS.

VI. Conclusions

Numerous topological variations and modulation strategies have been reported in the literature to mitigate common mode voltages. A brief review of these techniques has been presented. A new modification to the conventional VSI topology has been proposed in this paper. Adding three switches to the conventional VSI, this Auxiliary Zero State Synthesizer (AZSS) is capable of synthesizing zero state components without generating any common mode voltage at the output. Preliminary simulation results verify the feasibility of the proposed approach and indicate promising results in mitigation of common mode EMI. However an elaborate analysis of the modulation process and the corresponding device ratings is necessary to prove the practicability and will be reported in future.

References

[1] Laszlo Tihanyi, *Electromagnetic Compatibility*, IEEE Press, 1995.

[2] T.A. Lipo, "WEMPEC Experience with EMI", *Tutorial report at WEMPEC Annual Meeting*, University of Wisconsin – Madison, 1997.

[3] G. Skibinski, J. Pankau, R. Sladky, J. Campbell, "Generation, Control and Regulation of EMI from AC Drives," *Conference proceedings of IEEE-IAS Annual Meeting*, 1997, pp. 1571-1583.

[4] D. Leggate, J. Pankau, D. Schlegel, R. Kerkman, G. Skibinski, "Reflected Waves and their Associated Current," *Conference proceedings of IEEE-IAS Annual Meeting*, 1998, pp. 789-798.

[5] S. Chen, T.A. Lipo, D. Fitzgerald, "Modeling of Motor Bearing Currents in PWM Inverter Drives," *Conference proceedings of IEEE-IAS Annual Meeting*, 1995, pp. 388-393.

[6] US Department of Defense, *Measurement of Electromagnetic Interference Characteristics: MIL-STD-462D*, 1993.

[7] CISPR Pub. 22, *Limits and Methods of Measurements of Radio Interference Characteristics of Information Technology Equipment*, 1985.

[8] D. Rendusara and P. Enjeti, "New Inverter Output Filter Configuration Reduces Common Mode and Differential Mode dv/dt at the Motor Terminals in PWM Drive Systems," *Conference record of IEEE-PESC*, 1997, pp. 1269-1275.

[9] S. Ogasawara and H. Akagi, "Modeling and Damping of High Frequency Leakage Currents in PWM Inverter-fed AC Motor Drive Systems," *IEEE Trans. on IA*, Vol. 32, No. 5, 1996, pp. 1105-1114.

[10] S. Ogasawara, H. Ayano, H. Akagi, "An Active Circuit for Cancellation of Common Mode Voltage Generated by a PWM Inverter," *IEEE Trans. on PE*, Vol. 13, No. 5, 1998, pp. 835-841.

[11] A.L. Julian, T.A. Lipo, G. Oriti, "Elimination of Common Mode Voltage in Three Phase Sinusoidal Power Converters", *Conference record of IEEE-PESC*, 1996, pp. 1968-1972.

[12] A.L. Julian, *Active Common Mode Voltage Reduction in Voltage Source Inverters*, Ph. D. Thesis, University of Wisconsin-Madison, 1997.

[13] G. Oriti, A.L. Julian, T.A. Lipo, "A New Space Vector Modulation Strategy for Common Mode Voltage Reduction", *Conference record of IEEE-PESC*, 1997, pp. 1541-1546.

[14] H.W. van der Broeck, H.-Ch. Skudenly, G. Stanke, "Analysis and Realization of a Pulse Width Modulator based on Voltage Space Vectors," *Conference proceedings of IEEE-IAS Annual Meeting*, 1986, pp. 244-251.

[15] A.V.K. Rao, *The Design and Implementation of a Modified Single Phase Inverter Topology with Active Cancellation of Common Mode Voltage*, M.S. Thesis, University of Wisconsin-Madison, 1998.