A Modified Single Phase Inverter Topology with Active Common Mode Voltage Cancellation

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***Abstract* - This paper addresses the problem of common mode EMI reduction in single phase PWM inverters by means of active cancellation. A topological modification which balances the switching pattern of the inverter is made. Common mode voltage, which results chiefly from unbalanced switching is thus significantly attenuated. This attenuation translates into a substantial reduction in the size and cost of passive filtering components needed to comply with conducted EMI standards. The principles of operation and performance of the proposed topology are discussed in this paper.**

I. INTRODUCTION

Switching frequencies of power electronic converters have been on the rise in recent years due to advances in power semiconductor technology. This has led to significant increases in their levels of EMI. A large number of the techniques for conducted EMI reduction rely on the use of passive filtering. The use of these filters, unfortunately, is associated with a significant size, cost and weight penalty. The application of active EMI filtering techniques, however, can significantly reduce their size and cost. This fact, coupled with the steadily falling prices of power semiconductor devices is making their use both attractive and feasible.

In the recent past, active techniques have been applied with considerable success to various power converter topologies [1-4]. The primary objective of active cancellation techniques is to balance the switching pattern of the converter under consideration, thereby attenuating the common mode voltage applied to the load. This is achieved in practice by means of topological modifications and/or alterations in modulation strategy. Active cancellation, therefore, aims to mitigate EMI at its source rather than suppress it by conventional (passive) means [5-7]. Since the mechanism by which common mode EMI is generated by power electronic converters varies with topology and modulation strategy, it follows that no single topological modification can be prescribed as a solution that encompasses all switching power converters. A fairly detailed analysis of the operation of a given power converter topology must therefore be carried out in order to arrive at a practical and cost effective solution.

This work addresses the problem of conducted EMI in single phase PWM inverters. A topological modification for common mode voltage cancellation is proposed. Two additional switching devices (configured to form a single bi-directional device) augment the conventional topology. These devices and a carefully considered commutation strategy significantly attenuate common mode voltage applied to the load without affecting the differential mode performance of the inverter in any way. The remarkable improvement in EMC performance of a laboratory prototype inverter incorporating the modified topology establishes the efficacy of this technique.

The cost benefit (in the form of a cheaper EMI filter) resulting from the superior common mode performance of the proposed topology must be weighed against the cost of the additional switching devices in order to establish its relative economic merit. However, as the cost of solid state devices continues to diminish this active cancellation approach becomes increasingly attractive.

II. OPERATION OF MODIFIED SINGLE PHASE INVERTER

A schematic diagram of the proposed single phase topology driving a passive load is presented in Fig. 1 below. It is seen that it differs from the conventional topology on account of switches S5 and S6, which together form a bi-directional device. The load is coupled to ground through a parasitic capacitance which causes undesirable common mode emissions due to the high frequency excitation impressed upon it by the inverter [8]. It is the goal of the proposed topology to significantly attenuate these emissions.

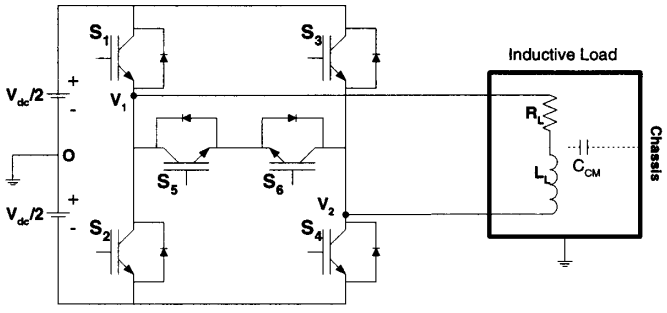


Fig. 1. Schematic diagram of modified single phase topology.

A. Common Mode Voltage

The common mode voltage applied to the load at any instant by a single phase inverter with pole voltages V_1 and V_2 is given by [9,10]:

$$V_{cm} = \frac{V_1 + V_2}{2} \quad (1)$$

From (1) it is clear that a common mode voltage would be applied to the load if and only if switches S1,S3 or S2,S4 are turned on (see Fig. 1). It follows therefore that in the absence of switches S5,S6, i.e. in the case of the conventional topology, a common mode voltage is applied to the load during freewheeling or "zero" states alone. In the case of the proposed topology, however, the zero state is implemented by turning on the freewheeling device pair (S5,S6). Thus, provided that devices S1 through S4 share voltage equally in the off state, the common mode voltage applied to the load by the proposed topology is identically zero.

It is apparent from the above discussion that the proposed topology allows exactly three inverter switching states. Two of these states (namely S1,S4 ON and S2,S3 ON) are "active" while the third (S5,S6 ON) is a "zero" state. These states are identical in terms of their (differential mode) effect on the load to the four switching states of the conventional topology. The differential mode characteristics of the proposed topology are therefore virtually identical to those of the conventional topology [11].

B. Commutation Strategy

The differential mode performance of the proposed topology is dependant to a large extent upon the manner in which current is commutated into and out of the freewheeling device pair S5,S6.

Clearly, shoot through and destruction of switching devices can result if the freewheeling device pair is turned on simultaneously with an active device pair (S1,S4 or S2,S3). A suitable commutation strategy must therefore be devised to allow a safe transition to and from active switching states.

One possible strategy is to turn off the active device pair, wait for a suitable blanking time and subsequently turn on the freewheeling device pair. This strategy, although robust, has a serious drawback. Consider the operation of the inverter during the positive half cycle of the fundamental output voltage. With the output voltage being defined as V_1 - V_2 (see Fig. 1), the active device pair is S1,S4. For practical loads the output current will not flow through the freewheeling diodes of the device pair for much of the half cycle. When these devices are turned off to initiate commutation to the zero state, the load current will continue to flow through switches S2 and S4 until the freewheeling device pair S5,S6 is turned on. For the blanking time interval therefore, the load voltage polarity will reverse. This phenomenon, which will be observed even during the negative half cycle, constitutes a loss of volt seconds and can inject significant low order harmonics into the load current. It can also be regarded as a source of differential mode emissions. The performance degradation caused by this commutation strategy is entirely unacceptable.

The problems posed by the above commutation strategy can be largely obviated by employing a (fundamental output voltage) polarity sensitive technique. It is apparent upon some reflection that the switch S6 may be safely turned on throughout the positive half cycle of the fundamental output voltage (defined as V_1 - V_2), leaving S5 to perform the voltage blocking function (see Fig. 1). Transitions to the zero state are therefore accomplished by turning off devices S1 and S4, allowing the blanking time interval to elapse, and then turning on switch S5. Transitions from the zero state may be carried out in the reverse order. Further, during the negative half cycle, the roles of switches S5 and S6 may be reversed. It is clear that this commutation technique eliminates voltage polarity reversal and makes the differential mode performance of the modified topology virtually identical to that of the conventional topology.

The conclusions drawn above were substantiated by laboratory testing of the prototype inverter.

C. Device Voltage and Current Ratings

An analysis of the ratings of the switching devices used to realize the modified topology is of considerable importance both from the technical and economic standpoints.

By inspection, the peak voltage ratings of each of the switching devices S1 through S6 must be identical. It is also apparent that these ratings must be identical to those of an equally rated inverter incorporating the conventional topology.

The r.m.s. and average currents carried by each of the switching devices were analytically calculated (it was assumed that the switching frequency is far greater than the fundamental output frequency). These ratings are compared with those of an equally rated conventional inverter in Table I, at a modulation index and load power factor approaching unity. The load current is assumed to be sinusoidal with a peak value I_m.

TABLE I
DEVICE CURRENT RATINGS AT MOD. INDEX→1, P.F. →1

Device	Conventional Topology			Proposed Topology		
	Peak	RMS	Avg.	Peak	RMS	Avg.
S1	I_m	0.5 I_m	0.31 I_m	I_m	0.46 I_m	0.25 I_m
S2	I_m	0.5 I_m	0.31 I_m	I_m	0.46 I_m	0.25 I_m
S3	I_m	0.5 I_m	0.31 I_m	I_m	0.46 I_m	0.25 I_m
S4	I_m	0.5 I_m	0.31 I_m	I_m	0.46 I_m	0.25 I_m
S5	N/A			I_m	0.27 I_m	0.13 I_m
S6				I_m	0.27 I_m	0.13 I_m

Table I shows that the peak current ratings of the freewheeling switches (S5,S6) of the proposed topology are equal to those of all other inverter switches. However, their r.m.s. and average current ratings are far lower than those of the main switches. Depending upon the type of devices chosen to implement the inverter, this could result in the choice of lower rated and consequently relatively inexpensive devices to implement them.

It is interesting to note that the aggregate r.m.s. and average current ratings of the inverter switches for both topologies are identically equal for a given load current. This is true irrespective of operating point. It merely reflects the fact that exactly two switching devices carry the load current at any given time, irrespective of topology. The change of topology, therefore, merely redistributes the current among the inverter switches. The aggregate peak current rating of the proposed topology, however, is 1.5 times that of the conventional topology due to the two additional switching devices.

III. Experimental Results

A prototype inverter incorporating the conventional and proposed single phase inverter topologies was designed, developed and tested. The two topologies were compared under identical conditions so as to precisely determine their relative merits. The inverter was rated at 1.25 kW, with a DC bus voltage of 150 V. The PWM frequency was chosen to be 21.0 kHz. The modulation strategy for the conventional topology was unipolar sinusoidal PWM with equal device loading. The modified topology was modulated as discussed in the preceding section.

A. Device Voltage Sharing

It is clear that the effectiveness of the proposed topology in attenuating common mode emissions is dependant to a large extent upon the off state voltage sharing of devices S1 through S4. It has been found that this is unsatisfactory for practical switching devices. As a result, snubber capacitances need to be added across each of the devices S1 through S4. The magnitudes of these capacitances need only be large enough to swamp out device capacitance inequalities. Snubber capacitances also serve to equalize switching dv/dt's. A value of 10 nF was found to be quite satisfactory for the laboratory prototype. The snubber capacitances were directly connected across the switching devices as shown in Fig. 2.

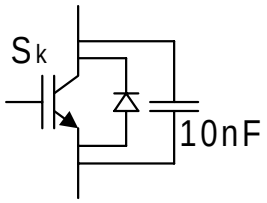


Fig. 2. Snubber configuration of laboratory prototype inverter.

Such a configuration, although not a preferred embodiment, was found to be satisfactory in the case of the laboratory prototype due to the rating of the switching devices used and the relatively small value of capacitance. A conventional discharge current limiting topology could have been employed just as easily. The choice of snubber topology, however, has virtually no bearing on the operation of the inverter.

B. Inverter Operation

Experimental load voltage and current waveforms for the conventional and proposed topologies are presented in Fig. 3 and Fig. 4 respectively. It is apparent from the figures that the differential mode performance of the two topologies is virtually indistinguishable.

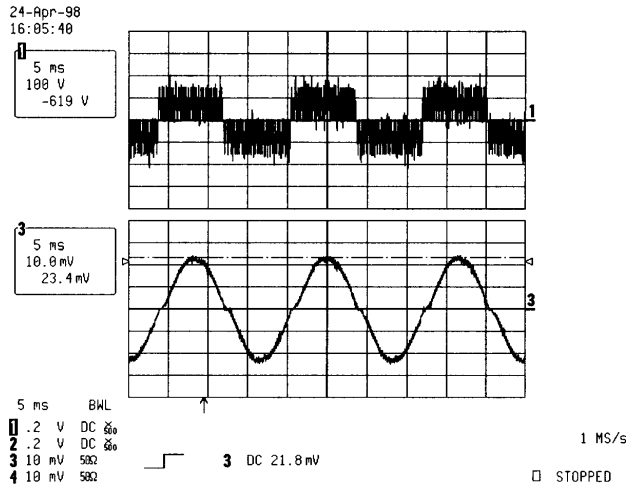


Fig. 3. Load voltage and current waveforms for conventional topology. (a) Upper trace: Voltage (100V/Div) (b) Lower trace: Current (10A/Div).

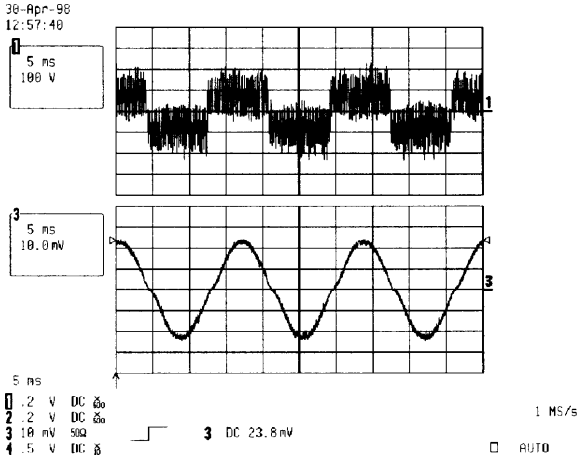
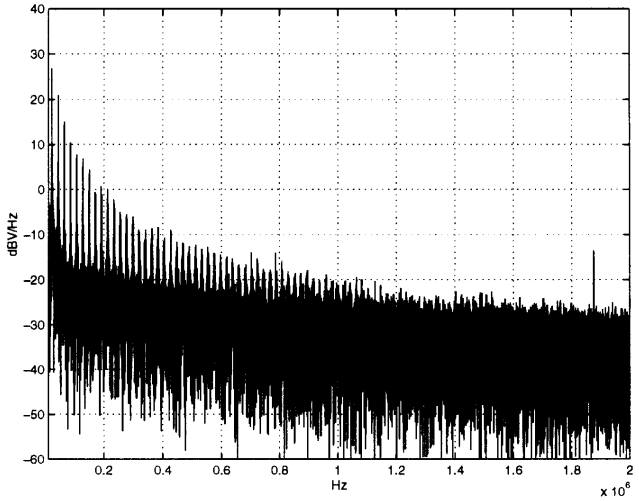


Fig. 4. Load voltage and current waveforms for proposed topology. (a) Upper trace: Voltage (100V/Div) (b) Lower trace: Current (10A/Div).

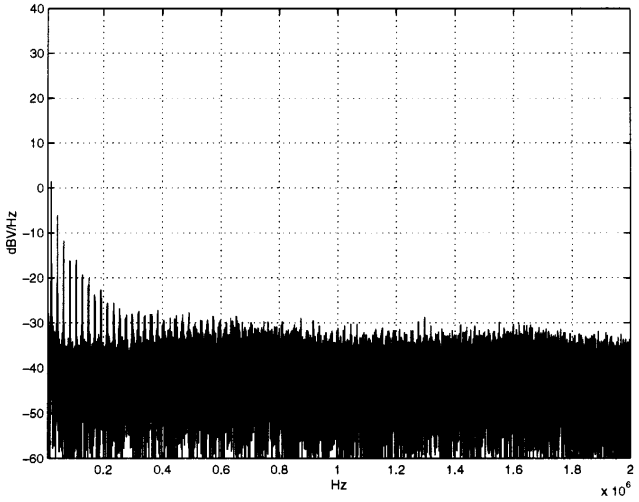
C. Common Mode Voltage

The common mode voltage applied to the load was measured with respect to the mid-point of the DC bus of the prototype inverter.

The frequency spectra of the common mode voltage applied to the load by the two topologies (10 kHz to 2 MHz) are shown in Fig. 5. The modified topology is seen to attenuate the common mode load voltage by up to 27 dBV. The considerable superiority of the proposed topology is demonstrated by these results.



(a)

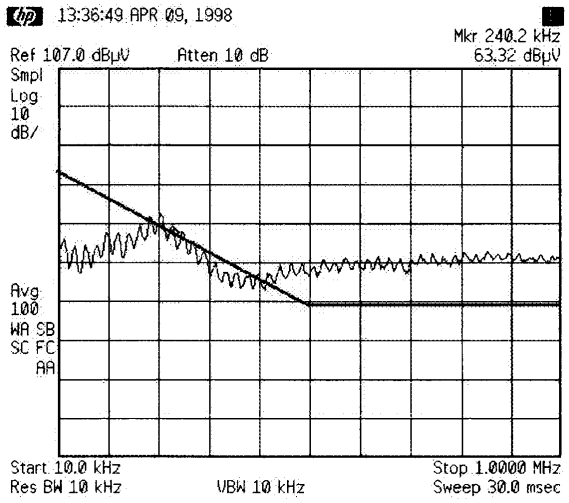


(b)

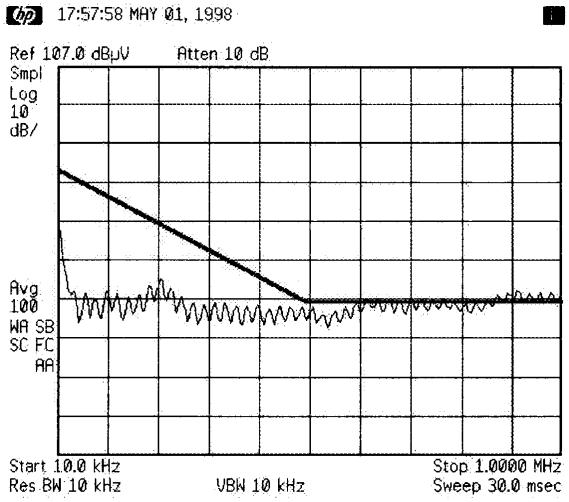
Fig. 5. Common mode load voltage spectra (10 kHz to 2 MHz).
(a) Conventional topology (b) Proposed topology.

D. Conducted Emissions Test Results

The frequency spectra of conducted emissions generated by the two topologies were measured at the terminals of a LISN (line impedance stabilization network) connected to the three phase input power cords. The AC power cords of the control circuit and gate drive power supplies were not connected through the LISN's. This was done to isolate the conducted emissions generated by the power devices. Conducted emissions spectra were sample detected and video averaged. Measurements were made from 10 kHz to 10 MHz. The emissions spectra (10 kHz to 1 MHz) generated by the two topologies are illustrated in Fig. 6 (the solid lines represent CE-102 requirements). The proposed topology is seen to provide an attenuation of up to 20 dBμV.



(a)



(b)

Fig. 6. Conducted emissions spectra (10 kHz to 1 MHz).
(a) Conventional topology (b) Proposed topology.

IV. CONCLUSIONS

A modified single phase inverter topology has been introduced for the purposes of reducing conducted EMI. The proposed single phase inverter topology introduces an additional bi-directional switch (to the conventional topology) which allows the choice of the zero state without necessitating unbalanced switching. A prototype inverter incorporating this topology was determined to perform very satisfactorily. The differential mode performance of the proposed topology was seen to be indistinguishable from the conventional topology. Total inverter losses (switching + conduction) were estimated to be 6 % higher for the proposed topology. The common mode voltage applied to the load was attenuated by up to 27 dBV by the proposed topology. The conducted emissions (measured across a LISN) were attenuated by up to 20 dBμV.

The large attenuation in common mode voltage resulting from the proposed topology translates into a substantially cheaper and smaller EMI filter needed to meet regulatory specifications. This benefit, of course, must be traded off against the cost of the additional switching devices needed to effect the desired topological modification. However, as power semiconductor devices become cheaper such active cancellation techniques are expected to become increasingly attractive.

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