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Switching Angles and DC Link Voltages Optimization for Multilevel Cascade Inverters

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The optimization of both DC link voltages and switching angles of fundamental switching strategy for the output waveform of a multilevel cascade inverter is investigated in this study. Previous work in the area of fundamental switching for multilevel inverters is highlighted by the pulse width optimization technique, where the switching angle at each voltage level is optimized so that the resulting staircase output voltage has the minimum harmonic content. The DC link voltage of each level, however, is assumed to be the same and constant. As an extension to this work, the optimization of both DC link voltages and switching angles of the staircase output voltage is carried out. Harmonic performance of the proposed switching strategy is simulated and results are compared with that of the previous work. It is confirmed theoretically that substantial improvement in the harmonic minimization can be obtained.

In practice, the proposed method is especially suitable for the control of multilevel cascade inverters, the latest development of its kind, where each DC voltage can be self-maintained and independently controlled. The description of the multilevel cascade inverters for applications of AC drives, as well as Static Var Generation, is also given in this article.

1 Introduction

Semiconductor switch ratings and problems concerned with series connection of these switches have limited the development of high-power inverters. This limitation can be overcome by the multilevel structure for the voltage source inverter [1–3]. The concept of multilevel inverter drives was introduced by Bhagwat and Stefanovic [1] in 1983. The structure, being based on the Neutral Point Clamped

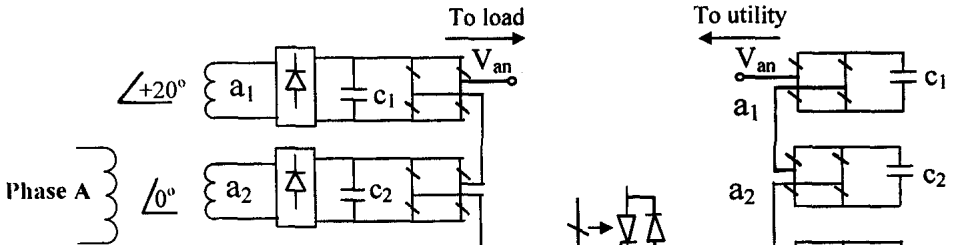
level inverters become difficult to control. In this case, the topology using modular H-bridges in a cascade connection has been preferred [3,4], where the generation of M-level voltage waveforms can easily be produced by cascading (M-1)/2 H-bridges. Such extension is much more difficult in the case of NPC-type multilevel inverters.

The applications of the multilevel cascade inverter to AC drives and static VAR generation have the same circuit configuration for the inverter portion; however, the interfaces of the portion with the utility differ from each other, as is the case for the three-level system of a single unit. Figure 1 shows the single-phase configuration of the two applications for a seven-level voltage source cascade inverter. In Figure 1(a), the cascade inverter is used as AC drives [3,5], and each H-bridge is powered by an isolated secondary winding of an integral isolation transformer, which are wound to obtain a phase angle difference by multiples of 20° for 3 H bridges in cascade. In this manner, the harmonic cancellation between the reflected secondary current is caused to produce an 18-pulse primary current. The lowest harmonic that is not cancelled is the 17th.

In the case of using cascade inverter for static VAR generation [4], the H-bridge is directly connected to the utility, from which the DC source of each H-bridge is supplied as shown in Figure 1(b). The regulation of the DC link voltage is closely related to the operation of the inverter. This arrangement is different from the structure of Figure 1(a), where the DC source is supplied via the rectifier and is independent from the operation of the inverter. This difference must be taken into account in the control of the cascade inverter.

The cascade inverter appears to be superior to other multilevel structure inverters in applications at higher power ratings. When such applications are considered, most of them do not require too high a dynamic response, but an excellent harmonic performance is a necessity for cleaner power, high efficiency, and less electromagnetic interference. The suitable switching strategies are those based on the fundamental frequency switching with minimum weighted total harmonic distortion (WTHD). The fundamental frequency switching requires each device to be switched on and off just once per cycle of the fundamental frequency output.

Previous work in the area of fundamental switching for multilevel cascade inverter is highlighted by the pulse width optimization technique proposed in [4], where the switching angle of each H-bridge is optimized so that the resulting stair-



case output voltage has the minimum harmonic content, whereas the DC link voltage at each level is assumed to be the same and constant.

As an extension to this work, the optimization of both DC link voltages and switching angles of the output waveform is investigated in this paper. With the addition of one more degree of freedom in the optimization, harmonic minimization is demonstrated to be substantially improved.

2 Review of Switching Strategies for the Cascade Inverter

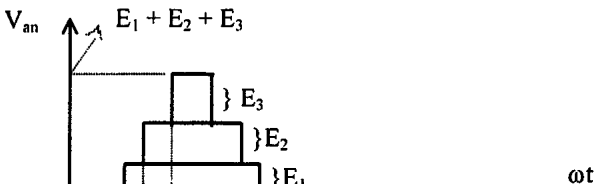
Most switching strategies applied to control a single H-bridge inverter are ready to be extended to a multilevel cascade inverter with certain modifications to take the full advantage of the multilevel structure. The selection of specific switching strategy depends on given performance specifications. To achieve high-dynamic response, the hysteresis band current control method and the sine PWM technique for a multilevel structure were proposed in [3,5]. If the minimum harmonic content in the output voltage is a main concern, then switching at the fundamental frequency with switching angle optimization at each voltage level is preferred [4]. The latter is exclusive to the multilevel structure, where the access to each level of the DC voltages is possible. In [4] each DC voltage was maintained at the same level, E_d, while the switching angle of each bridge is optimized for minimum harmonic distortion of the output waveform.

To take the full advantage of the separate control of DC link voltages of the cascade inverter, the optimizations of both DC voltages and switching angles are explored in this paper. When both the pulse height and the pulse width are optimized, harmonic performance is greatly enhanced.

A case study approach is taken to investigate this technique, where the seven-level cascade inverter of Figure 1 is used as an example. In Figure 1, each H-bridge has its own DC source E_1, E_2, and E_3, respectively, and is isolated from one another. If each H-bridge is to be switched to E_1 at α_1, E_2 at α_2, and E_3 at α_3, respectively, the output waveform produced is the staircase-type as shown in Figure 2 for phase a, V_{an}. The outputs of phase b and c are 120° phase shift from V_{an}. The Fourier coefficients of the output voltage are calculated as the simple sum of the coefficients of the three rectangular waves:

$$H(n) = \frac{4}{\pi n}[E_1 \cos(n\alpha_1) + E_2 \cos(n\alpha_2) + E_3 \cos(n\alpha_3)], \tag{1}$$

where $n = 1, 3, 5, 7, \ldots$.



From equation (1) one can derive two control options for the output voltage:

1. The DC voltages E_i's remain constant at a same level, $E_1 = E_2 = E_3 = E_d$, and angles α_i varied to control the fundamental voltage as proposed in [4].
2. The angles α_i remain constant at their optimal values, whereas the DC voltage steps are varied to control the fundamental component of the output voltage, as proposed in this paper.

The first and second methods are hereafter referred to as option 1 and option 2, respectively, in the following sections.

3 Option 1 Technique

Option 1 is the pulse width control at a constant DC voltage E_d. The fundamental output voltage, $H(1)$, is controlled by switching angles that can be optimized by eliminating the lowest harmonics while achieving the target fundamental voltage output. Different cost functions are required for the optimization, depending on the modulation index concerned. If the modulation index, M, is defined as the ratio of $H(1)$ or V_{com}, to that of the six-step output, having a voltage level of $3E_d$ and a zero switching angle, then we have

$$M = V_{com} \Big/ \left(3E_d \frac{4}{\pi}\right), \tag{2}$$

where V_{com} is the voltage command.

To optimize switching angles α_1, α_2, and α_3 at $M = M_{\max}$, the cost function, f_{cost}, is defined as

$$f_{\cos t} = \begin{cases} H(5) = 0 \\ H(7) = 0 \\ H(11) = 0 \end{cases} \quad \text{for } M = M_{\max}. \tag{3}$$

It can be seen that the 5th, 7th, and 11th harmonics are eliminated in this case. Solving equation (3) for α_1, α_2, and α_3, and calculating $H(1)$ in terms of (1), $M_{\max} = 0.92$ can be obtained by substituting resulting $H(1)$ into equation (2). This implies that with these constraints the maximum fundamental voltage output attainable is 92% of the six-step output voltage.

For other values of $M(0 < M < M_{\max})$, the cost function differs from equation (3) in that the target fundamental voltage, $H(1)$, has to be defined in the cost function, and leave only the 5th and 7th harmonics to be eliminated as given in (4):

$$f_{\cos t} = \begin{cases} H(1) - \dfrac{12}{\pi} E_d \times M = 0 \\ H(5) = 0 \\ H(7) = 0 \end{cases} \quad \text{for } 0 < M < M_{\max}. \tag{4}$$

height of the output voltage, can be optimized. To proceed with the DC voltage optimization, it is useful to define

$$\begin{aligned} E_1 &= E_d, \\ E_2 &= E_d + \Delta e_1, \\ E_3 &= E_d + \Delta e_2, \end{aligned} \tag{5}$$

where Δe_i represents the voltage incremental portion of E_d.

It is convenient to introduce the per-unit value approach into the DC voltage optimization by normalizing variables in equation (5) to E_d; thus E_d is equal to one, and Δe_1 and Δe_2 are per-unit values. Now substituting equation (5) into equation (1), the Fourier coefficients of the output voltage is rewritten:

$$H(n) = \frac{4}{\pi n}\{E_d[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] + \Delta e_1 \cos(n\alpha_2) + \Delta e_2 \cos(n\alpha_3)\}. \tag{6}$$

It can be seen in equation (6) that with the introduction of the voltage increments Δe_1 and Δe_2, the number of variables to be optimized are increased to 5, including the three switching angles α_i. Harmonics up to the 17th can be eliminated in the cost function of option 2:

$$f_{\cos t} = \begin{cases} H(5) = 0 \\ H(7) = 0 \\ H(11) = 0 \\ H(13) = 0 \\ H(17) = 0 \end{cases}. \tag{7}$$

Substituting equation (6) into equation (7) and solving the five equations for the five unknowns in equation (7) yields optimal values of Δe_1, Δe_2, α_1, α_2, and α_3. Once the optimal values are found, they should be kept constant over the entire modulation range to maintain the best harmonic performance. The amplitude of the fundamental component of the output waveform can be controlled by the variation of the nominal DC link voltage E_d to control E_1, E_2, and E_3, as defined in equation (5):

$$E_d = \frac{V_{com}\pi}{4k} \tag{8}$$

Where k is a constant after optimization and determined by the five optimal values:

$$k = \cos\alpha_1 + (1 + \Delta e_1)\cos\alpha_2 + (1 + \Delta e_2)\cos\alpha_3. \tag{9}$$

If the modulation index defined in equation (2) is used, then $M_{\quad} = k/3$ can be

5 Harmonic Analysis

To measure the harmonic performance of option 1 and 2 for purpose of comparison, the weighted THD (WTHD), which evaluates harmonics in the line current into an inductive load, was chosen as criteria. The WHTD is defined in equation (11) as the rms value of the harmonic voltages (line-to-line) normalized to the maximum fundamental voltage and divided by the harmonic number, n. For fundamental switching, harmonic numbers up to $n = 50$ is used in this study and is found to be adequate:

$$WTHD = \frac{\sqrt{\sum_{i=2}^{n} \left(\frac{V_i}{i}\right)^2}}{V_1}, \tag{11}$$

where V_i is the harmonic components of the switched line voltage obtained by subtracting the switching phase voltages from each other. The phase leg output voltages can be formed by optimal values of DC voltages and switching angles, as shown in Figure 2.

The digital solution for the WTHD in equation (11) was obtained using the FFT capability of the MatLab package to analyze the simulated switched line voltage waveform, $V_{ab}(.)$. The MatLab solution is an accurate representation of a real inverter output under the same modulation conditions, with the exclusion of crossover delay effects; however, this simplification involved in neglected crossover delay does not affect the conclusions of this paper. The following tasks have been performed in the digital simulation:

1. Invoke the optimization process
2. Generate the waveform of inverter output line voltage
3. Perform a harmonic analysis of the line voltage

The simulation results are given in the following section.

6 Digital Simulation Results

Simulation results of a seven-level cascade inverter, including optimal values of switching angle and voltage increment, as well as the WTHD for options 1 and 2, respectively, are summarized in Table 1. The corresponding values for the six-step switching technique are included for comparison. The switched line voltage of the inverter under option 2 switching is depicted in Figure 3.

Table 1
Simulation results for a seven-level cascade inverter

				WTHD

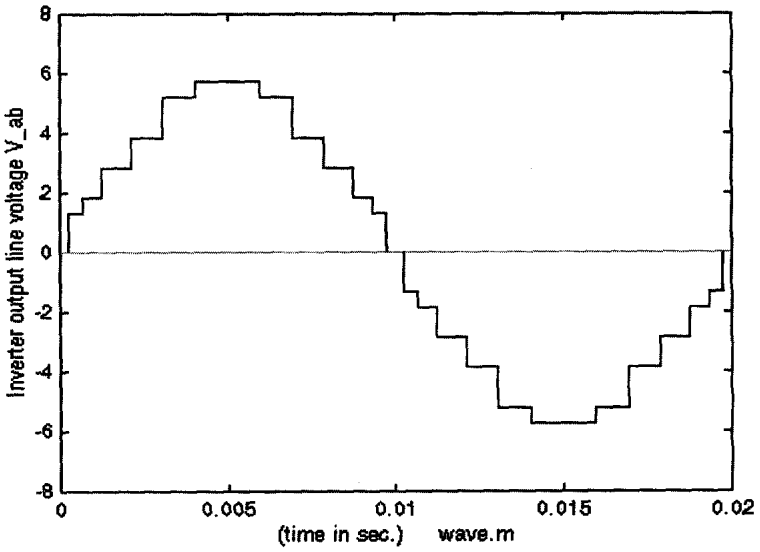


Figure 3. Inverter output line voltage V_{ab} (seven-level).

To summarize the characteristics of option 2:

1. In the cases of option 1 and six-step switching, there is $E_1 = E_2 = E_3 = E_d$ (i.e., the DC voltage sum is $3E_d$), based on which the $M_{\max}$ values of Table 1 are calculated. In fact, the DC voltage sum of option 2 is 2.86 E_d, for $E_1 = E_d$, $E_2 = 1.33\ E_d$, and $E_3 = 0.53\ E_d$, respectively. Therefore, the nominal value of E_d is increased by 1.049 in the calculation of $M_{\max}$ for option 2, as $2.86(1.049\ E_d) = 3\ E_d$.
2. The limit of $M_{\max}$ of option 2 depends on that of E_i, (i =1,2,3), or $E_{d\_\max}$.
3. For the seven-level structure, WTHD is 22% reduced from that of option 1 at $M = M_{\max}$.

Digital simulation is also performed for a five-level cascade inverter for comparison, and results of both options 1 and 2 are given in Table 2.

It can be seen in Table 2 that if the option 2 switching strategy is implemented, the DC voltage ratio for the five-level cascade inverter is 1:1.734, and WTHD is 40% reduced from that of option 1. Comparing with the DC voltage ratio of 1:1.33:0.53 and 20% WTHD reduction in the case of the seven-level structure, the result indicates that DC voltages and harmonic differences between options 1 and 2 decrease with the increased number of levels. It is therefore expected that for levels higher than 11 (i.e., a total 5 H-bridges per phase in series connection), the WTHD of

Table 2

option 2 would approach that of option 1. Eventually, the switched waveform of option 2 would approach that of option 1.

7 Conclusion

In this paper, the effect of DC voltage optimizations on the WTHD performance of the fundamental switching strategy is investigated. Results of digital simulation are presented and compared with those of the switching angle optimization alone and the six-step switching technique. It is confirmed theoretically that the harmonic distortion of option 2 is significantly reduced from that of option 1 for five- and seven-level structure. For levels higher than 7, the difference between the two options become marginal.

The proposed method is especially suitable for the control of multilevel cascade inverters, where independent control of DC voltage is possible. In practice, the DC voltage control of AC drives is quite different from that of Static Var Generation due to the different circuit topology (Figs. 1(a) and (b)). The former requires the regulation of the integral transformer's output to control the DC link voltage, whereas in the latter, the DC capacitor voltage can be directly controlled by the switching strategy. It is therefore recommended that the best application of the option 2 technique for AC drives is under a constant load condition, when the DC link voltages can be fixed at their optimized values, and no on-line regulation of E_i is required. Thus, the implementation of option 2 is simplified to option 1 while a better harmonic performance is achieved.

As for the Static Var Generation, the DC capacitor voltage of each H-bridge can be independently controlled by asymmetrical positioning of the on-pulse of the gating signal over a half-wave period accordingly [4]. This can be easily performed on-line. Considering the design aspects, with different DC voltages in operation, capacitance of the DC capacitors should be designed separately to match their voltage ratings. Also, different voltage rating and thermal capability of the converter switches need to be taken into account in the design of each H-bridge.

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