A New Multilevel Inverter Topology with a Hybrid Approach

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Abstract **-** This paper presents some novel cascade multilevel inverter approach for high voltage and high power inverter applications. It is based on the series connection of the half and full bridge inverter cells. With the conventional cascade H-bridge multilevel inverters composed of the only full bridge inverter cells, an even-level system can not be obtained, which may cause some limitation in selecting the switching devices and the number of inverter levels regarding maximum inverter output voltage magnitude. The proposed configuration allows any kinds of even-level inverters leading to utilizing all of the levels like the diode-clamped multilevel inverter circuit, having inherent advantages of the cascade H-bridge inverters. Structural and operational characteristics are discussed and also an effective carrierwave-based space vector PWM scheme is given for ac drive applications. Validity of the proposed circuit and effectiveness of the PWM method are verified by some simulation and experimental results.

Keywords – Cascade multilevel inverter, Space vector-based PWM, High voltage inverter

Introduction

High power and high voltage conversion systems have become very important issues for the power electronic industry handling the large ac drive and electrical power transmission applications. In particular, multilevel inverters for adjustable speed drive applications not only effectively reduce harmonics and EMI problems, but also avoid possible high frequency switching dv/dt induced motor failure [1]-[2]. Therefore, in recent years, the use of multilevel inverters to realize the systems is widely spread and well-understood. There are roughly three different types of multilevel inverter topologies, which have been studied and received considerable interest from high power inverter system manufacturers. The detailed overview and comparison of characteristics, and their implementation issues are given in [1]-[5].

Of those inverters, it would be noted that the cascade H-bridge multilevel inverter has the

simplest and easiest structure from practical manufacturing point of view and offers very attractive extension toward higher levels resulting in higher voltage and higher power capability [4]-[7]. One of the disadvantages of the cascade inverter is that an even-level inverter can not be obtained. Design of high voltage multilevel inverter system needs that both the voltage rating of the power devices and the number of levels of the inverters should be taken into account simultaneously. Therefore, there would be some constraint in determining the voltage rating of the devices and the number of the inverter levels for a specific application. The IGBT inverter systems requiring 3.3kV ac output voltage, that is, above dc-link voltage of 4700V can be considered as an example. The breakdown voltage rating of the highest voltage IGBT module available on the market now is 3.3kV. But it should be noted that its guaranteed continuous blocking voltage is lower than 1800V. In the case of the application, 3-level structure can not be applied and 5-level inverter will result in a lot of over-specification from design point of view. 4-level inverter circuit would be most suitable for the system with the use of 3.3kV-IGBT module.

Thus this paper proposes an new approach for the cascade multilevel inverter topology on the basis of the series connection of half and full bridge inverter, which allows one to achieve any kinds of even-level topology while having the inherent advantages of the cascade inverter compared to other types of multilevel structure. Structural and operational characteristics are discussed and also an effective carrierwave-based space vector PWM scheme is given for ac drive applications. Validity of the proposed circuit and effectiveness of the PWM method are verified by some simulation and experimental results.

A New Approach to the Cascade Multilevel Inverter

Conventional Cascade Multilevel Inverter

Fig. 1 shows schematic of a single phase, consists of two inverter legs, of conventional cascade 5-level inverter using IGBTs connected in series to form each H-bridge (full bridge) cell of the multilevel inverter. In this approach, a number of full bridge single phase inverters with dedicated isolated dc bus capacitors/voltage sources are connected together in series to form a high voltage inverter for each phase of the system [4]. It may be seen that a leg of the inverter is capable of synthesizing five distinct voltage levels (±2Vd, ±Vd, 0) and then output voltage of the single phase will be possible to synthesize stepped waveforms with nine voltage levels viz. ±4Vd, ±3Vd, ±2Vd, ±Vd, 0 if all the dc bus voltages are equal to Vd. The remaining one phase for three-phase inverter has the same switch configuration and respective independent dc voltage source. The output line-to-line voltage waveform becomes the same as the single phase one. The advantage of this topology is that it provides flexibility for expansion of the number of levels easily without introducing undue complexity in the power circuit. Moreover, it requires same number of switches as in diode-clamped topology to achieve a given number of (odd) voltage levels. However this configuration can not provide even-level inverter in contrast to the diode-clamped structure.

New Type of Cascade multilevel Inverter

Structure and Operation Principle

As mentioned in the last section, conventional cascade inverter can have only odd-level characteristics owing to the combination of full bridge cells. Figs. 2(a) and (b) show the structure of one leg and a single phase for the cascade 4-level inverter respectively as an example of the proposed cascade topology. From Fig. 2(a), it can be seen that the new approach for cascade inverter is based on the series connection of half and full bridge inverter cells. Fig. 3 is schematic for new three-phase 4-level inverter resulting in the combination of three full bridge inverters and one three-phase two inverter. This approach also offers numerous advantages like modularity, least number of switches for a given number of levels, simple capacitor voltage balancing etc of the conventional cascade multilevel inverters compared to the diode-clamped type.

Table I shows the possible switching states and the corresponding inverter voltage, Vao for the 4-level inverter shown in Fig. 2(a). There are two redundant switching states for voltage levels, Vd and 0, and total number of redundant states is four. Fig. 4 shows the operation principle of the proposed circuit regarding each switching state shown in Table I with bi-directional current flow.

Fig. 5 is Pspice simulation result for the three phase 4-level inverter shown in Fig. 3. It explains the validity of the developed circuit. From Figs. 5(a) and (b), it can be observed that the line-to-line voltage of seven levels, ±3Vd, ±2Vd, ±Vd, 0 are obtained like the generalized diode-clamped 4-level inverter case. Fig. 5(c) is the phase voltage of the load, Vbn, which has the voltage waveform of eight levels. Asymmetrical inverter leg voltage Vbo, which is the general characteristics of even-level inverters, is shown in Fig. 5(d).

An Effective Space Vector Modulation Method

Fig. 6 shows the proposed disposition of the triangular carrier waves and the principle of the PWM generation for the 4-level inverter, which is corresponding to the switching states of Table I. Subscripts represent different switch states, that is redundancy of the available switching, is capable of obtaining the same phase voltage level. We can see how the redundant switching states are selected. This PWM algorithm allows the current flow through each switch to be equal due to the optimal utilization of the redundant states. The detailed analysis and performance are given in [8]

Simulation and Experimental Verification

The simulation has been performed by using Matlab Simulink power blockset. Three kinds of modulation index for the PWM generation and R-L load to generate the output current were applied to see the three-phase 4-level inverter operation. Figs. 7(a), (b) and (c) show the output currents and line-to-line voltages at each modulation index. We can see 2-, 3-, 4-level inverter operations corresponding to each PWM index. Fig. 7(d) is the line-to-line and inverter leg voltage waveforms

under the condition of 4-level mode. That means high modulation case.

Figs. 8 shows experimental waveforms corresponding to the each simulation result shown in Fig. 7. It may be seen that the proposed circuit and PWM method will be able to have good effectiveness and performance.

Conclusions

Due to the simple and easy design characteristics, it may be expected that the application area of the cascade multilevel inverter can be widely extended for higher voltage and higher power converters. There is some limitation point in designing the inverter about determining the power switching devices and the number of the inverter levels because even-level topology can not be obtained. In this paper, in order to overcome the constraint, some novel cascade multilevel inverter structure was presented on the basis of the series connection of half and full bridge inverter cells. It shall be called hybrid cascade multilevel inverter in the case of the application requiring the use of the even-level cascade inverter.

References

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Table I. The relation between the switching states and the inverter leg voltages (V_{ao}).

Switches / Switching States Notation	A1	A2	A3	A4	A5	A6	V_{ao}
3	OFF	ON	ON	OFF	ON	OFF	2 V_d
2_1	OFF	OFF	ON	ON	ON	OFF	V_d
2_2	ON	ON	OFF	OFF	ON	OFF	
2_3	OFF	ON	ON	OFF	OFF	ON	
1_1	ON	OFF	OFF	ON	ON	OFF	0
1_2	ON	ON	OFF	OFF	OFF	ON	
1_3	OFF	OFF	ON	ON	OFF	ON	
0	ON	OFF	OFF	ON	OFF	ON	- V_d

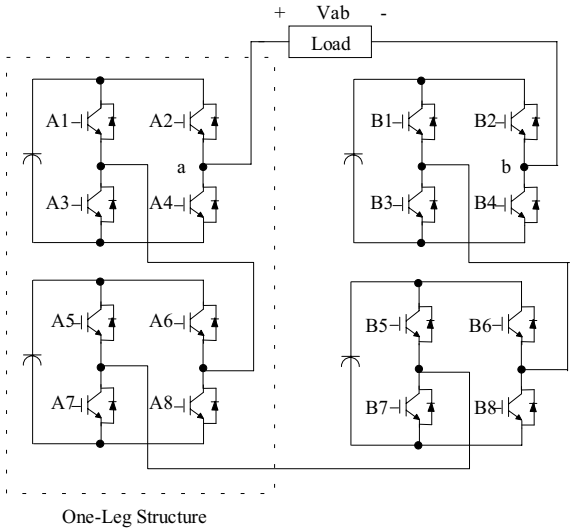
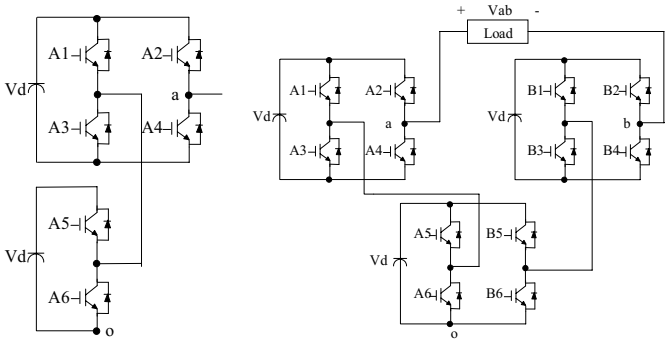


Fig. 1: Schematic of a single phase of conventional cascade 5-level inverter.



(a) a leg (b) a single phase

Fig. 2: The proposed 4-level inverter structure.

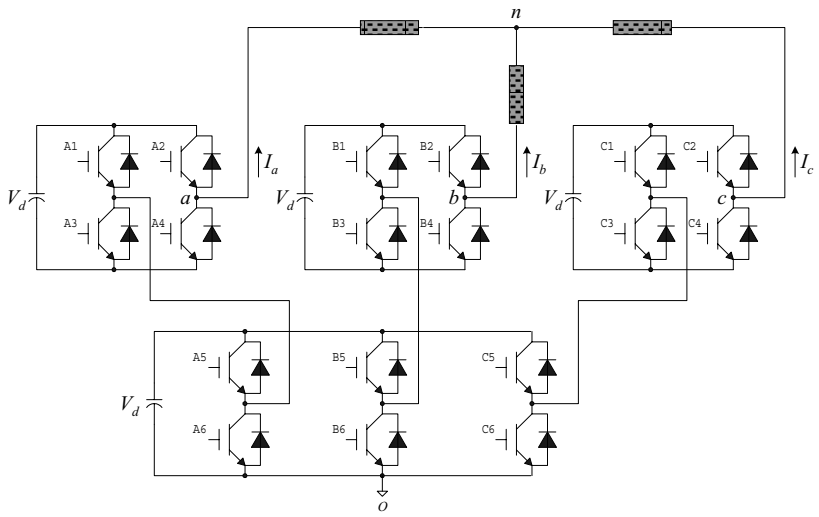


Fig. 3: The proposed three-phase 4-level inverter circuit.

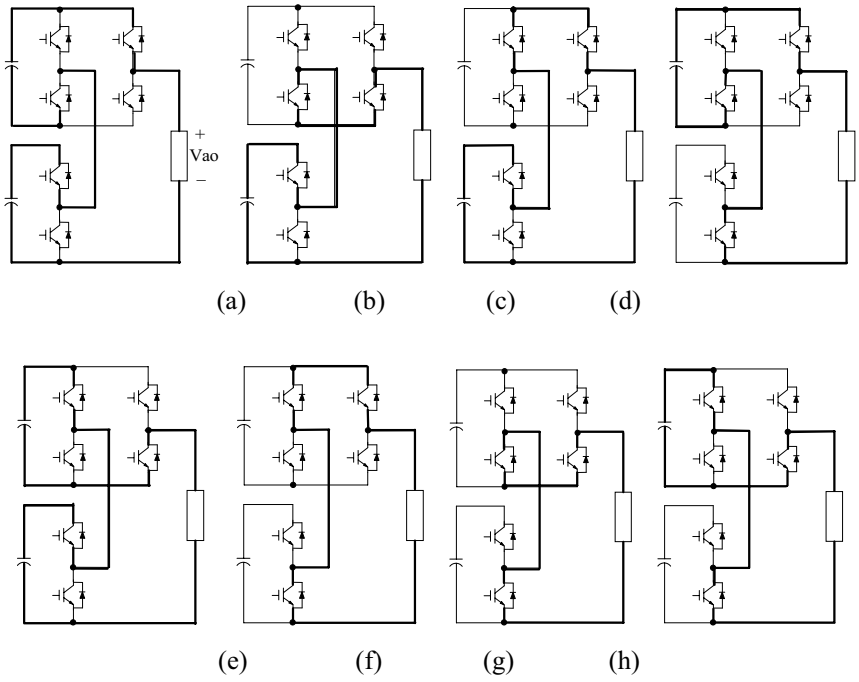


Fig. 4: Operation principle of the proposed circuit regarding a leg of the 4-level inverter.
(a) Switching state 3, Vao=2Vd, (b) Switching state 21, Vao=Vd, (c) Switching state 22, Vao=Vd
(d) Switching state 23, Vao=Vd, (e) Switching state 11, Vao=0, (f) Switching state 12, Vao=0
(g) Switching state 13, Vao=0, (h) Switching state 0, Vao=-Vd.

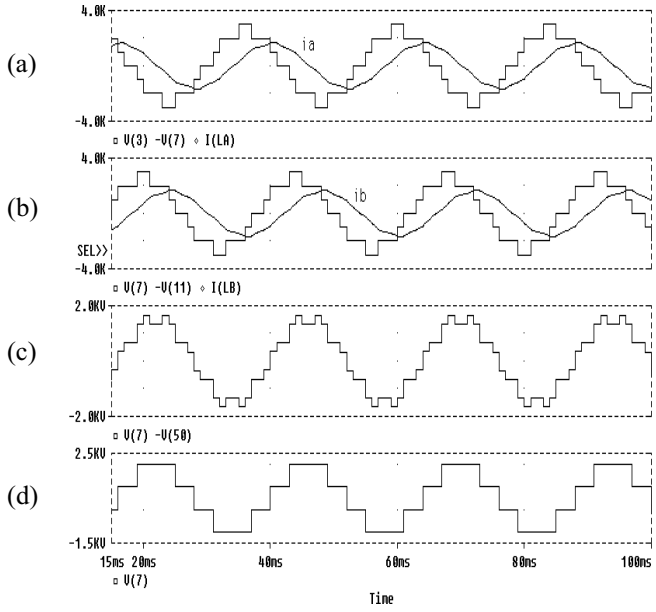


Fig. 5: PSpice simulation results for the three-phase 4-level inverter operation.

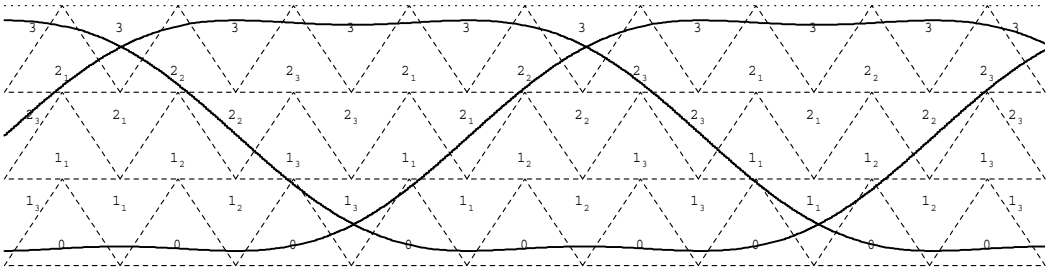
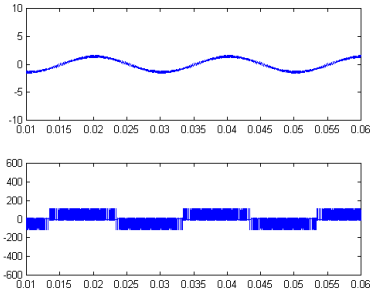
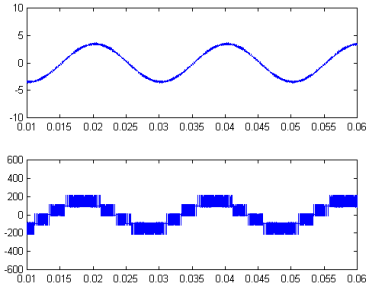


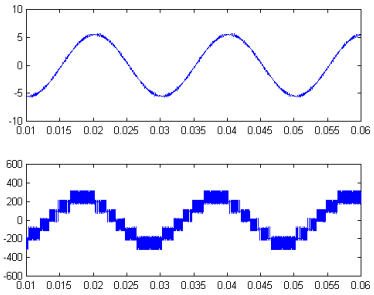
Fig. 6: PWM generation algorithm for the three-phase 4-level inverter.



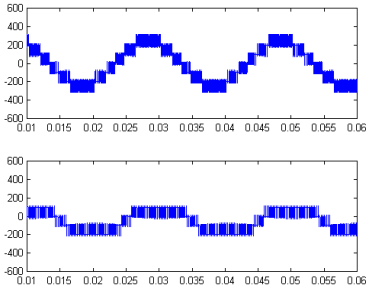
(a) I_a and V_{ab} in low modulation index



(b) I_a and V_{ab} in middle modulation index

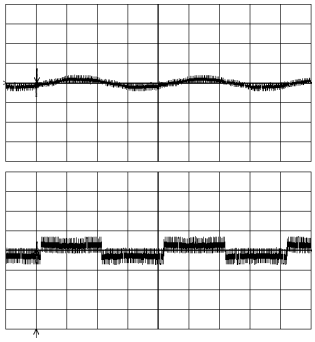


(c) I_a and V_{ab} in high modulation index

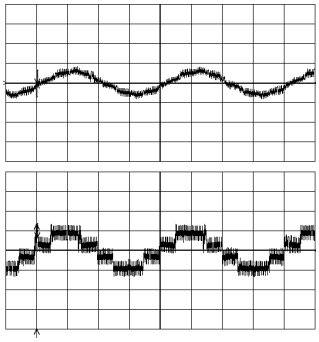


(d) V_{ab} and V_{ao} in high modulation index

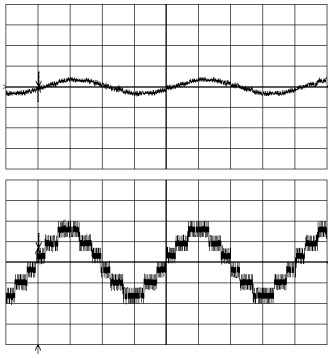
Fig. 7: Matlab simulation results for the three-phase 4-level inverter.



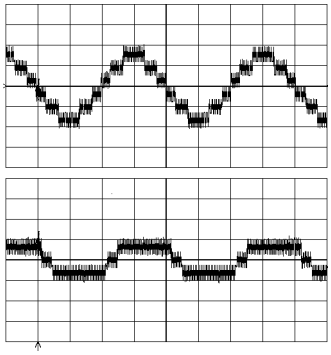
(a) I_a and V_{ab} in low modulation index (5A/div. 150V/div.)



(b) I_a and V_{ab} in middle modulation index (5A/div. 150V/div.)



(c) I_a and V_{ab} in high modulation index (10A/div. 150V/div.)



(d) V_{ab} and V_{ao} in high modulation index (5A/div. 150V/div.)

Fig. 8: Experimental verification for the three-phase 4-level inverter.