Complementary Half Controlled Three Phase PWM Boost Rectifier for Multi-DC-Link Applications

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Abstract— **The half controlled three phase pulse width modulated (HC3ΦPWM) boost rectifier has simpler and more robust structure compared to the full controlled three phase (FC3Φ) PWM boost rectifier (reduced switch count and shoot through free legs), and better performance compared to the diode rectifier (actively controlled dc link voltage and lower input current total harmonic distortion (THD)). One of the main drawbacks is its even harmonic input current distortion which may cause undesirable resonance problems. Other issues of concern are fairly large ac side inductance and the necessity of intentional lagging power factor current command to obtain reasonably low input current THD.**

This paper describes methods with which these problems can be handled for a certain type of applications by introducing complementary topologies of HC3ΦPWM boost rectifiers. Two types of complementary configuration, rectifier leg complementary and input transformer complementary, are introduced. The former comprises an emitter common and a collector common HC3ΦPWM boost rectifiers. The latter utilizes complementary polarity of the input transformer secondary windings. Application candidates are those which need multiple dc links, e.g. H-bridge multilevel inverter systems or some types of multidrive systems.

Two control schemes for this rectifier are presented, viz. a) independent local control (ILC) and b) coordinated central control (CCC). ILC can lead to even harmonics cancellation with equally supplied loads by two dc links. CCC can reduce not only even harmonics but also non-triplen odd harmonics (5th, 7th, ...). In CCC, ac side inductor size can be reduced and no lagging power factor current command is necessary. In addition, CCC can handle load imbalance between two dc links to a certain extent.

Power stage description, control principles, simulation results and experimental results are presented.

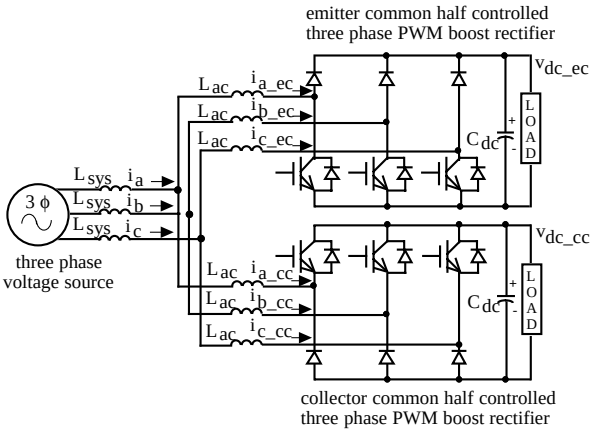

Fig. 1. Complementary half controlled three phase PWM boost rectifier (rectifier leg complementary)

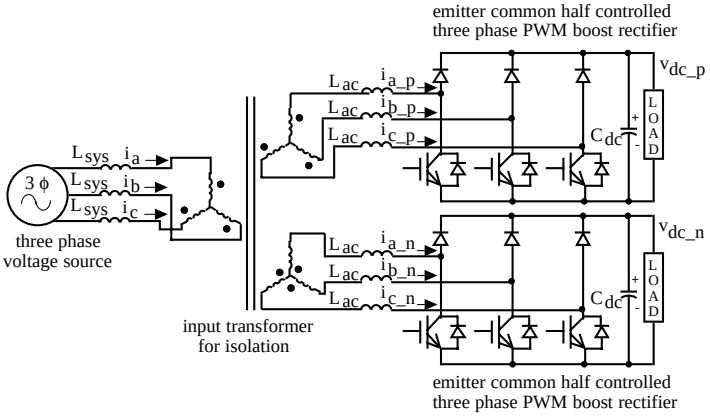

Fig. 2. Complementary half controlled three phase PWM boost rectifier (input transformer complementary)

I. Introduction

A study on the half controlled three phase pulse width modulated (HC3ΦPWM) boost rectifier has been reported in a recent publication [1]. This rectifier has simpler and more robust structure compared to the full controlled three phase (FC3Φ) PWM boost rectifier (reduced switch count and shoot through free legs), and better performance compared to the diode rectifier (actively controlled dc link voltage and lower input current total harmonic distortion (THD)) [1]. One of the main drawbacks is its even harmonic input current distortion which may cause undesirable resonance problems [1], [2]. Other issues of concern are fairly large ac side inductance and the necessity of intentional lagging power factor current command to obtain reasonably low input current THD [1].

This paper describes methods with which the abovementioned problems can be handled for a certain type of applications by using complementarily configured HC3ΦPWM boost rectifiers. These applications are those which need multiple dc links, e.g. H-bridge multilevel inverter systems [3] or some types of multidrive systems [4].

In the following sections, power stage description, control principles, simulation results and experimental results are presented. A conventional hysteresis current regulator is assumed as the method of current control throughout this work.

II. Complementary Half Controlled Three Phase PWM boost rectifiers

Fig. 1 shows a power stage schematic of the complementary HC3ΦPWM boost rectifier. The system consists of two HC3ΦPWM boost rectifiers [1] configured in complementary manner combining one collector common and one emitter common topology. This can be called *the rectifier leg complementary* configuration.

In both of the emitter common and collector common HC3ΦPWM boost rectifiers, it can be said that they have simpler structure compared to FC3ΦPWM boost rectifiers (only three controlled switches and gate drives, shoot through free leg structure), and are capable of better performance compared to diode rectifiers (actively controlled dc link voltage and lower input current THD). In addition, for the emitter common HC3ΦPWM boost rectifier, only one floating power supply for three gate drives is needed due to the emitter common structure. If complementary power semiconductor devices with comparable performance and cost would be available, a single floating power supply could be used for the collector common rectifier as well.

If the application needs input transformers for galvanic isolation, as in H-bridge multilevel inverters, the complementary structure can be transferred from the rectifier legs to the transformer secondary windings. Fig. 2 shows a power stage schematic of this topology. This can be called *the input transformer complementary* configuration.

In the transformer complementary approach, only the emitter common half controlled bridge topology can be used as a common building block. In Fig. 2, the ac side inductors, L_{ac}, can be thought of as partially or entirely leakage inductance of the input transformer.

It may be noted that the HC3ΦPWM boost rectifiers do not have power regenerating capability. This is incurred at the cost of obtaining shoot through free leg structure.

III. Control Schemes and Simulation Results

In this section, two control schemes for the complementary HC3ΦPWM boost rectifier and simulation results are presented. In the simulation, 600 [V] and 15 [A] (9 [kW]) of rated dc link voltage and current are assumed for each one of HC3ΦPWM boost rectifier with 230 [Vrms] line-to-line input voltage. In the simulation results to be presented, all the notations representing voltages and currents correspond to those in Fig. 1 unless otherwise specified.

A. Independent Local Control (ILC)

If two loads supplied by a complementary rectifier are equal to each other, a simple independent local control (ILC) theoretically leads to even harmonic cancellation because their even harmonics are out of phase by 180 degrees. The advantage of this scheme is its straightforwardness since it simply involves replicating the control scheme proposed for the stand alone HC3ΦPWM boost rectifier [1].

Fig. 3 shows *Saber* simulation results for a 25 [deg] lagging current command operation under a balanced load

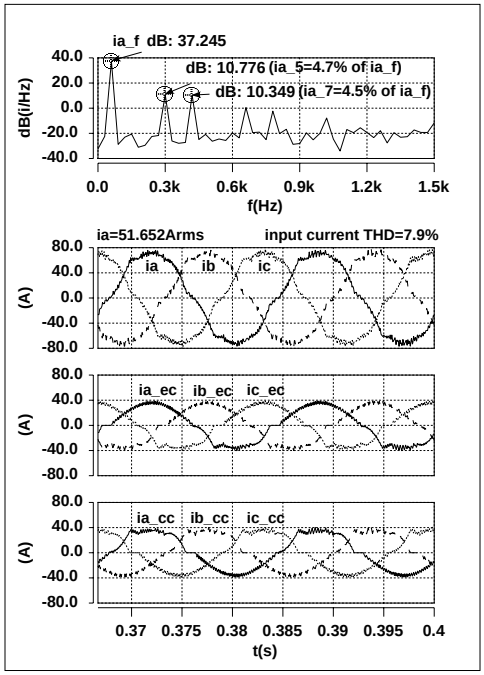

Fig. 3. *SABER* simulation results of ILC for balanced load operation with 25 [deg] lagging current command (ac source 230 [Vrms] line-to-line, L_{ac} =3.1 [mH] (0.2pu), dc link 600 [V] and 15 [A] for each dc load, the top trace is spectrum of overall input current i_a)

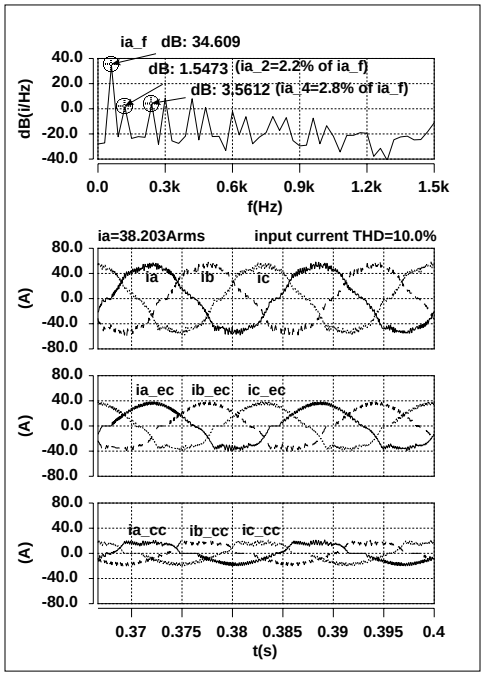

Fig. 4. *SABER* simulation results of ILC for 50 [%] unbalanced load operation with 25 [deg] lagging current command (ac source 230 [Vrms] line-to-line, L_{ac} =3.1 [mH] (0.2pu), dc link 600 [V] and dc load currents 15 [A] and 7.5 [A], the top trace is spectrum of overall input current i_a)

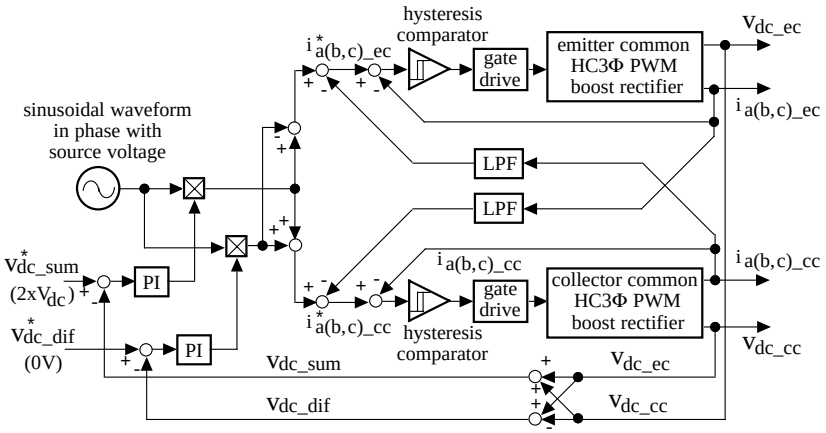

Fig. 5. Block diagram of Coordinated Central Control (CCC)

condition. The emitter common rectifier input currents, i_{a_ec}, i_{b_ec}, and i_{c_ec} and the collector common rectifier input currents, i_{a_cc}, i_{b_cc}, and i_{c_cc}, are in the relation of inverted and 180 [deg] phase shifted with each other. Though each one of HC3ΦPWM boost rectifier input current does not have half-wave symmetry, the overall input currents shown in Fig. 3, i_a, i_b and i_c, regain half-wave symmetry and the even harmonics are eliminated. The non-triplen odd harmonics (5th, 7th, ...) are however still present as shown in this figure.

Fig. 4 shows *Saber* simulation results for a 25 [deg] lagging current command operation with loads having 50 [%] imbalance. Since each half controlled rectifier is independently controlled, the load imbalance directly reflects on the overall input current even harmonic distortion.

B. Coordinated Central Control (CCC)

A coordinated central control (CCC) is expected to be able to reduce the non-triplen odd harmonics in the overall input currents and to handle load imbalance to a certain extent. Fig. 5 shows a block diagram of CCC. Two proportional-integral (PI) control loops, one for each the sum and the difference of the two dc link voltages are used for the sinusoidal current reference amplitude calculation, where the PI controller gain of the dc link voltage difference nulling is smaller than that of the dc link voltage sum regulating. The cross-coupled current feedback loops make it possible for each one of the HC3ΦPWM boost rectifiers to function as an active harmonic filter for the other. Here, the cut-off frequency of two low-pass filters (LPF's) on the cross coupling feedback paths is fairly important. If this cut-off frequency is too high, a current regulator unwantedly responds to the other one's switching frequency ripple. If it is too low, the desired mutual power filtering effect can not be obtained.

It is important to note here that each rectifier participates in controlling its own real power transfer and the other one's harmonic compensation simultaneously. This is a quite consistent approach with IEEE-519 which is not an equipment oriented harmonic standard but a point of common coupling (PCC) oriented standard [5] [6]. In addition, because of the mutual active filtering effect between the two HC3ΦPWM rectifiers, unlike ILC operation, not only the even harmonics but also non triplen odd harmonics are suppressed. This harmonic compensation performance now can make the ac side inductor size smaller than that of ILC operation, as far as the switching frequency limitation allows, and the lagging power factor current command operation is no longer necessary.

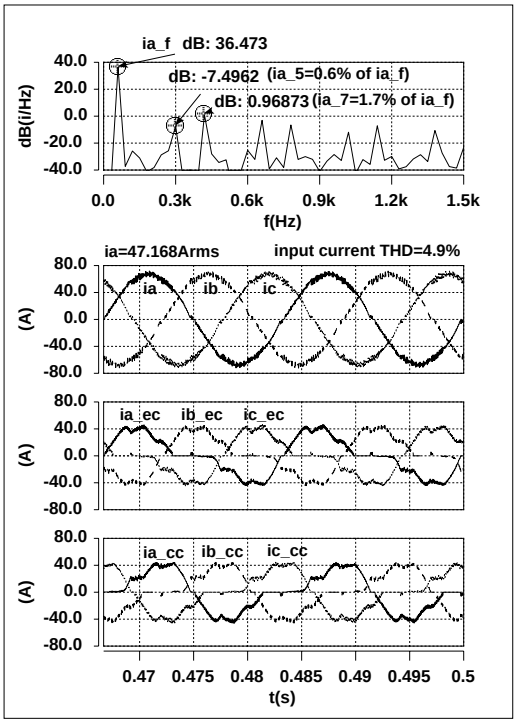

Fig. 6. *SABER* simulation results of CCC for balanced load operation (ac source 230 [Vrms] line-to-line, L_{ac} =1.5 [mH] (0.1pu), dc link 600 [V] and 15 [A] for each dc load, the top trace is spectrum of overall input current i_a)

Fig. 6 shows *Saber* simulation results for a balanced load operation. The ac side inductor size is 0.1 [pu] and the switching frequency of the hysteresis current controller is 7 $\sim$ 13 [kHz] (beyond the range of the top trace in Fig. 6). Without lagging power factor current command, much lower input current THD, 4.9 [%], is obtained.

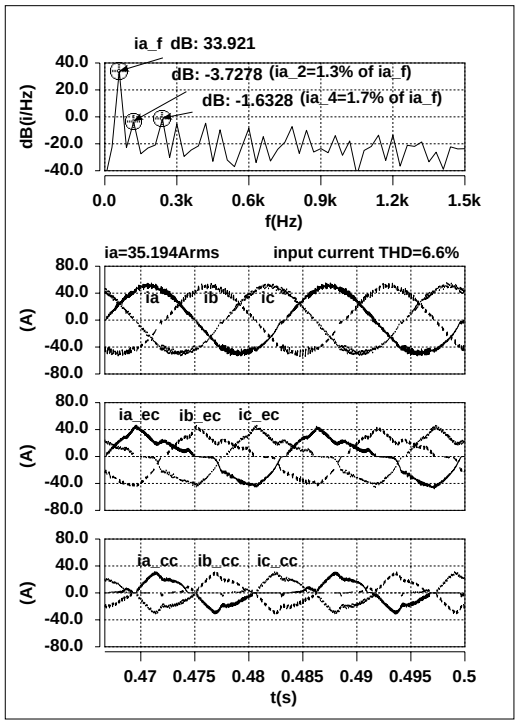

Fig. 7. *SABER* simulation results of CCC for 50 [%] unbalanced load operation (ac source 230 [Vrms] line-to-line, L_{ac} =1.5 [mH] (0.1pu), dc link 600 [V] and dc load currents 15 [A] and 7.5 [A], the top trace is spectrum of overall input current i_a)

Fig. 7 shows *Saber* simulation results with loads having 50 [%] imbalance. Even with this amount of load imbalance, the even harmonics are still reasonably suppressed, and the input current THD is maintained at a fairly low level, 6.6 [%] in this simulation. These results suggest the potential of this approach for meeting IEEE-519 for systems whose short circuit ratio is as small as 20 [5].

Fig. 8 and Fig. 9 show *Saber* simulation results of dc link voltage ripples and dc load currents for a balanced and an unbalanced load condition, corresponding to Fig. 6 and Fig. 7, respectively. Each dc link capacitance is 1000 [μF] and 0.1 [Ω] of equivalent series resistance (ESR) is assumed. The peak-to-peak dc link voltage ripple is approximately 3 [%] in both cases.

Almost the same simulation results have been obtained for *the input transformer complementary* HC3ΦPWM boost rectifier, Fig. 2, though lack of space does not allow to present them here.

IV. Experimental Results

In this section, experimental results obtained with a laboratory prototype of the complementary HC3ΦPWM boost rectifier are presented. This prototype is rated for 300 [V] and 7.5 [A] (2.25 [kW]) on each one of the dc links with 115 [Vrms] line-to-line voltage on the ac source side.

In the experiment, approximately 1.0 [%] of background distortion has been observed in the three phase ac source voltage.

A dynamic signal analyzer *HP 3561A* has been used for harmonic measurement. The spectra presented here are rms averaged results of 256 measurements.

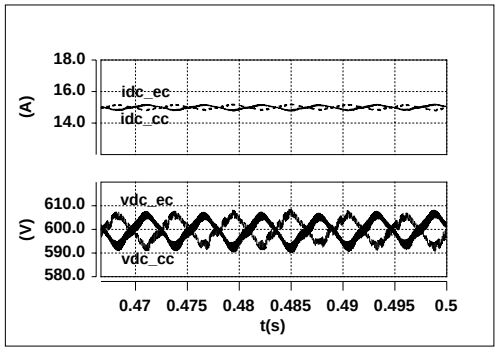

Fig. 8. *SABER* simulation results of load current and dc link voltage ripple for balanced load operation with CCC (C_{dc}=1000[μF] and ESR=0.1[Ω]. Operating condition is the same as that of Fig. 6)

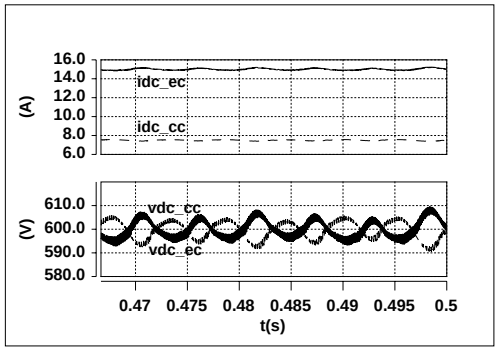

Fig. 9. *SABER* simulation results of load current and dc link voltage ripple for unbalanced load operation wit CCC (C_{dc}=1000[μF] and ESR=0.1[Ω]. Operating condition is the same as that of Fig. 7)

A. Independent Local Control (ILC)

Fig. 10 and Fig. 11 show experimental ac current waveforms and overall input current spectrum, respectively, for ILC with balanced loads, where line-to-line voltage v_{cb}, trace1, is shown along with the input current for phase reference purpose. The maximum point of v_{cb} which coincides with the origin point of time axis is 0 [deg] reference for unity power factor angle. The current waveforms are in reasonably good agreement with the corresponding simulation results shown in Fig. 3. The measured input current THD is 7.0 [%]. This value is slightly better than that of the simulation result. The probable cause of this is that the equipment used for harmonic measurement is capable of THD computation with first 20 harmonics [7]. This is the case for all the following experimentally measured THD values.

Fig. 12 and Fig. 13 show experimental results for ILC with loads having an imbalance of about 50 [%], which correspond to Fig. 4.

In Fig. 10 through Fig. 13, compared to stand alone operation results presented in reference [1], the even harmonics are well suppressed, although the perfect even harmonic cancellation can not be realized even with balanced

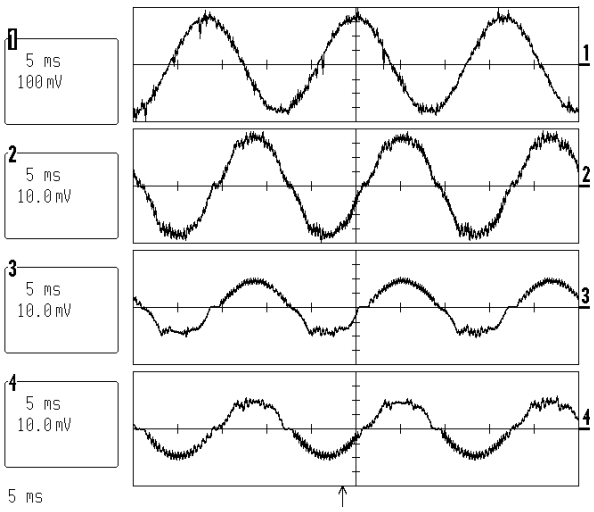

Fig. 10. Experimental results of ILC for balanced load operation with 25 [deg] lagging current command (ac source 117 [Vrms] line-to-line, L_{ac} =3.1 [mH] (0.2pu), dc link 300 [V] and 7.5 [A] for each dc load), trace 1: v_{cb}, 50 [V/div], trace2: i_a, trace3: i_{a_ec}, trace4: i_{a_cc}, 10 [A/div], time axis 5 [ms/div]

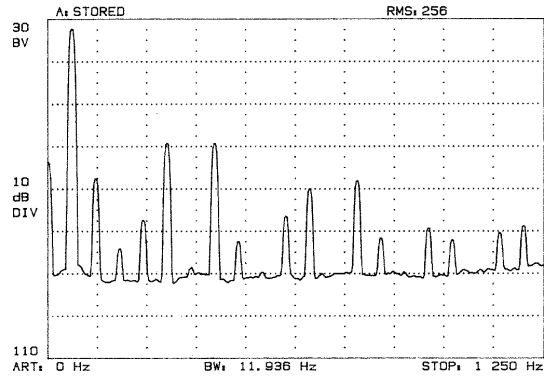

Fig. 11. Experimental spectrum of overall input current i_a in Fig. 10, THD=7.0 [%] (computed with up to the 20th harmonic)

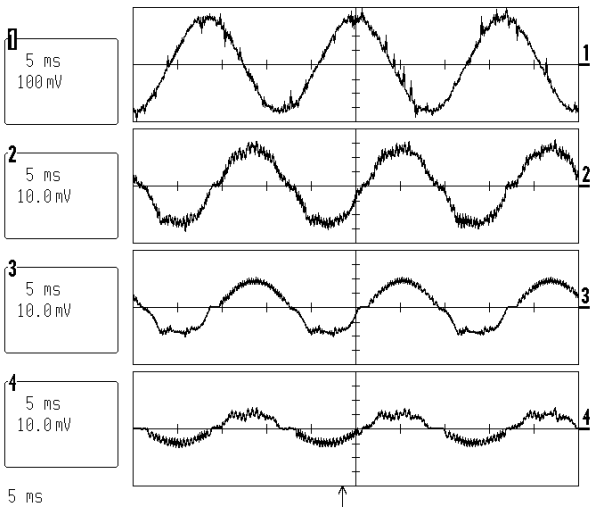

Fig. 12. Experimental results of ILC for unbalanced load operation with 25 [deg] lagging current command (ac source 117 [Vrms] line-to-line, L_{ac} =3.1 [mH] (0.2pu), dc link 300 [V] and dc load current 7.5 [A] and 4.4 [A]), trace 1: v_{cb}, 50 [V/div], trace2: i_a, trace3: i_{a_ec}, trace4: i_{a_cc}, 10 [A/div], time axis 5 [ms/div]

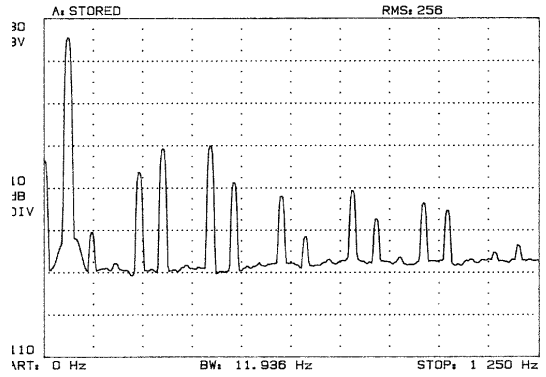

Fig. 13. Experimental spectrum of overall input current i_a in Fig. 12, THD=8.3 [%] (computed with up to the 20th harmonic)

loads. This is because that it is difficult to achieve the exact complementary operation in practical situations. In Fig. 13, it is observed that the second harmonic is decreased with the load imbalance. The cause of this rather strange phenomenon is currently under investigation. As expected, the non triplen odd harmonics observed here are fairly large.

B. Coordinated Central Control (CCC)

In the hardware experiments for CCC, unity power factor current command is maintained and the ac side inductor value has been reduced from 0.2 [pu] of ILC to 0.1 [pu].

Fig. 14 and Fig. 15 show experimental ac current waveforms and overall input current spectrum, respectively, for CCC with balanced loads. These are in reasonably good agreement with corresponding simulation results shown in Fig. 6.

Compared to experimental results of ILC shown in Fig. 10, the overall input current waveform is closer to sinusoid. This is because, as observed in the spectrum of Fig. 15, not only even harmonics but also non-triplen odd harmonics are reduced by CCC. In addition, phase relation between v_{cb} and i_a shows that almost unity power factor operation is realized.

Fig. 17 and Fig. 18 show experimental results for CCC with loads having an imbalance of about 50 [%]. It may be observed that current waveforms are in reasonably good agreement with those of simulation results shown in Fig. 7. With this load imbalance, the overall input current, i_a, is still maintained to be fairly sinusoidal.

Fig. 16 and Fig. 19 show experimental dc link voltage ripple for a balanced and an unbalanced load condition, corresponding to Fig. 14 and Fig. 17, respectively. Similar to the simulation results of Fig. 8 and Fig. 9, 180 [Hz] ripple is dominant and its peak-to-peak magnitude is approximately 4 [%] of the dc link voltage.

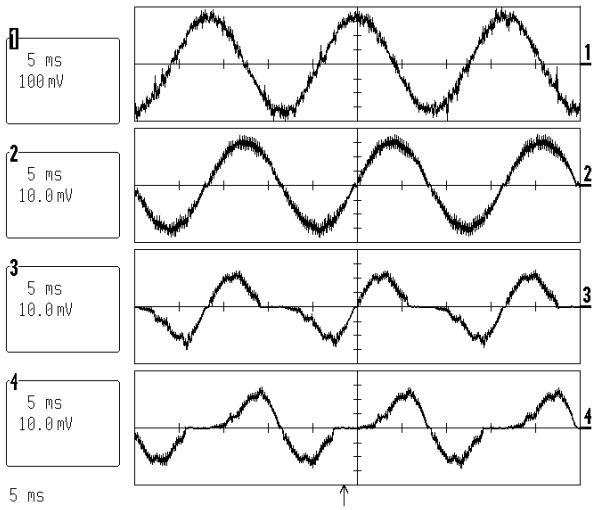

Fig. 14. Experimental results of CCC for balanced load operation with unity power factor current command (ac source 117 [Vrms] line-to-line, L_{ac} =1.5 [mH] (0.1pu), dc link 300 [V] and 7.5 [A] for each dc load), trace 1: v_{cb}, 50 [V/div], trace2: i_a, trace3: i_{a_ec}, trace4: i_{a_cc}, 10 [A/div], time axis 5 [ms/div]

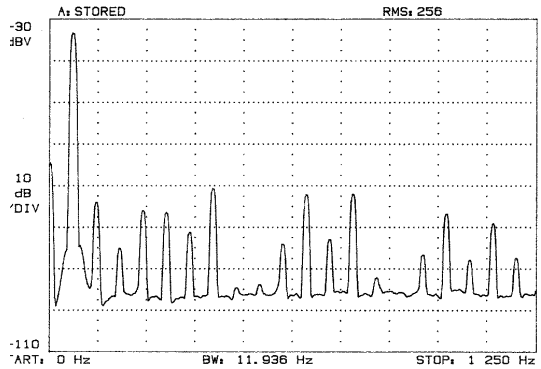

Fig. 15. Experimental spectrum of overall input current i_a in Fig. 14, THD=2.8 [%] (computed with up to the 20th harmonic)

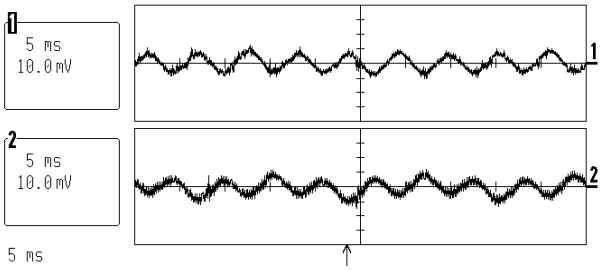

Fig. 16. Experimental dc link voltage ripple of CCC for balanced load operation of Fig. 14 (C_{dc}=1250[μF]), trace 1: v_{dc_ec}, trace2: v_{dc_cc}, 5 [V/div], time axis 5 [ms/div]

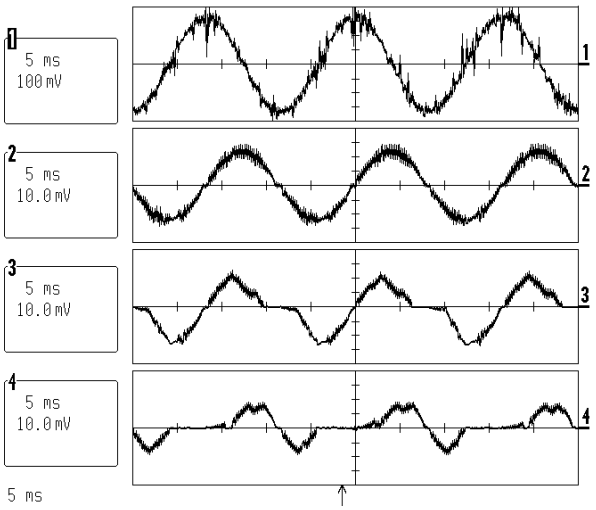

Fig. 17. Experimental results of CCC for unbalanced load operation with unity power factor current command (ac source 117 [Vrms] line-to-line, L_{ac} =1.5 [mH] (0.1pu), dc link 300 [V] and dc load current 7.5 [A] and 4.3 [A]), trace 1: v_{cb}, 50 [V/div], trace2: i_a, trace3: i_{a_ec}, trace4: i_{a_cc}, 10 [A/div], time axis 5 [ms/div]

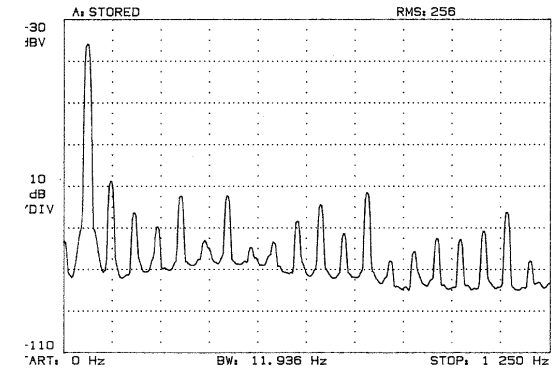

Fig. 18. Experimental spectrum of overall input current i_a in Fig. 17, THD=4.2 [%] (computed with up to the 20th harmonic)

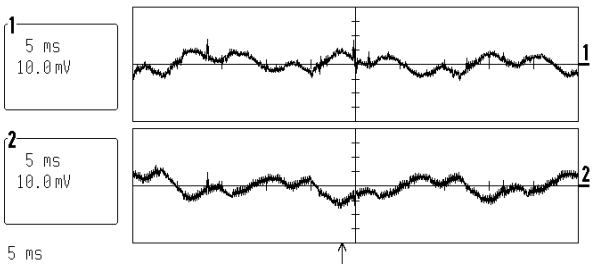

Fig. 19. Experimental dc link voltage ripple of CCC for unbalanced load operation of Fig. 17 (C_{dc}=1250[μF]), trace 1: v_{dc_ec}, trace2: v_{dc_cc}, 5 [V/div], time axis 5 [ms/div]

Fig. 20 shows measured characteristics of load imbalance vs. low order harmonics with respect to fundamental component, I_f, and THD, where the load imbalance is expressed as the ratio of R_{dc_cc} to R_{dc_ec} with R_{dc_ec}=1.0 [pu]. Then, the operating condition of Fig. 12 and Fig. 17, i.e. i_{dc_ec}=7.5 [A] and i_{dc_cc}≈4.4 [A], corresponds to R_{dc_cc}/R_{dc_ec} = 1.7. According to this measured data, 4th and 7th harmonics are fairly well suppressed, and 2nd and 5th harmonics increase as the dc link load imbalance increases, and accordingly THD increases.

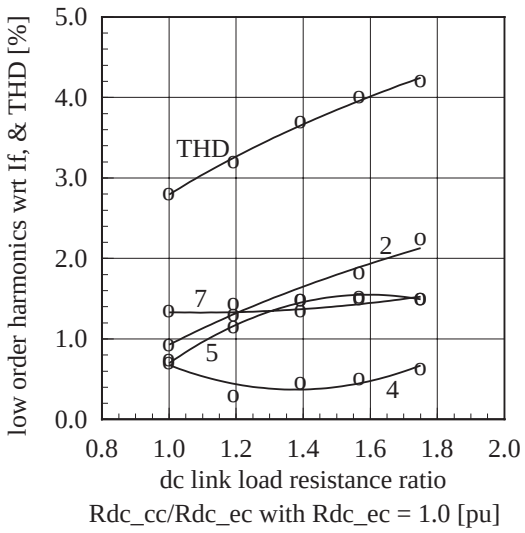

Fig. 20. Experimentally measured characteristics of load imbalance vs. low order harmonics with respect to fundamental component I_f, and THD for CCC (THD is computed with up to the 20th harmonic)

Referring to IEEE-519, even harmonics are limited to 25 [%] of the odd harmonic limits [5]. For example in the case of a system with short circuit ratio,$20 < I_{sc}/I_L < 50$, 2nd harmonic component should be less than 1.75 [%] of I_L. Since I_L is the maximum demand load current fundamental component at PCC and $I_f \leq I_L$, the measure taken in Fig. 20 is a more conservative metric, similar to the difference between THD and the total demand distortion (TDD).

The judgment on if or not a system can satisfy a harmonic standard such as IEEE-519 should be based on measurement with long term operation. In addition, even harmonic limitation monitoring involves fairly subtle measurement because of its even less maximum limit. However, it has been demonstrated here on a laboratory experiment basis that the complementary HC3ΦPWM rectifier with CCC has a potential to realize a rectifier front-end for multi-dc-link applications with meeting IEEE-519 standard.

V. Conclusions

The complementary HC3ΦPWM boost rectifier for multi-dc-link applications has been investigated. It has been shown that the main disadvantages associated with stand alone operation of HC3ΦPWM boost rectifier, i.e. even harmonic input current distortion, large ac side inductor, and lagging power factor current command operation for low THD, can greatly be mitigated by the approach presented here.

Two control schemes, ILC and CCC, have been introduced and their performance has been studied with simulations and hardware experiments. In particular, it has been demonstrated that CCC has a capability to reduce not only even harmonics but also non-triplen odd harmonics and has potential to meet IEEE-519 with certain dc link load imbalance handling capability.

In this paper, *the rectifier leg complementary* structure, Fig. 1, has almost exclusively been discussed. However, as mentioned in Section III, the same simulation results have been obtained for *the input transformer complementary* structure, Fig. 2. Experimental work on *the input transformer complementary* configuration is currently under progress.

So far, only the steady state operation characteristics of the complementary HC3ΦPWM boost rectifier have been studied mainly from the power quality point of view. Since, unlike diode rectifiers, HC3ΦPWM boost rectifiers are capable of active dc link voltage control, the dynamic characteristics is another issue of interest. For example, if the system could handle the voltage sag problem to a certain extent, or could manage to softly recover from an ac source voltage upset, this would be an added advantage of HC3ΦPWM boost rectifier front-end. The dynamic characteristic investigation should be one of the focuses for future work.

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References

[1] J. Kikuchi, M. D. Manjrekar and T. A. Lipo, "Performance Improvement of Half Controlled Three Phase PWM Boost Rectifier," *Proceedings of IEEE PESC 99*, 1999, pp. 319-324.

[2] A. Mansoor, J. McGee and F. Z. Peng, "Even-Harmonics Concerns at an Industrial Facility Using a Large Number of Half-Controlled Rectifiers," *Proceedings of IEEE APEC 98*, 1998, pp. 994-1000.

[3] P. W. Hammond, "A New Approach to Enhance Power Quality for Medium Voltage AC Drives," *IEEE Trans. on Industry Applications*, Vol. IA-33, No. 1, 1997, pp. 202-208.

[4] E. P. Wiechmann, R. P. Burgos and J. R. Rodriguez, "Active Front-End Optimization using Six-Pulse Rectifiers in Multi-Motor AC Drives Applications," *Conference Record of IEEE IAS 98*,1998,pp.1294-1299.

[5] IEEE Industry Applications Society/Power Engineering Society, *IEEE Std 519-1992, IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE, 1993, esp. Table 10.3 in p. 78.

[6] C. K. Duffey and R. P. Stratford, "Update of Harmonic Standard IEEE-519: IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems," *IEEE Trans. on Industry Applications*, Vol. IA-25, No. 6, 1989, pp. 1025-1034.

[7] Hewlett Packard, *3561A Dynamic Signal Analyzer, Operating Manual*, Hewlett Packard, 1983, p. XXXXI