A Novel Control Method for Input Output Harmonic Elimination of the PWM Boost Type Rectifier Under Unbalanced Operating Conditions

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***Abstract*—This paper presents a new control strategy to improve the performance of the PWM Boost Type Rectifier when operating under an unbalanced supply. An analytical solution for harmonic elimination under unbalanced input voltages is obtained resulting in a smooth (constant) power flow from ac to dc side in spite of the unbalanced voltage condition. Based on the analysis of the open loop configuration, a closed loop control solution is proposed. Simulation results show excellent response and stable operation of the new rectifier control algorithm. A laboratory prototype has been designed to verify the discussions and analyses done in this paper. Theoretical and experimental results show excellent agreement. Elimination of the possibility of low order ac and dc side harmonics due to unbalance is expected to materially affect the cost of dc link capacitor and ac side filter. The proposed method will be particularly useful in applications where the large second harmonic at the DC link may have a severe impact on system stability of multiply connected converters on a common link.**

***Index Terms*—PWM boost type rectifier, unbalanced conditions.**

I. Introduction

THE boost type PWM rectifier has been increasingly employed in recent years since it offers the possibility of a low distortion line current with unity power factor for any load condition [2], [6]. Another advantage over traditional phase-controlled thyristor rectifiers is its capability for nearly instantaneous reversal of power flow. Unfortunately, the features the PWM boost type rectifier offers are fully realized only when the supply three phase input voltage source is balanced both in terms of its Thevenin equivalent voltage and impedance, which is often not the case in a real power system. It has been shown [1] that unbalanced input voltages or impedances cause an abnormal second harmonic at the dc bus, which reflects back to the input causing a (nonzero sequence) third-order harmonic current to flow. Next, the third-order harmonic current causes a fourth-order harmonic voltage on the dc bus, and so on. This results in the appearance of even harmonics at the dc output and odd harmonics in the input currents. These additional components cause added losses in the dc link filter capacitor. They must also be considered in the filter design of these converters since they clearly add to the cost because they are of low frequency. In addition, ripple on the dc link is a known cause of interaction between current regulators which can even cause system instability [7]. The problem increases in severity as the number of converters connected to the link increases. While an attempt was made to reduce low order harmonics at the input and the output of the PWM Boost Type Rectifier under unbalance [4], harmonics were only reduced but not eliminated. Enjeti and Choudhury [5] proposed a method for the harmonic elimination of the buck ac to dc converter under unbalanced conditions. However, the approach does not lend itself well to the more popular boost type rectifier so that an exact solution for this problem has never been addressed.

This paper proposes a completely new control strategy for harmonic elimination of the PWM Boost Type rectifier operating under unbalanced input voltages. Specifically, by PWM current regulation, the magnitudes and the phase angles of the three input currents are independently adjusted in order to maintain a smooth output dc voltage level entirely eliminating low-order harmonics. The proposed technique maintains a high quality sinusoidal current input and dc current output even though the input voltages remain unbalanced. However, the power factor cannot be adjusted in this case. This is not seen as a disadvantage particularly in situations where imbalance in the input supply is a temporary phenomenon. Simulation as well as experimental results is presented to confirm the proposed control strategy. The theoretical and experimental results show excellent agreement.

II. Theoretical Approach

In Fig. 1 it is assumed that the PWM rectifier is supplied by unbalanced input voltages but balanced input impedances. The assumptions used in the derivation are as follows.

1) The system is lossless.
2) The switching functions used to represent switching action of the converter are unbalanced but contain no zero sequence.
3) Only fundamental components of switching functions and input currents are taken into account (PWM switching harmonics are not considered).

By using symmetrical component theory, line to neutral switching functions are given as

$$\begin{matrix} \\ SW_1,\, SW_2,\, SW_3 \end{matrix}$$

$$\begin{bmatrix} SW_1 \\ SW_2 \\ SW_3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \cdot \begin{bmatrix} 0 \\ S^+ \\ S^- \end{bmatrix}. \tag{1}$$

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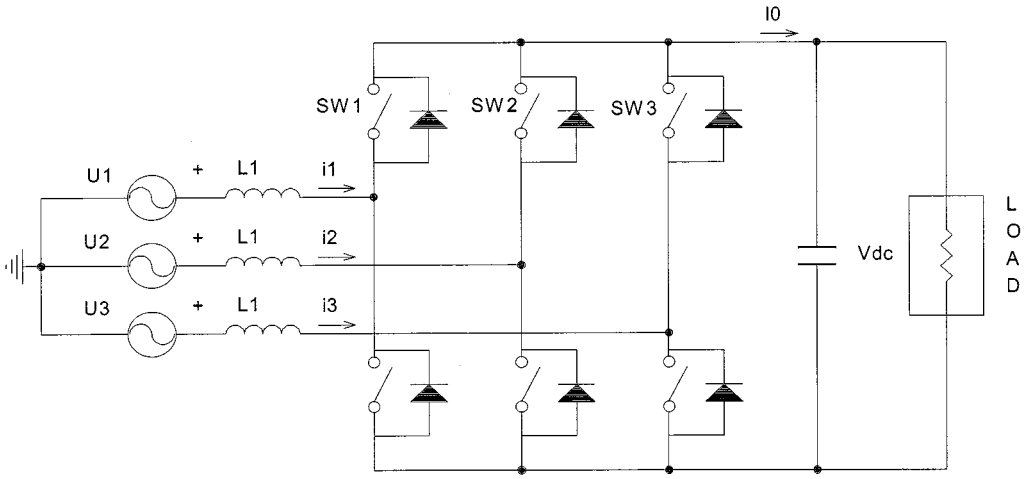

Fig. 1. PWM boost type rectifier.

Since the zero sequence current is never present in this circuit, currents I_1, I_2 and I_3 are given by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \cdot \begin{bmatrix} 0 \\ I^+ \\ I^- \end{bmatrix} \tag{2}$$

where

S^+ and S^- positive and negative sequence switching functions;

I^+ and I^- positive and negative sequence currents;

a $1 \angle 120^0$.

Output current I_0 is given by

$$\begin{aligned} I_0 &= SW_1 I_1 + SW_2 I_2 + SW_3 I_3 \\ &= (S^+ + S^-)(I^+ + I^-) + (a^2 S^+ + aS^-)(a^2 I^+ + aI^-) \\ &\quad + (aS^+ + a^2 S^-)(aI^+ + a^2 I^-) \\ &= 3S^+ I^- + 3S^- I^+. \end{aligned} \tag{3}$$

In the time domain, the pulsating component of the output current is expressed as

$$\begin{aligned} I_0(t) = {} & 3 \text{ Real} \left(|S^+| e^{jwt} e^{j\theta_s^+} \right) \text{ Real} \left(|I^-| e^{jwt} e^{j\theta_i^-} \right) \\ & + 3 \text{ Real} \left(|S^-| e^{jwt} e^{j\theta_s^-} \right) \text{ Real} \left(|I^+| e^{jwt} e^{j\theta_i^+} \right). \end{aligned} \tag{4}$$

By using trigonometric identity

$$\cos(\alpha)\cos(\beta) = 1/2\,[\cos(\alpha+\beta) + \cos(\alpha-\beta)]$$

one arrives at the result

$$\begin{aligned} I_o(2wt) = {} & 3/2|S^+|\,|I^-| \cos(2wt + \theta_s^+ + \theta_i^-) \\ & + 3/2|S^-|\,|I^+| \cos(2wt + \theta_s^- + \theta_i^+). \end{aligned} \tag{5}$$

The previous equation shows the presence of the second-order harmonic at the output of the rectifier. It also indicates that the second-order harmonic could be eliminated under the following conditions.

1)

$$|S^+|\,|I^-| = |S^-|\,|I^+|$$

2)

$$\theta_s^- + \theta_i^+ = \pi + \theta_s^+ + \theta_i^- \tag{6}$$

where S^+, S^-, θ_s^+ and θ_s^- are magnitudes and phase shifts of positive and negative switching functions. I^+, I^-, θ_i^+ and θ_i^- are magnitudes and phase shifts of input currents.

The per-phase equivalent circuits under unbalanced input voltages and unbalanced synthesized voltages at the input of the rectifier are shown in Fig. 2. From Fig. 2, two additional equations can be obtained and given by,

$$ZI^+ = U^+ - V_s^+ \tag{7}$$

$$ZI^- = U^- - V_s^- \tag{8}$$

where V_s^+ and V_s^- are the positive and negative sequence voltages at the rectifier input and U^+ and U^- are the positive and negative sequence input voltages.

$$V_s^+ = V_{\rm dc} S^+ / 2\sqrt{2}, \quad V_s^- = V_{\rm dc} S^- / 2\sqrt{2}$$

where $V_{\rm dc}$ is the output dc voltage.

From the power equation, the following relationship can be obtained:

$$P_{\rm dc} = \text{Real}(3U^+ I^+ + 3U^- I^-) \tag{9}$$

where $P_{\rm dc}$ is the average output power.

The solution for harmonic elimination is obtained by combining (6)–(9). The solution is given by the following set of equations:

1) $$\frac{|S^+|}{|S^-|} = \frac{|U^+|}{|U^-|} \tag{10}$$

2) $$\theta_u^- - \theta_s^- = \theta_s^+ - \theta_u^+ \tag{11}$$

3) $$|S^+| = \frac{2\sqrt{2}|U^+|}{V_{\rm dc}} \cos(\theta_u^+ - \theta_s^+) \tag{12}$$

4) $$\sin 2(\theta_u^+ - \theta_s^+) = \frac{2P_{\rm dc} Z}{3(|U^{+2}| - |U^{-2}|)}. \tag{13}$$

The set of four equations shown above represents the steady-state solution for input–output harmonic elimination of the PWM boost type rectifier under unbalanced input voltages.

The steady-state solution is also presented in graph form on Fig. 2.

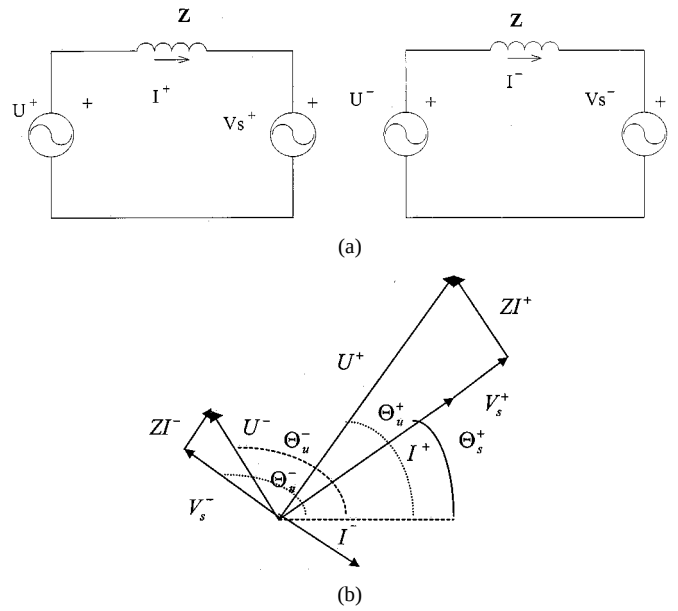

Fig. 2. (a) Per-phase positive and negative sequence equivalent circuit. (b) Graph representation of the proposed solution for harmonic elimination.

A. The Physical Meaning of the Proposed Solution in d–q Stationary Frame

The proposed solution for harmonic elimination can be explained in the d–q stationary frame, where cancellation of input pulsating power becomes more obvious. The positive and negative sequence components of the input voltages and currents are instantaneous quantities and are shown on Fig. 3.

The instantaneous power input, $p(t)$ is given by

$$p(t) = p_0(t) + p_1(t) + p_2(t) + p_3(t) \tag{14}$$

where

$$p_0(t) = 3/2(u_{pq}i_{pq} + u_{pd}i_{pd} + u_{nq}i_{nq} + u_{nd}i_{nd}) \tag{15}$$

$$p_1(t) = 3/2(u_{pq}i_{nq} + u_{nq}i_{pq} + u_{pd}i_{nd} + u_{nd}i_{pd}) \tag{16}$$

$$p_2(t) = 3/2(u_{pd}i_{pq} - u_{pq}i_{pd}) \tag{17}$$

$$p_3(t) = 3/2(u_{nd}i_{nq} - u_{nq}i_{nd}). \tag{18}$$

The first term, $p_0(t)$, represents the constant portion of input pulsating power, since all its components are products of in-phase q and d quantities of the positive and negative sequence input voltages and currents. This term also exists in a balanced three-phase system.

The second term, $p_1(t)$, represents the pulsating portion, since all its components are products of the positive and negative in-phase components of input currents and voltages. It basically represents a mutual interaction between positive and negative sequence quantities, which normally does not exist in a balanced three-phase system.

The third term, $p_2(t)$, represents the interaction between d and q positive sequence quantities. This term exists in a balanced three-phase system.

The fourth term, $p_3(t)$, represents the interaction between d and q negative sequence quantities. This term does not normally exist in a balanced three-phase system.

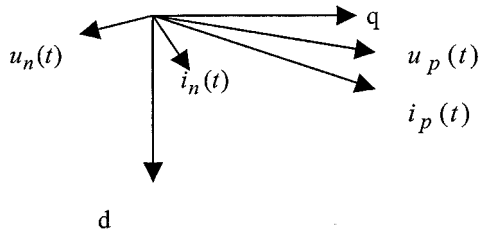

Fig. 3. The positive and negative sequence input voltages and currents in d–q stationary frame.

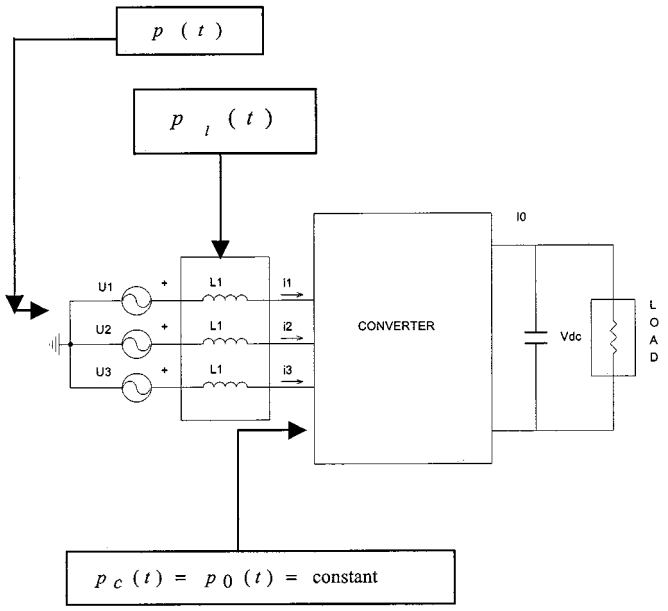

Fig. 4. Cancellation of the instantaneous pulsating power.

Similarly, instantaneous power on the inductor, $p_l(t)$, consists of three parts and can be expressed as

$$p_{1l}(t) = 3/2\,wL(2i_{pd}i_{nq} - 2i_{pq}i_{nd}) \tag{19}$$

$$p_{2l}(t) = 3/2\,wL(i_{pq}i_{pq} + i_{pd}i_{pd}) \tag{20}$$

$$p_{3l}(t) = 3/2\,wL(i_{nq}i_{nq} + i_{nd}i_{nd}). \tag{21}$$

The solution for second harmonic elimination assumes the following form:

1) $$p_1(t) = p_{1l}(t) \tag{22}$$

2) $$p_2(t) = p_{2l}(t) \tag{23}$$

3) $$p_3(t) = p_{3l}(t) \tag{24}$$

The power going into the converter is given by

$$p_c(t) = p(t) - p_l(t). \tag{25}$$

The power going into the converter, as shown in Fig. 4, is constant since all the other components are shown to cancel out.

III. Control Method

Based on the analysis of the open loop configuration presented above, a feed-forward control method is proposed. In order to control the output dc voltage and eliminate harmonics at the input and output of the PWM Boost Type Rectifier under unbalance, not only current magnitudes but also their phase angles have to be controlled. The DC bus error is used to synthesize the

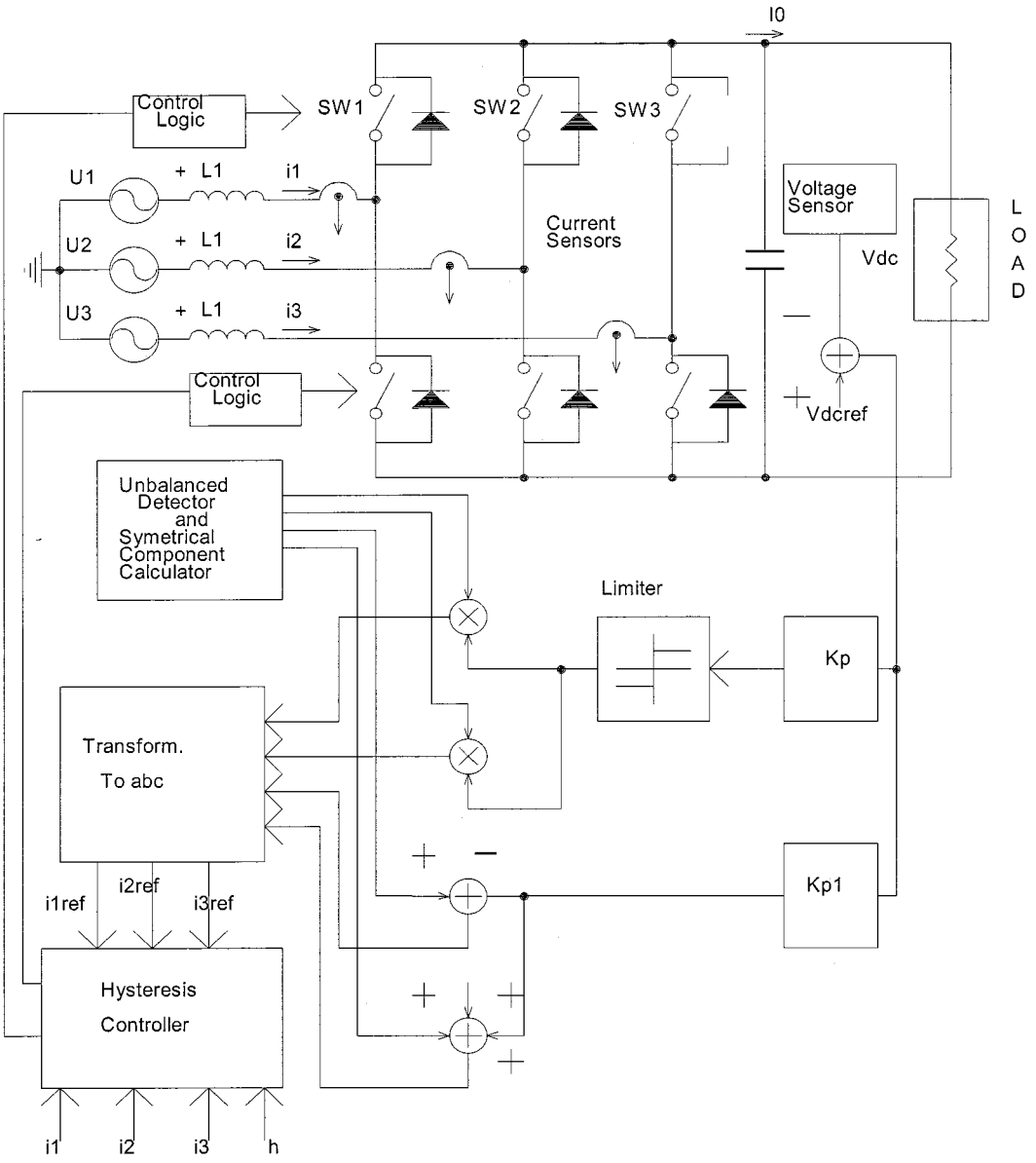

Fig. 5. Proposed control loop solution under unbalanced input voltages.

magnitudes and the phase angles of the positive and negative sequence reference currents. The sequence components are then transformed into three phase (abc) quantities which become reference signals for the hysteresis controller [3].

The relationship between input currents and input voltages in the open loop configuration for harmonic elimination is obtained by combining (7), (8), (10) and (11) and given by

$$\frac{|U^+|}{|U^-|} = \frac{|I^+|}{|I^-|} \tag{26}$$

$$\theta_u^+ - \theta_i^+ = \theta_i^- - \theta_u^- - \pi. \tag{27}$$

However, it is always true that average power input is equal to average power output and given by

$$P_{\rm dc} = V_{\rm dc} I_{\rm dc} = 3|U^+|\,|I^+|\cos(\theta_u^+ - \theta_i^+) + 3|U^-|\,|I^-|\cos(\theta_u^- - \theta_i^-). \tag{28}$$

The output dc voltage is proportional to the positive and negative sequence currents (magnitudes) so is the error signal $(V_{ref} - V_{\rm dc})$. In order to satisfy (26), the condition for second harmonic elimination, the positive and negative sequence commands for current magnitudes should satisfy (29) and (30):

$$|I^+| = K_p |U^+|(V_{ref} - V_{\rm dc}) \tag{29}$$

$$|I^-| = K_p |U^-|(V_{ref} - V_{\rm dc}). \tag{30}$$

Equations (29) and (30) represent positive and negative sequence magnitude commands. The positive and negative sequence commands for phase angles are derived from Fig. 2

$$\sin(\theta_u^+ - \theta_i^+) = \frac{Z|I^+|}{|U^+|}. \tag{31}$$

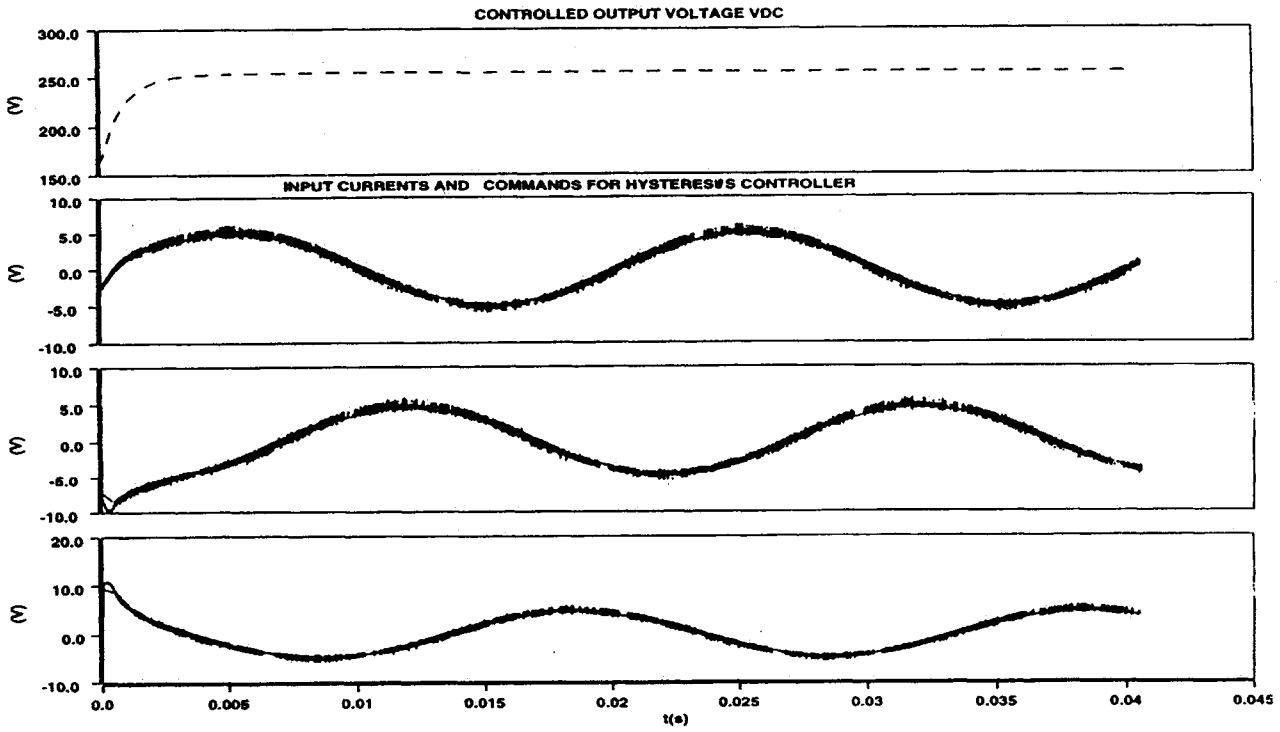

Fig. 6. Controlled output voltage, input currents, and commands for the hysteresis controllers (simulation results).

TABLE I
PARAMETERS USED IN SIMULATION

Parameter	Value	Parameter	Value
Input supply peak voltages	$U_1 = 100V$ $U_2 = 105V$ $U_3 = 104V$	DC-link capacitor, C	$100\mu F$
DC – link Reference voltage, V_{ref}	280V		
DC-link voltage, V_{dc}	270V	Output resistive load, R	100Ω
Input, L inductances	$1mH$	Fundamental frequency, f	50Hz
K_p	0.0096	K_{p1}	0.003

By combining equations (29) and (31) the following equation is obtained and given by

$$\sin(\theta_u^+ - \theta_i^+) = \frac{ZK_p\|U^+\|(V_{ref} - V_{\rm dc})}{|U^+|} = ZK_p(V_{ref} - V_{\rm dc}) = K_{p1}(V_{ref} - V_{\rm dc}). \quad (32)$$

Since high power factor is a desirable for the operation of the rectifier, the size of input inductor is small and equation (32) can be approximated by using Taylor series

$$\sin(\theta_u^+ - \theta_i^+) = (\theta_u^+ - \theta_i^+) - \frac{(\theta_u^+ - \theta_i^+)^3}{3!} + \frac{(\theta_u^+ - \theta_i^+)^5}{5!} - \cdots \quad (33)$$

$$\sin(\theta_u^+ - \theta_i^+) \approx (\theta_u^+ - \theta_i^+). \quad (34)$$

By combining equations (32) and (34) the positive phase angle commands are obtained and given by

$$\theta_i^+ = \theta_u^+ - K_{p1}(V_{ref} - V_{\rm dc}). \quad (35)$$

The negative sequence commands are derived in a similar way from Fig. 2

$$\sin(\theta_i^- - \pi - \theta_u^-) = \frac{Z|I^-|}{|U^-|}. \quad (36)$$

By combining equations (30) and (36) the following equation is obtained and given by:

$$\sin(\theta_i^- - \pi - \theta_u^-) = \frac{ZK_p|U^-|(V_{ref} - V_{\rm dc})}{|U^-|} = K_{p1}(V_{ref} - V_{\rm dc}). \quad (37)$$

By using the approximation shown above, equation (37) can be expressed as,

$$\theta_i^- = \theta_u^- + \pi + K_{p1}(V_{ref} - V_{\rm dc}). \quad (38)$$

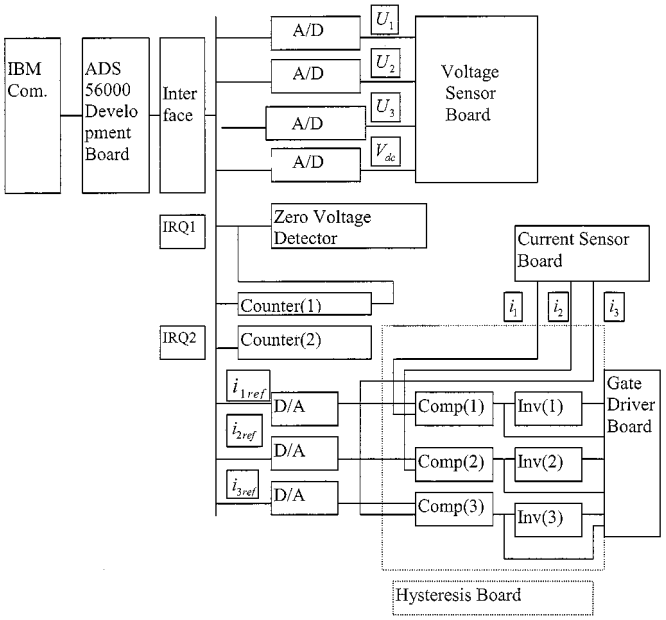

Fig. 7. Hardware configuration.

Equations (38) and (35) represent the phase angle commands.

Positive and negative sequence current commands are transformed to abc quantities and used as references for hysteresis controller. The transformation is given by

$$i_{1ref}(t) = |I^+|\sin(wt+\theta_i^+) + |I^-|\sin(wt+\theta_i^-) \quad (39)$$

$$i_{2ref}(t) = |I^-|\sin\left(wt+\theta_i^+ - \frac{2\pi}{3}\right) + |I^-|\sin\left(wt+\theta_i^- + \frac{2\pi}{3}\right) \quad (40)$$

$$i_{3ref}(t) = |I^+|\sin\left(wt+\theta_i^+ + \frac{2\pi}{3}\right) + |I^-|\sin\left(wt+\theta_i^- - \frac{2\pi}{3}\right). \quad (41)$$

Only two proportional controllers are utilized (one for the magnitude, the other for phase angle control) which has been determined to be sufficient for good regulation. An integral controller can be added to further reduce the steady state error. The proposed control method is shown in more detail in Fig. 5.

The unbalanced detector and symmetrical component calculator (block shown on Fig. 5) calculates the positive and negative sequence magnitudes as well as the phase shifts of input voltages. Based on the dc bus error and the positive and negative sequence components of three input voltages, magnitudes and phase angles of the positive and negative sequence reference currents are obtained. It is shown on Fig. 5 that the positive and negative sequence reference current magnitudes are calculated by using equations (29) and (30) whereas the positive and negative sequence reference current phase angles are calculated by using equations (35) and (38). Once the positive and negative sequence current commands are calculated, the block-Transform to abc is used to calculate the three phase (abc) quantities which

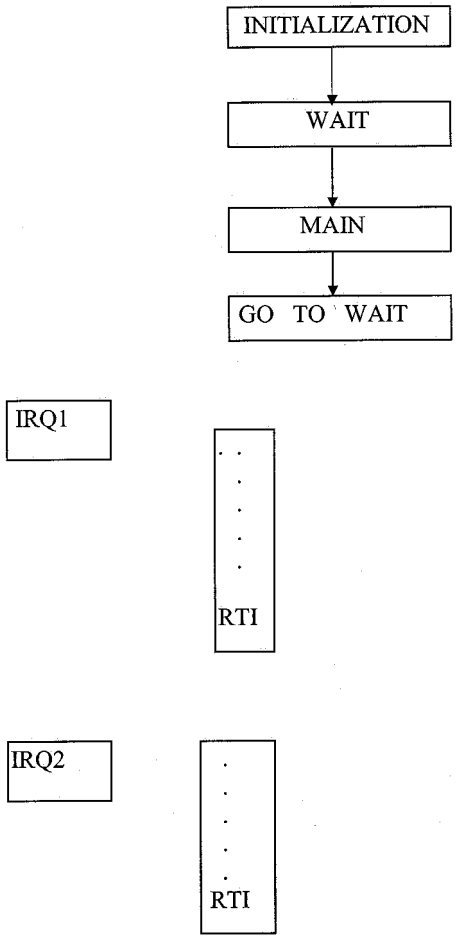

Fig. 8. Main structure of the program.

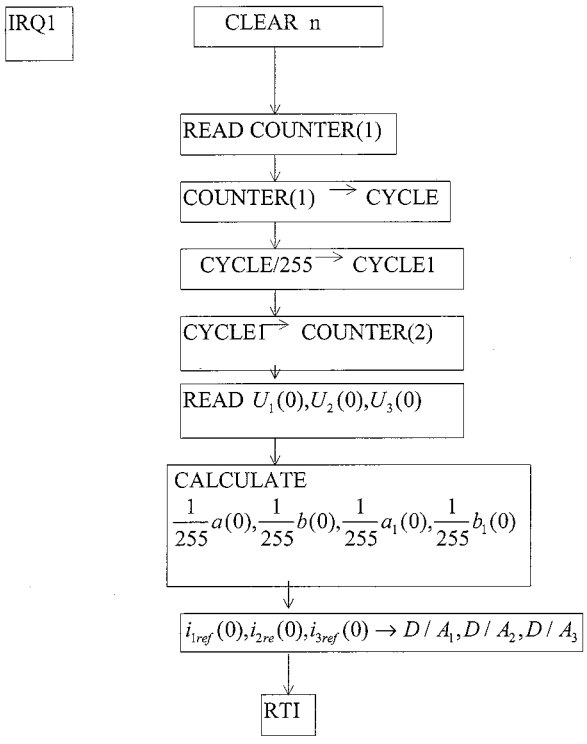

Fig. 9. Flowchart of interruption loop (IRQ1).

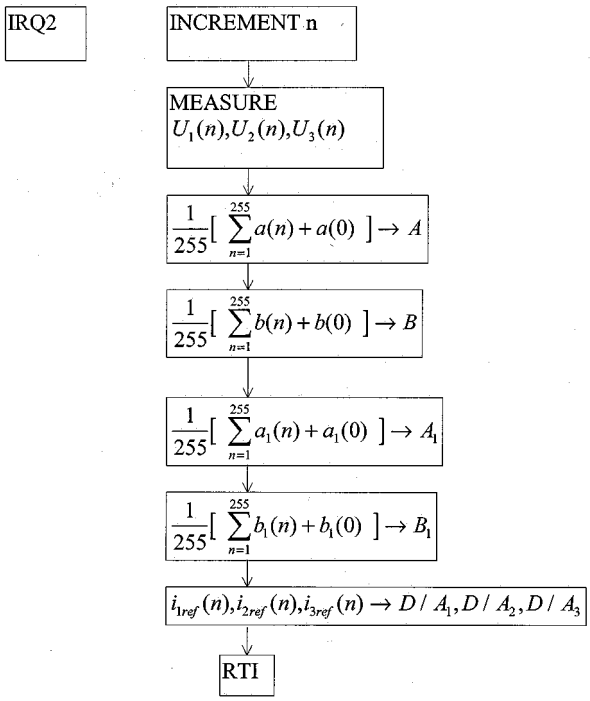

Fig. 10. Flowchart of interruption loop (IRQ2).

become reference signals for a hysteresis controller. The reference signals are compared with actual currents (block-hysteresis controller). The output of the hysteresis controller determines the control logic for the rectifier switches. Since the positive and negative sequence current commands are proportional to the dc bus error, the limiter has to be used to limit the current command value during transients when the error signal is large.

IV. Simulation and Experimental Results

In order to demonstrate feasibility, the system shown in Fig. 5 has been simulated in SABER. The parameters used for the simulation are shown in Table I. It is worth mentioning how the values of the parameters, K_p and K_{p1} are designed.

Parameter, K_p, is obtained from equation (29). The dc voltage steady state error is set to a maximum desirable value. The value for the input current is obtained from the power equation under the assumption that the input voltages are balanced. The maximum value of the input rms current that corresponds to the maximum power flow in the circuit is used in equation (29). For all other power levels, the steady state error is going to be smaller. The unbalance in input voltages will slightly affect a desirable dc voltage steady state error but this is not seen as a disadvantage especially in the situations when input unbalance is a temporary phenomenon.

Parameter, $K_{p1} = ZK_p$ [see equation (39)]. The values of K_p and K_{p1} are given in Table I.

The plot in Fig. 6 shows the controlled output dc voltage under unbalanced input voltages. It also gives the current commands for the hysteresis controller.

Good control of the dc voltage is evident in spite of the phase unbalance. A laboratory prototype was built to confirm the theoretical results. The bridge consists of six IGBT switches and

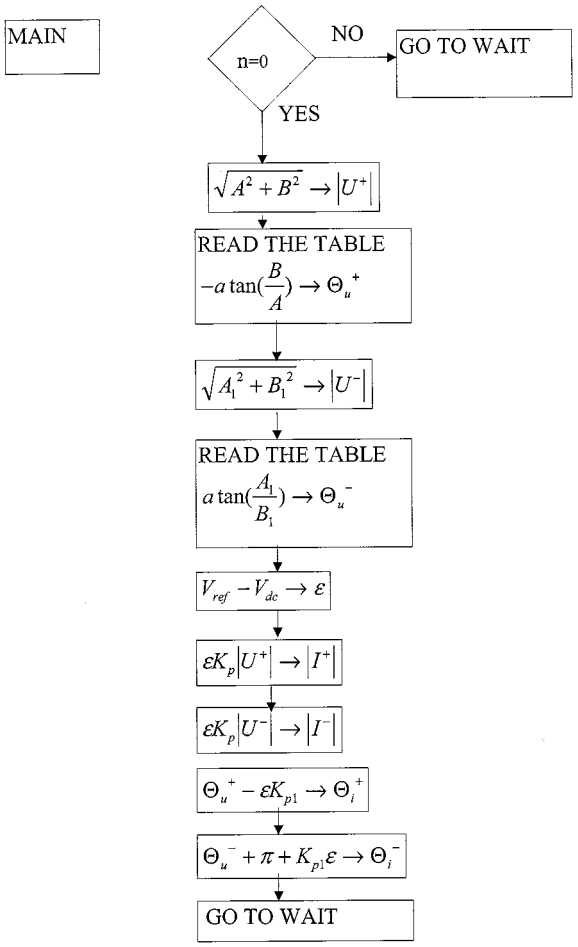

Fig. 11. Flowchart of the main loop (MAIN).

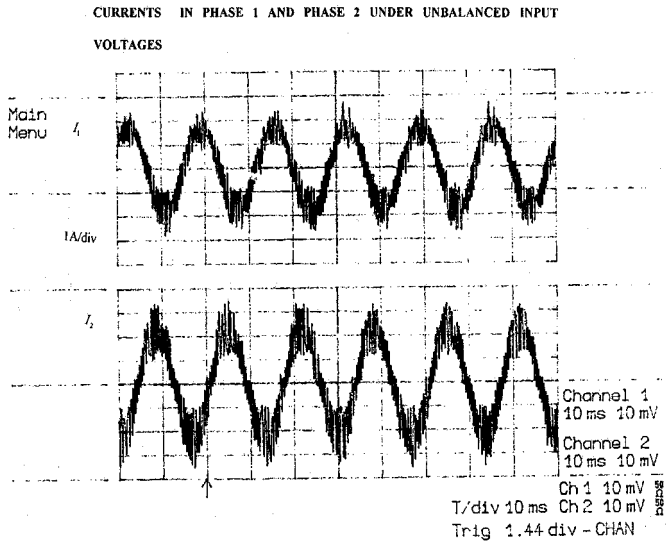

Fig. 12. Currents in phase 1 and 2 under unbalanced input voltages (experimental results).

six diodes connected in parallel. The control circuit consists of: voltage sensor board, current sensor board, hysteresis board, gate driver board and DSP56000 development system, as shown in Fig. 7. CPU runs at 27 MHz and is connected to an IBM personal computer. The zero voltage detector along with one

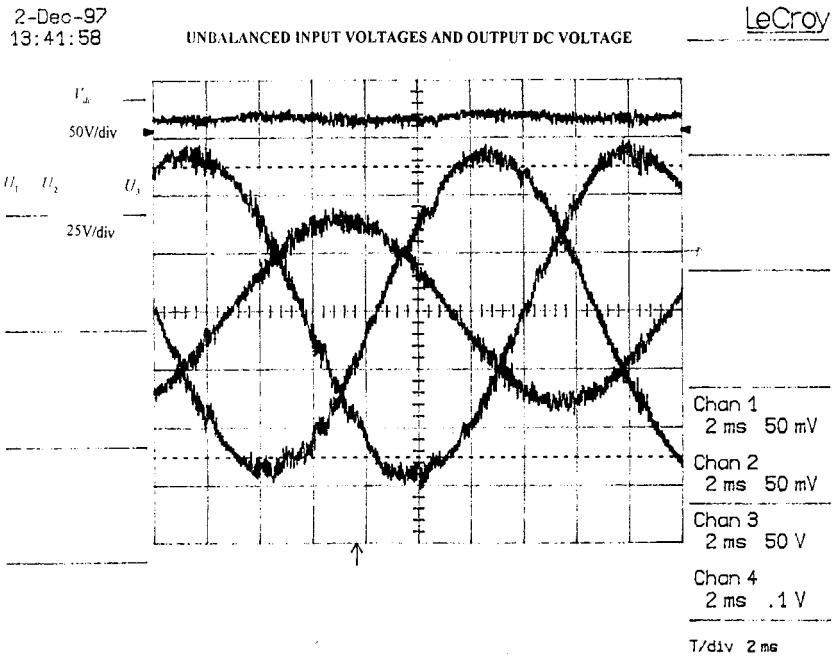

Fig. 13. Controlled output dc voltage and three input voltages (experimental results).

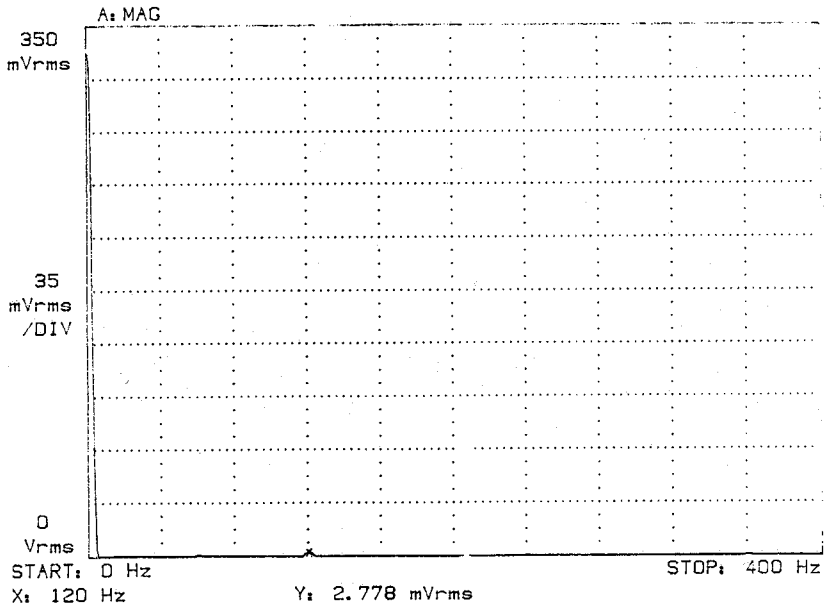

Fig. 14. Frequency spectrum of the output dc voltage (experimental results).

counter [counter (1)] which runs at 2 MHz, measures the frequency of the system and synchronizes the control functions (current commands) for D/A converters.

The output of the zero voltage detector, as shown in Fig. 7, is connected to the interrupt line (priority level 1) and to the gate of the counter. On the falling edge of the input signal, the output of the zero crossing detector, counter (1) stops counting. Since the program jumps into interrupt subroutine at that point (IRQ1), the second counter [counter (2)], which runs at 8 Mhz, gets loaded with the value measured by counter (1) divided by 255. In other words, the second counter is loaded by T/255 which represents the sampling time of the system. Since the frequency of the network may vary, the appearance of the second interrupt may vary accordingly. The hysteresis board consists of three comparators and three inverters. The inputs to the three comparators, as shown in Fig. 7, come from the current sensor board and the outputs of the D/A board. The software has been written in assembly language and consists of a main loop and two levels of interruption loops.

The main structure of the program is shown in Fig. 8. The first level of interruption loop (IRQ1) occurs once in a cycle. It detects the zero points of the input voltage. This subroutine sets the value in counter (2) to be T/255. It also reads the instantaneous values of the three input voltages and calculates variables necessary for calculating the sequence components of the three input voltages. At the end of this subroutine current commands

are sent to the D/A converter. Fig. 9 shows the simplified flowchart of the loop IRQ1. The second level of the interruption loop (IRQ2) occurs 255 times a cycle. It measures the input voltages and calculates variables necessary for calculating the sequence components. At the end of this subroutine, the commands for three input currents are sent to D/A converters. Fig. 10 shows the simplified flowchart of the loop IRQ2.

The main loop (MAIN) occurs once a cycle and calculates the sequence components of the three input voltages based on measurements and calculations performed in two interruption loops. It also measures the output dc voltage and calculates the error between its set and measured value. Finally, it calculates the sequence commands for the three input currents. Fig. 11 shows the simplified flowchart of the loop MAIN.

Experimental results are shown on Figs. 12–14. Fig. 12 shows input currents in phase 1 and phase 2 under unbalanced input voltages. The currents are unbalanced, as expected, to cancel the pulsating power coming from the input. The currents are sinusoidal and do not contain low-order harmonics. Fig. 13 shows the output dc voltage of the PWM Boost Type Rectifier under unbalanced supply voltages. Fig. 14 shows the frequency spectrum of the output dc voltage. Phase 2 is significantly unbalanced (by 50%) with respect to other two phases. In spite of the level of unbalance, the output voltage is smooth and contains no low order harmonics.

V. Conclusions

This paper proposes a new control strategy to improve the performance of the PWM Boost Type Rectifier under unbalanced operating conditions. An analytical solution for harmonic elimination under unbalanced input voltages and balanced input impedances is obtained. Based on analysis of the open loop configuration, a closed loop solution is proposed. With the proposed technique, high quality input and output waveforms are maintained under unbalanced input voltages and balanced input impedances. The simulation results show the excellent response and stable operation of the PWM Boost Type Rectifier under unbalanced operating conditions when this method is applied. The laboratory prototype has been designed to verify the discussions and analyses done in this paper. An excellent agreement occurs between the theoretical and experimental results.

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