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Optimised Space Vector Switching Sequences for Mutilevel Inverters

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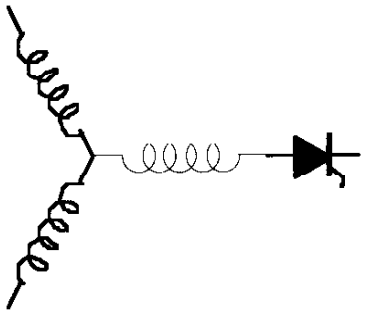

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Abstract **Previous work has shown that Space Vector modulation and Carrier modulation for 2 level inverters achieve the same phase leg switching sequences when appropriate zero sequence offsets are added to the reference waveforms for Carrier modulation. This paper presents a similar equivalence between the PD Carrier and Space Vector Modulation Strategies applied to Diode Clamped, Cascaded N-level or Hybrid multilevel inverters. By analysis of the time integral trajectory of the converter voltage, the paper shows that the optimal harmonic profile for a Space Vector Modulator occurs when the two middle Space Vectors are centred in each switching cycle. The required zero sequence offset to achieve this centring for an equivalent carrier based modulator is then determined. The results can be applied to any multilevel converter topology without differentiation. Discontinuous behaviour is also examined, with the Space Vector and Carrier based modulation methods shown to similarly produce identical performance. Both simulation and experimental results are presented.**

I. Introduction

Multilevel converters offer many benefits for higher power applications. In particular, these include an ability to synthesise voltage waveforms with lower harmonic content than two level converters and operation at higher DC voltages using series connected semiconductor switches.

While many different multilevel converter topologies have been proposed, the two most common topologies are the Cascaded Inverter and its derivatives [1][2], and the Diode Clamped inverter [3]. Figure 1 shows topologies for five level configurations of a Cascaded Inverter and a Diode Clamped Inverter. The two most popular control strategies for these multilevel inverter topologies are Carrier [4] and Space Vector (SVM) [5] modulation.

Carrier based modulation techniques control each phase leg of the inverter separately and allow the line to line voltage to be developed implicitly. For multilevel inverters, it is generally accepted that the Phase Disposition (PD) method [4] gives rise to the lowest harmonic distortion. This method was first applied to an N-level Diode Clamped converter, and arranges N-1 phase matched triangular carrier waveforms to fully occupy contiguous bands between $+V_{DC}$ and $-V_{DC}$. A single reference waveform for each phase is then compared against these carriers to determine how the phase leg should switch. Recent work has also shown how PD modulation can be applied to Cascaded Inverter structures to achieve the same harmonic performance [6].

In contrast SVM identifies each switching state of a multilevel inverter as a point in complex (α,β) space. Then a reference phasor rotating in the (α,β) plane at the fundamental frequency is sampled within each switching period, and the nearest three inverter switched states are selected with duty cycles calculated to achieve the same volt-

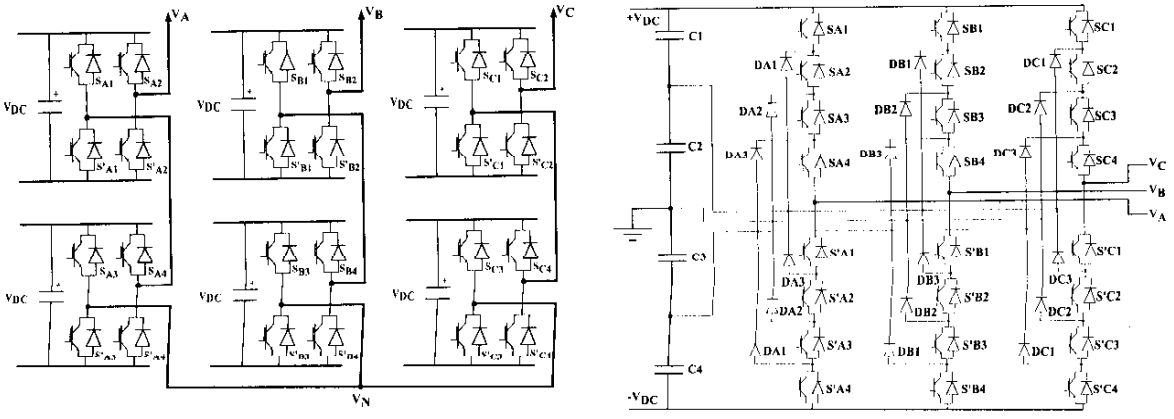


Figure 1: Five Level configurations of a (a) Cascaded Inverter, (b) Diode Clamped Inverter.

second average as the sampled reference phasor. This directly controls the inverter line to line voltages, and only implicitly develops the phase leg voltages. Recent work has shown how to do this calculation for a general N-level Diode Clamped inverter [5], but gives no insight into the optimal sequence of space vector states or the method's applicability to other multilevel inverter topologies.

Previous work has shown that Space Vector and Carrier modulation of two level converters produce identical space vector sequences despite their apparent differences [7]. This paper presents a similar equivalence for multilevel inverters by showing that the optimised SVM switching sequences for a multilevel inverter are the same as those created by Carrier PD modulation when an appropriate zero sequence component is injected into the carrier system references.

II. Optimised Space Vector Sequences.

Figure 2 shows the space vector diagrams for 3 and 5 level Diode Clamped systems, where each digit of the space vector identifier represents the voltage level to which the A, B and C phase legs are respectively switched. Note that some switched states are redundant and create the same space vectors. The difficult task of selecting the optimum set of these space vectors for a given reference phasor was recently solved by Celanovic et al. [5] using a linear coordinate transformation, and identified that the harmonic profile of the overall switched waveform is minimised when the nearest three space vectors are used. However, this solution does not identify how to sequence or place these three nearest space vectors in the (half carrier equivalent) switching period so as to minimise the total number of switching transitions and fully optimise the harmonic profile of the output voltage.

For a three phase inverter the minimum number of switch transitions in one switching cycle under continuous modulation is 3 (ie. one per phase leg), so that the converter cycles through 4 switched states in each switching period. At least the first and last of these must be a redundant space vector state if only the three nearest space vectors are to be used (eg. 101 – 201 – 211 – 212).

Depending where in the αβ space the reference phasor is located, there are two alternatives for this sequence, viz:

(i) Select two vectors of even redundancy and one vector of odd redundancy (eg. 211/100, 221/110 and 210), or:

(ii) Select one vector of even redundancy and two vectors of odd redundancy (eg. 211/100, 200 and 210).

(For two level inverters, only case (ii) is possible since the zero state vector is the only redundant switch combination.)

Figure 3 illustrates a subset of a 5 level Space Vector plot, and Table 1 summarises all possible sequences for this subset that achieve the required minimum of three switching transitions per phase leg in a switching period. Note that from two level SVM theory it is well known that these sequences should be reversed in the next switching cycle for minimum harmonic impact [7] and so the reverse sequences need not be explicitly considered.

For triangles (b) and (d) there is only one possible sequence. For triangles (a) and (c) the "correct" sequence can be identified from the possible alternatives by ensuring that no extra switching transitions occur when moving between triangles. For example, sequence c(i) should be used when moving from triangle (b) to (c) since it begins with the same state as the sequence in (b), or sequence c(ii) should be used when moving from triangle (c) to (d) since it begins with the same state as the sequence in (d). Within triangle (c) sequences c(i) and c(ii) must be swapped at some point, and this is most conveniently done when the duty cycle for the space vector {431/320} exceeds that of {421/310}.

Applying this principle to triangle (a) means that sequences a(i) and a(ii) cannot be used because they will introduce extra switching transitions when moving into

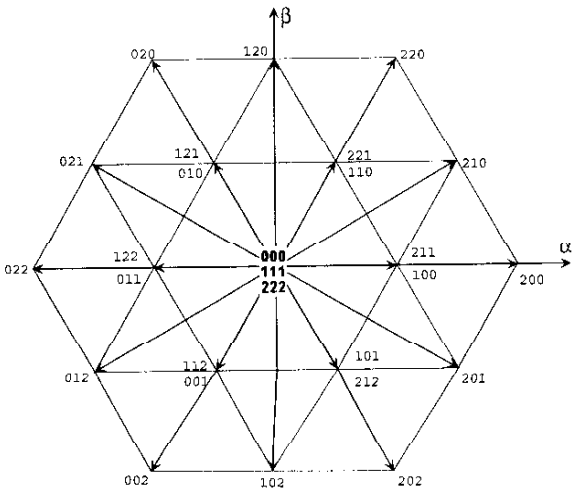


Figure 2(a): Space Vector States for 3 Level NPC converter.

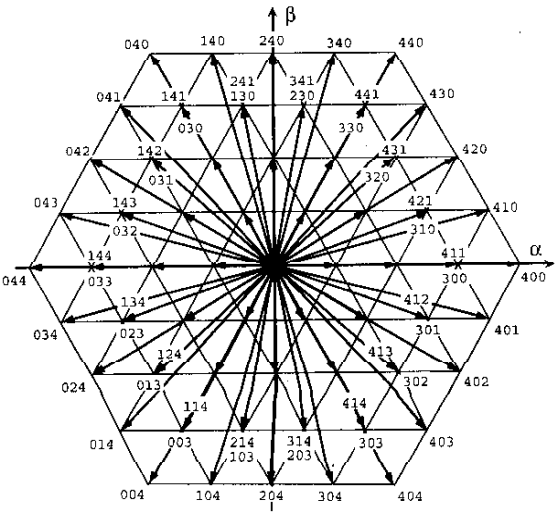


Figure 2(b): Space Vector States for 5 Level NPC converter.

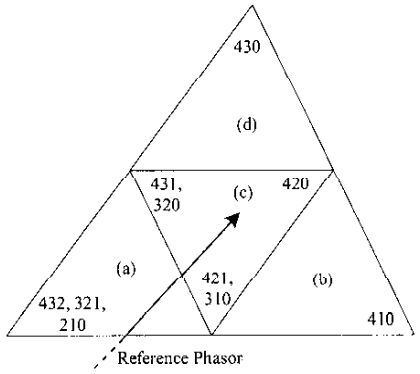


Figure 3 : Subset of 5 Level Space Vector Diagram. In triangles (a) and (c) 2 vectors of even redundancy and 1 of odd redundancy exist. In triangles (b) and (d) 1 vector of even redundancy and 2 of odd redundancy exist.

triangle (c). This is very important if the reference phasor lies near the boundary of triangles (a) and (c) because it will cross the linear boundary between triangles (a) and (c) twice in a fundamental cycle, and there are many type (c) triangles in the space vector plot. So only sequences a(iii) and a(iv) can be used, and these are identical to sequences c(i) and c(ii) except that state {420} has been replaced by state {321}. Hence only state {321} of the triply redundant vector {432/321/210} is useable.

Similar analysis for vectors with even redundancies greater than three reveals that only two states can ever be used to achieve minimal switching, and for vectors with odd redundancies greater than two, only one state is useable. Note also that all useful sequences begin and end with an even redundant space vector state.

While the above analysis is from the perspective of a Diode Clamped topology the only significant difference with the Cascaded topologies is that there is a greater variety of redundancies. A similar analysis for Cascaded type inverter systems leads to an identical restriction on states and sequences which can be used to achieve the minimum number of switching transitions in a fundamental cycle.

TABLE 1 : POSSIBLE SEQUENCES IN FIVE LEVEL SPACE VECTOR SUBSET (SEE FIGURE 3). REVERSE SEQUENCES ARE NOT SHOWN.

Triangle	Sequence	
(a)	(i)	{432 to 431 to 421 to 321}
	(ii)	{210 to 310 to 320 to 321}
	(iii)	{421 to 321 to 320 to 310}
	(iv)	{431 to 421 to 321 to 320}
(b)		{421 to 420 to 410 to 310}
(c)	(i)	{421 to 420 to 320 to 310}
	(ii)	{431 to 421 to 420 to 320}
(d)		{431 to 430 to 420 to 320}

III. Optimal Space Vector Position Within A Switching Period

Once the optimum switching space vector sequence for continuous modulation has been identified, it must be placed in each switching period to optimise the harmonic profile of the waveform. This means splitting the duty cycle of the first vector in the sequence (which is redundant with the last vector) across the first and last switching state, but just what fraction of time should be spent in each state? Fukuda et al. [10]proposed a technique for two level converters which when refined for multilevel systems answers this question.

Figure 4(a) shows the trajectory of the time integral of the converter output voltage (ie. flux) in $\alpha\beta$ space. The ideal trajectory is circular for a sinusoidal output voltage, but the switched nature of the converter operation restricts the real trajectory to a quasi-circular path as shown.

Figure (4b) shows the flux trajectories for one switching cycle. The switching sequence uses space vectors V_1, V_2 and V_3 with respective duty cycles d_1, d_2, and d_3. Vector V_1 is split so as to occupy the first and last state of the switching sequence with durations given by:

$$t_1 = kd_1\Delta T \qquad t_2 = (1-k)d_1\Delta T \tag{1}$$

where ΔT denotes the switching period.

The deviation between the switched quasi-circular trajectory and the ideal circular path at each switching cycle gives a measure of the harmonic distortion of the modulating process. This distortion can be evaluated by integrating the area between the two trajectories over each switching period as shown in Figure 4(c). (Note that for large pulse ratios the ideal trajectory can be approximated to a chord between end points p and p', to simplify the evaluation.) The issue then becomes to determine the value for k that minimises this area to achieve the optimum modulation strategy.

Figure 5 shows the optimum values for k for successive switching periods over a complete fundamental cycle, for a 3, 5 and 7 level inverter. These values were found from simulation by varying k within each switching period to minimise the flux error area. Clearly the optimal value of k varies insignificantly about the value 0.5, and so for the optimal harmonic performance the start and end redundant vector periods should be made equal.

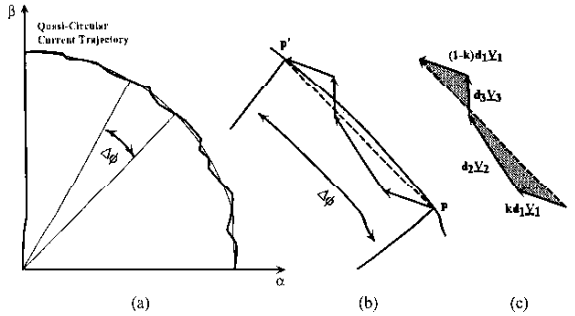


Figure 4: (a) Quasi-Circular Loci of the Flux Trajectories; (b) Flux Trajectories in one switching cycle; (c) Area between the nearest three space vectors and the approximated Ideal Flux trajectories.

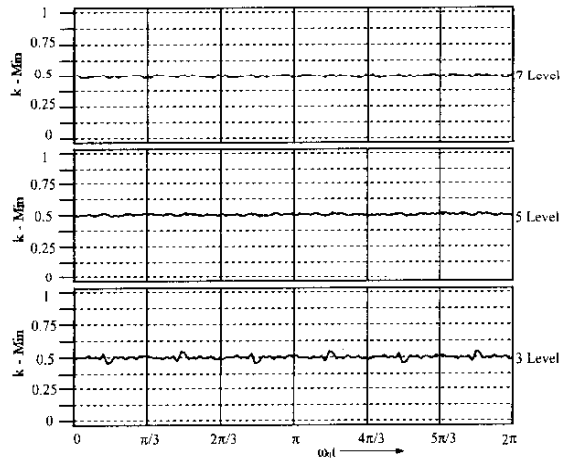


Figure 5: Value of k which gives Minimum Vector Area for a pulse ratio of 120, Modulation Depth of 0.8.

IV. SVM Compared to Carrier Based PWM.

For 2 level inverters, it is known [7] that the addition of a common offset voltage to the three phase references, of

$$V_{off} = -\frac{\max(Va,Vb,Vc)+\min(Va,Vb,Vc)}{2} \qquad (2)$$

will centre the active space vectors in the switching period, and hence match carrier modulation to optimised SVM.

Figure 6 shows the converter switching states which result when this offset is used for a 5 level system operating under PD modulation. For the expanded switching condition shown, the sequence consists of two vectors of even redundancy (V_1 and V_3) and one vector of odd redundancy (V_2). Examination of this sequence shows that the durations of the two states of V_1 are not equal, but rather centre the vector of odd redundancy in the middle of the half carrier period. Hence this offset will not achieve the optimum of

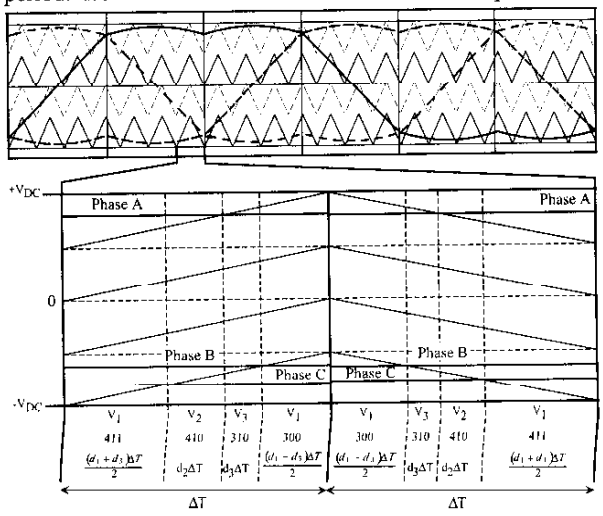


Figure 6: Space Vector Positions resulting from 2 level SVM common mode offset. The effect is to centre the Vector with odd redundancy (V_2), rather than making equal dwell times in the states of V_1.

centring the two middle vectors of the switching sequence.

The limitation with (2) is that it assumes that the first and last switching transition in the each switching period is determined by the comparison of the absolute maximum and minimum reference values against the carrier. This is not necessarily the case for a multilevel inverter. For example, Figure 6 shows that the last switching transition in the first half carrier period is caused by the comparison of V_b reference against the carrier, and this is the middle reference value. Hence to proceed it is necessary to identify which of references Va, Vb or Vc will be responsible for the first and last switching transitions in each half carrier period.

This can be done using a modulus function to vertically shift the (2 level optimised) reference voltages so their carrier intersections lie within a common carrier band, ie.

$$V_k' = \left(V_k + V_{off} + V_{DC}\right) \bmod \left(\frac{2V_{DC}}{N-1}\right), \quad k = a,b,c \qquad (3)$$

Note that a DC offset must be added to the reference waveforms to avoid the modulus function operating on a negative number. An additional common mode voltage which correctly positions the first and last switching transitions in each switching period can then be determined using a similar max/min expression as before, viz

$$V_{off}' = \frac{V_{DC}}{N-1} - \frac{\left(\max(V_a',V_b',V_c')+\min(V_a',V_b',V_c')\right)}{2} \qquad (4)$$

The final reference waveforms are then generated by adding the offset voltages described by (2) and (4) to the original sinusoidal phase voltages. Figure 7 shows the offset and phase voltages for 3, 5 and 7 level systems, which closely match results obtained by other authors [8], [9].

V. Discontinuous Modulation

A further possibility with space vector positioning is to move to discontinuous SVM by eliminating either the first or last state in each switching sequence. While this approach does not achieve a minimum flux error, the increase in

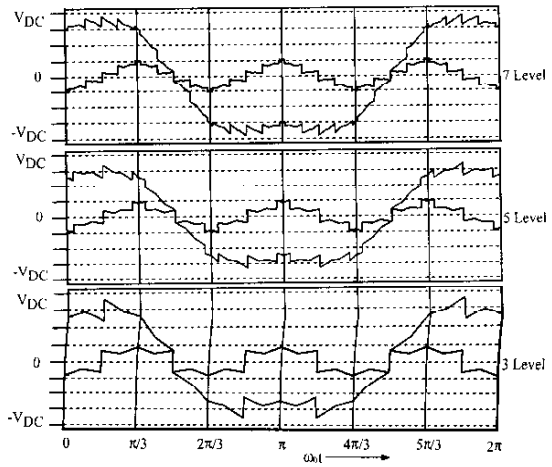


Figure 7: Centred SVM Reference and Offset Waveforms.

switching frequency of 3/2 that is possible because of the reduced number of switching transitions that are required, can give harmonic benefits for certain modulation ranges.

The simplest approach for discontinuous modulation is to lock particular phase legs to the upper or lower voltage rails for fractions of the fundamental cycle. For multilevel inverters, this may require additional switching transitions which reduce the possible increase in switching frequency from the theoretical maximum, but there are still useful harmonic gains to be achieved. (Note that for multilevel inverters, the increased number of voltage levels does create a greater variety of possible modes of discontinuity, but it has been found that all have similar harmonic profiles and so only the simplest alternative will be considered here.)

Figure 8 shows the zero sequence offset waveforms which should be added to the phase reference voltages to achieve discontinuous switching for a carrier based modulation system. These reference waveforms are immediately familiar as the DPWM1 and DPWM3 waveforms described in earlier work [11], and can be described mathematically as:

$$V_{off} = \max[abs(Va), abs(Vb), abs(Vc)], \quad V_{ZS\_DPWM1} = -\text{sgn}(Voff) + Voff \quad (5)$$

$$V_{off} = mid[abs(Va), abs(Vb), abs(Vc)], \quad V_{ZS\_DPWM3} = -\text{sgn}(Voff) + Voff \quad (6)$$

Alternatively, as was done for this paper, these offset waveforms can be developed by demodulating the phase voltages implicitly developed by a discontinuous implementation of a multilevel SVM system.

VI. Simulation and Experimental Results.

The modulation principles presented above have been verified both in simulation, and experimentally with a 3 and 5 level Cascaded inverter and a 7 level Hybrid inverter (with only two phase legs in each case). Each phase leg for the experimental system comprised 2 series connected full bridge single phase inverter modules, with DC buses supplied from tapped transformers to allow different bus voltages to be created for the Cascaded and the Hybrid inverter systems.

Previous work has reported how PD modulation can be implemented for the Cascaded and Hybrid inverter systems [6],[12] and this will not be discussed further here. But in passing it should be noted that the modulus function can be efficiently implemented experimentally by scaling the calculation in (3) to make the divisor a power of 2, and then simply masking the dividend with the divisor minus one.

Figure 9 shows the simulated spectrum of a 3 level inverter operating under centred SVM. Figures 10 and 11 show experimental results for PD modulation of a 3 level Cascaded inverter, with the appropriate zero sequence offsets added to the phase references to make the start and end redundant space vector periods equal. The extremely close match of the simulation and experimental results confirms the equivalence of SVM and PD Carrier modulation when an appropriate zero sequence offset is added to the reference waveforms.

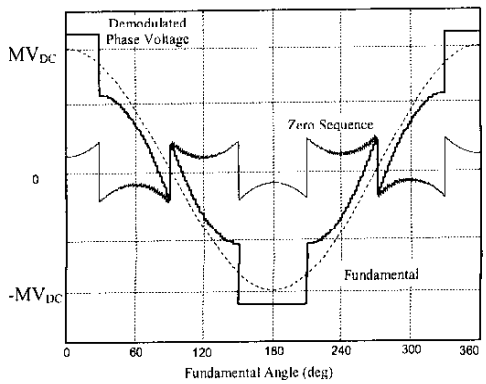
Similar results have been obtained for a 5 level inverter system, but are not presented here because of space limitations.

Figures 12, 13 and 14 show similar results for a 7 level PD modulated hybrid converter compared to 7 level centred SVM. Again, the extremely close match of the simulated and experimental spectra confirm the equivalence between SVM and PD carrier modulation for any multilevel converter topology, when appropriate zero sequence offsets are added to the carrier system phase reference waveforms.

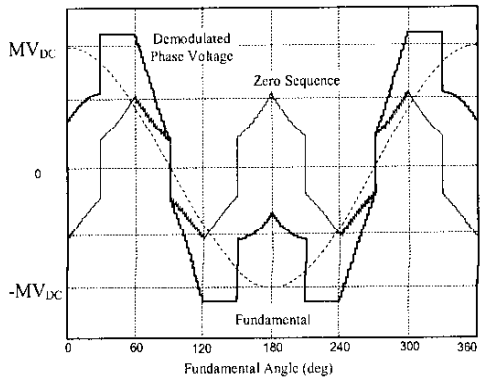
Figures 15, 16 and 17 compare 3 level SVM simulation results against 3 level Cascaded inverter PD modulation under 30° discontinuous operation (once more with the appropriate zero sequence offsets added for the PD modulation). Once again, the extremely close match of the simulation and experimental spectra confirm the equivalence between the two modulation strategies. Note also the characteristic low order extended spectral "tail" in Figures 15 and 16, and the low order distortion in the experimental system because of sector commutation, which is a typical signature of discontinuous modulation strategies.

VII. Conclusion.

It is already well established for 2 level inverters that Carrier and Space Vector modulation methods create exactly



(a) Three Level 60° Discontinuous SVM



(b) Three Level 30° Discontinuous SVM.

Figure 8: SVM Demodulated Phase Voltages for discontinuous modulation. Pulse Ratio = 200.

the same phase leg switching sequences when appropriate zero sequence offsets are added to the reference waveforms for Carrier modulation. This paper identifies a similar equivalence for PD Carrier modulation and Space Vector Modulation for Diode Clamped, N-level Cascaded and Hybrid multilevel inverters. Using flux trajectory concepts, it has been shown that the optimum switching arrangement maintains the middle space vectors of a switching sequence centred within each switching period. The required zero sequence component to achieve this result for a carrier based modulator is then determined, with the results being applicable to any multilevel inverter topology.

The paper also shows how discontinuous modulation can be applied to multilevel inverters using zero sequence offset voltages derived from 2 level inverter Space Vector concepts.

Both simulation and experimental results are presented to support the conclusions of the paper.

VIII. References.

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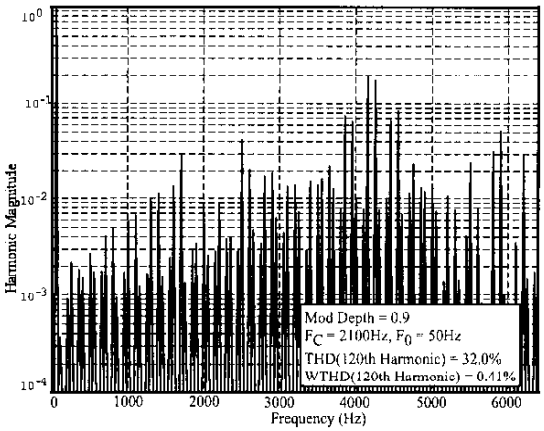

Figure 9: 3 Level Centred SVM – Simulated Line to Line Voltage Spectrum.

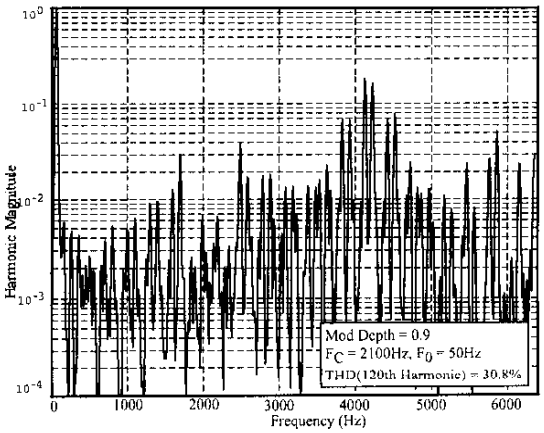

Figure 10: 3 Level Cascaded Inverter – Centred PD Modulation, Experimental Line to Line Voltage Spectrum.

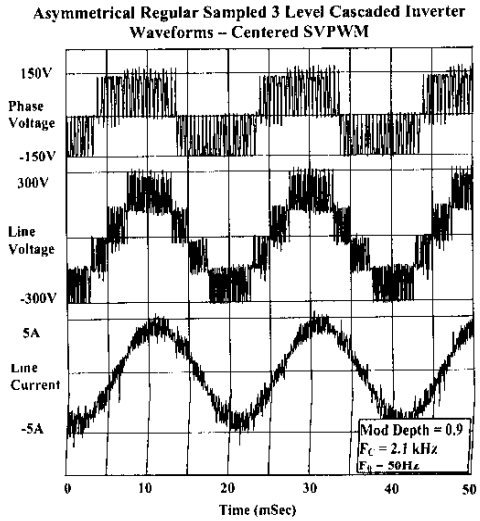

Figure 11: 3 Level Cascaded Inverter – Centred PD Modulation. Experimental Switched Inverter Waveforms.

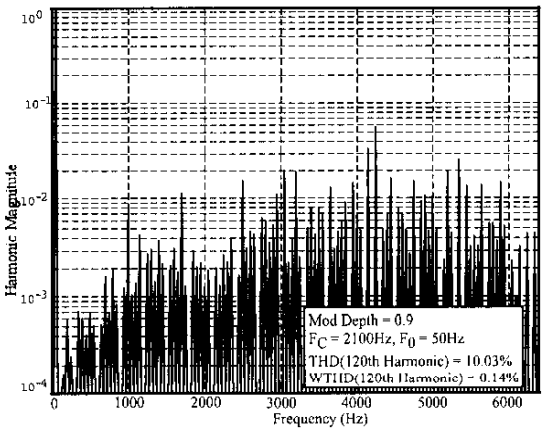

Figure 12: 7 Level Centred SVM – Simulated Line to Line Voltage Spectrum.

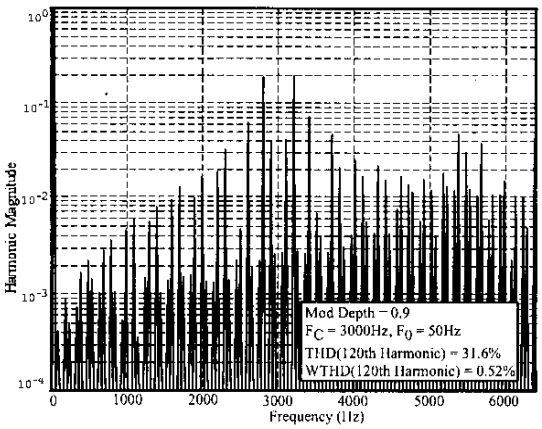

Figure 15: 3 Level 30° Discontinuous SVM – Simulated Line to Line Voltage Spectrum.

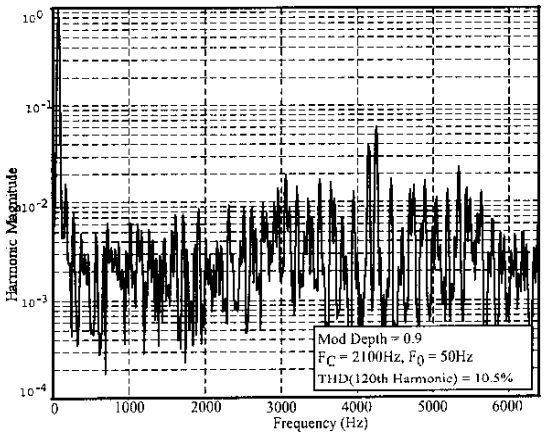

Figure 13: 7 Level Hybrid Inverter – Centred PD Modulation, Experimental Line to Line Voltage Spectrum.

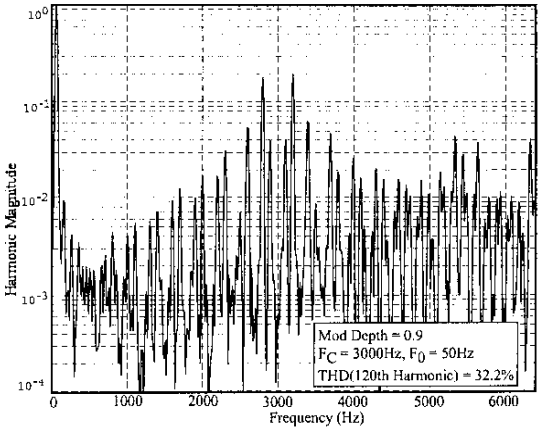

Figure 16: 3 Level Cascaded Inverter - 30° Discontinuous PWM . Experimental Line to Line Voltage Spectrum.

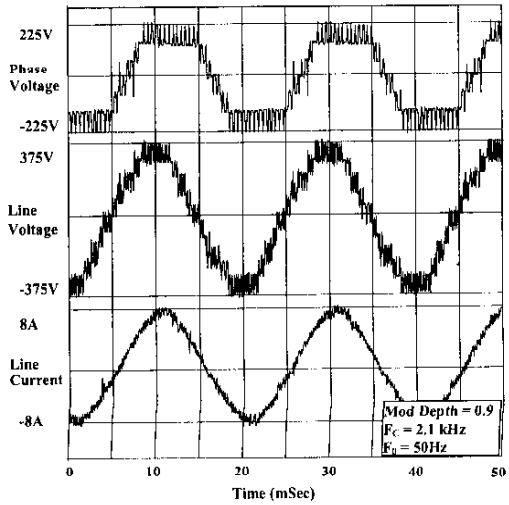

Figure 14: 7 Level Hybrid Inverter – Centred PD Modulation. Experimental Switched Inverter Waveforms.

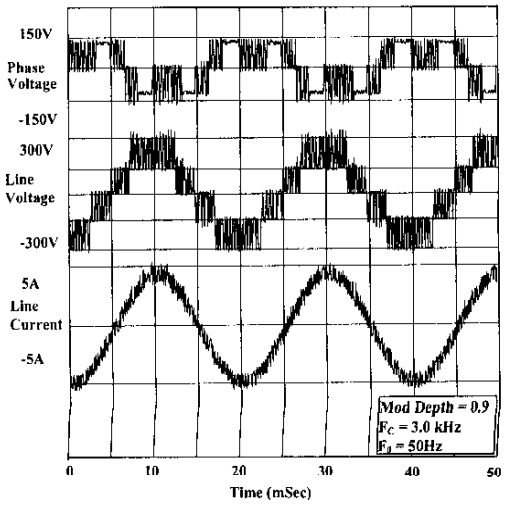

Figure 17: 3 Level Cascaded Inverter – 30° Discontinuous PD Modulation. Experimental Switched Inverter Waveforms.