Matrix Converter Topologies With Reduced Number of Switches

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***Abstract*– A direct AC-to-AC converter commonly termed a matrix converter has a simple structure and many attractive features. However, the complexity of its conventional PWM strategy is prone to commutation failure, which is a factor that keeps it from being utilized in industry. This paper focuses on several alternative dual-bridge matrix topologies which do not possess this problem. First, these converters have the same characteristics as a conventional matrix converter, such as four-quadrant operation, unity input power factor, no dc-link capacitor, and high quality voltage/current waveforms. Second, the number of switches can be reduced thus reducing the cost. Third, the switches on the line side can turn on and off at zero current, they do not have any difficult commutation problems. Lastly, the complexity of the clamp circuit in these topologies can be greatly simplified thereby further reducing the cost. This paper introduces several topologies with reduced number of switches and analyzes the characteristics of this converter family. Simulation and experimental results of a 9-switch topology are provided to verify its feasibility.**

I. INTRODUCTION

The matrix converter, Fig. 1, first introduced in 1979 [1], has experienced a resurgence of attention recently. Its main advantages are adjustable (including unity) power factor, bi-directional power flow, high quality waveform, and the possibility of a compact design due to the lack of large energy storage components. However, this topology has not yet been widely adopted in industry. One reason is that the conventional modulation algorithm of Venturini and Alesina [2] involves an involved and difficulty to implement PWM switching strategy. A complicated commutation scheme and an elaborate clamp circuit typically must be added for safe operation [3].

An alternative dual bridge matrix converter topology in Fig. 2 can be used to avoid above disadvantages. The reason this topology is also named a matrix converter is that, it shows the same input/output performance as conventional matrix converter and can also be described by switching matrices similar to the conventional matrix converter. Several papers have been published to illustrate this topology. In [4],[5] the circuit was used to explain the space vector PWM (SVPWM) of the conventional matrix converter. In contrast, [6]~[10] propose a similar topology based on dual-bridge model. In [6], this topology is treated as a rectifier/inverter, in which line side and load side switches are controlled separately. In [7], this topology is called direct frequency changer (DFC); the zero current commutation of line side switches is proposed. References [8]-[10] begin to treat this topology as a type of matrix converter, In these papers, detailed PWM control method is proposed with synchronized switching of both the line and load side switches. Zero current commutation of line side switches is also analyzed. Refs. [6]-[8], utilize the 18-switch topology of Fig. 3. References [9] and [10] propose several topologies with a reduced number of switches.

Compared to conventional matrix converters, the dual bridge matrix converter has following advantages:

- The difficulty of commutation is reduced. All line side switches turn on and off at zero current and all load side switches commutate similar to a conventional DC/AC inverter.
- The number of switches can be reduced under certain constraints.
- The clamp circuit can be greatly simplified, only one capacitor and one diode are used.

This paper focuses on variations of the alternative dual bridge matrix converter topology. After a brief presentation of its input/output transform equations, several topologies with reduced number of switches are discussed. An 18 and a 15-switch topology is derived for four-quadrant operation and 9-switch and a 12-switch topology are obtained for uni-directional power flow. Meanwhile, a clamp circuit using only one single diode and capacitor is introduced and its operation is discussed. Both the commutation principle and PWM control methods for these topologies are analyzed. Finally, simulation and experimental results of a 9-switch dual-bridge matrix converter are provided to verify its feasibility.

II. DERIVATION OF DUAL BRIDGE MATRIX CONVERTER

Considering the conventional matrix converter topology in Fig.1. If the switching function of a switch, S_k in Fig.1 is defined as '0' when open and '1' when closed, the output voltage of this converter is directly obtained in (1). Here j∈ {a,b,c} and k∈ {u,v,w}.

$$\begin{bmatrix} V_{su} \\ V_{sv} \\ V_{sw} \end{bmatrix} = \begin{bmatrix} S_{au} & S_{bu} & S_{cu} \\ S_{av} & S_{bv} & S_{cv} \\ S_{aw} & S_{bw} & S_{cw} \end{bmatrix} \cdot \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \qquad (1)$$

For balanced three-phase condition, the three-phase line voltage follows a constraint equation as in (2).

$$V_{sa} + V_{sb} + V_{sc} = 0 \tag{2}$$

Thus, (1) can be reduced to a two dimensional equation such that two additional points (*p*, *n*) can be introduced to replace Eq. (1), where

$$\begin{bmatrix} V_{su} \\ V_{sv} \\ V_{sw} \end{bmatrix} = \begin{bmatrix} S_{up} & S_{un} \\ S_{vp} & S_{vn} \\ S_{wp} & S_{wn} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_n \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} V_p \\ V_n \end{bmatrix} = \begin{bmatrix} S_{ap} & S_{bp} & S_{cp} \\ S_{an} & S_{bn} & S_{cn} \end{bmatrix} \cdot \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{4}$$

The dual bridge matrix converter in Fig. 2 is derived directly from Eqs. (3) and (4).

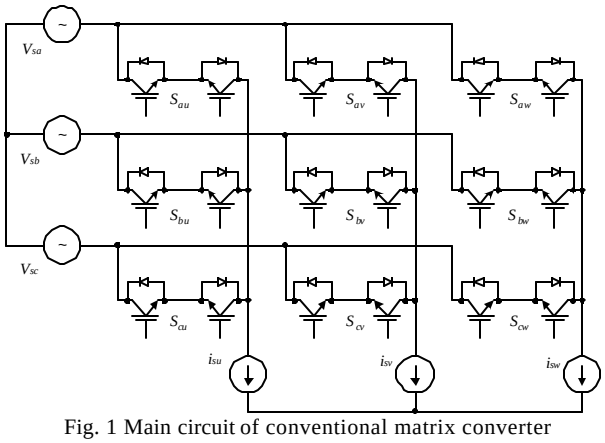


Fig. 1 Main circuit of conventional matrix converter

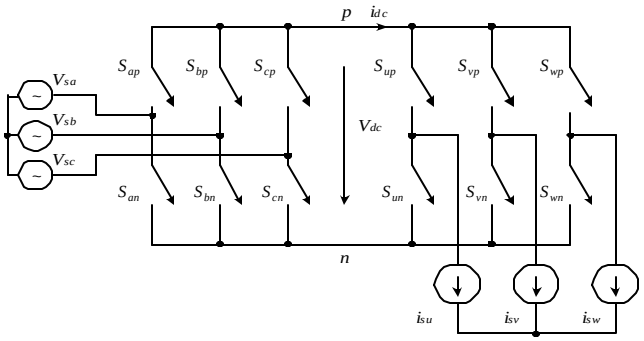


Fig. 2 Alternative matrix converter topology

III. STEPS TO REDUCE THE SWITCH NUMBER

In general, the 12 ideal switches in Fig. 2 requiring, in principle, 24 uni-directional current conducting, bi-directional voltage blocking switches can be implemented in a number of simpler realizations by appropriate assumptions. For example, if V_p is always higher than V_n, the bi-directional switches on the load side can be replaced by uni-directional voltage blocking switches as shown in Fig. 3. In this case, the topology of [5], [6], and [7] is realized.

Figure 4 (a) shows the equivalent circuit of input side phase leg "a". Noting that the switches S_{app} and S_{anp} can share the same gate drive signal. These two switches can be replaced by one single switch and two clamp diodes. As a result, a 15-switch topology is developed as shown in Fig. 4 (b)[9][10]. Compared to the 18-switch topology, this circuit possesses the same performance measures such as four-quadrant operation, low harmonic content and unity power factor. The primary difference is that, when current i_{dc} is positive, its conduction losses for the line side switches are higher than the 18-switch topology.

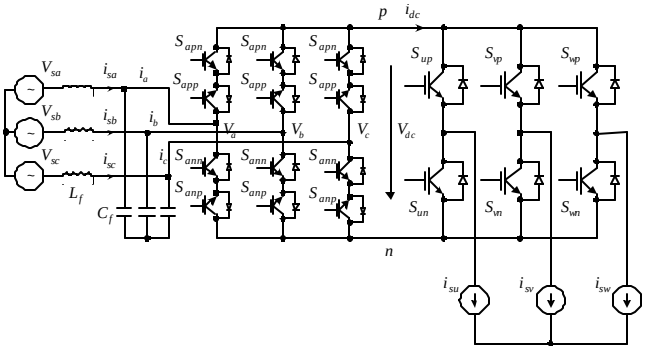


Fig. 3 Topology with 18 uni-directional voltage blocking switches

If the condition that link current $i_{dc} \geq 0$ is guaranteed, the number of switches can be further reduced. If the 18-switch topology in Fig. 3 is analyzed in detail, a 12-switch topology can be derived as shown in Fig. 5 (a). In this case, a standard current source inverter (CSI) and a voltage source inverter (VSI) connect directly to each other. By appropriate PWM modulation, the DC side current i_{dc} is determined by the three-phase output current and the DC side voltage V_{dc} is obtained by the three input voltages.

From Fig. 4 (b), it can also be determined that no current flows through S_{jp} and S_{jn} (j∈a,b,c) and only the three intermediate switches are conducting. Thus, a 9-switch topology can be obtained as shown in Fig.5 (b). Generally, both the 9-switch and the 12-switch topologies show the same performance except that the 9-switch topology has somewhat larger conduction losses than the 12-switch topology.

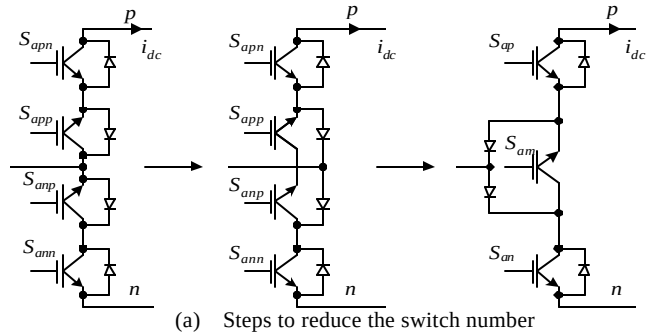
Because the 9-switch and 12-switch topologies can only be used when i_{dc} is greater than or equal to 0, the power through these two topologies can only flow from the line side to the load side. In order to ensure positive dc current flow with three-phase sinusoidal output current, it can be shown that the power factor on the load side should always be higher than 0.866. As a result, the application of these topologies is somewhat limited but suitable, for example, for permanent magnet motor drives.

IV CLAMP CIRCUIT

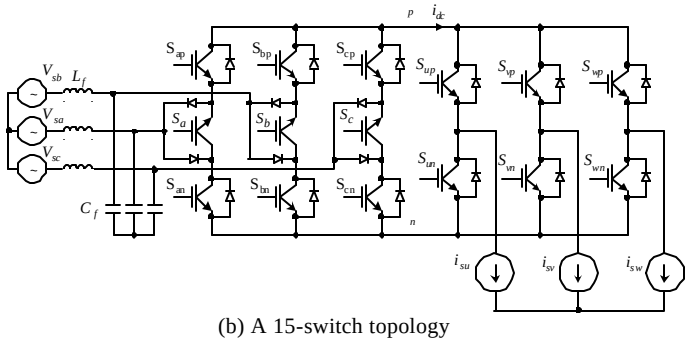
The clamp circuit is an important component for both conventional and dual-bridge matrix converters. Under normal condition, the main use of this circuit is to provide a path for the commutation energy stored in the load (motor) leakage inductance. Under a faulted condition, all switches in the converter are immediately turned off so that the clamp serves to de-energize the load current without damaging the power switches. Generally, the clamp circuit of a conventional matrix converter consists of dual six-pack diode rectifiers and one capacitor [3]

Compared to the conventional matrix converter, the clamp circuit of dual-bridge matrix converter is much simpler. A clamp circuit with only one diode D_c and one capacitor C_c is introduced in a 9-switch topology in Fig. 6 (Note: it can also be used for all the other topologies proposed previously). The operation of this circuit is shown below:

- When the converter is started, all the switches in the line side turn on initially and the clamp capacitor voltage is charged up to the maximum peak line voltage.
- Under normal operation, the clamp capacitor voltage is higher than V_{dc}. Hence, the clamp diode is reverse biased and this clamp circuit does not operate.
- Under a fault state, all switches in the converter are turned off immediately. The energy stored in the inductive load flows into the clamp capacitor to avoid high voltage spikes.

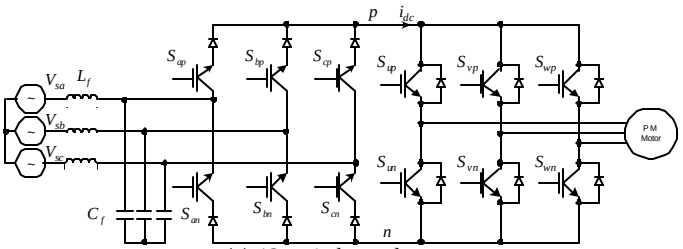


(a) Steps to reduce the switch number

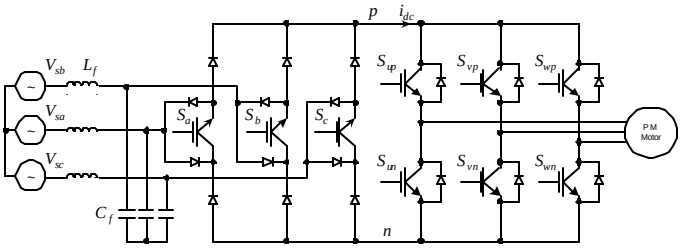


(b) A 15-switch topology

Fig. 4 Reduction of switch number from 18 to 15



(a) 12-switch topology



(b) 9-switch topology

Fig. 5 Reduction of switch number to 9 or 12

The clamp capacitor should be carefully selected to eliminate over-voltage as well as to reduce its size. The calculation of its value is the same as the conventional matrix converter. The appropriate value depends on the load current, the load inductance, and the highest allowable capacitor voltage. A detailed design scheme of conventional matrix converter can be found in [3].

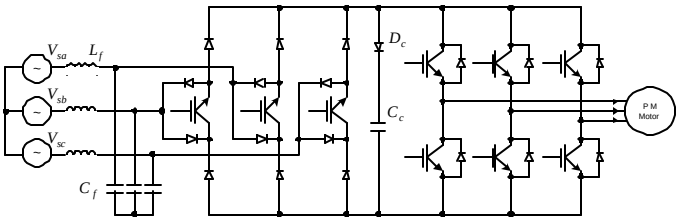


Fig. 6 The 9-switch topology with clamp circuit

V. COMMUTATION AND PWM CONTROL SCHEME

In the following chapters, the PWM control of the 18-switch topology will be discussed. For the other topologies, the same control philosophy can be obtained by selecting its switching states appropriately.

In order to simplify the analysis, it is assumed that there is no input filter on the line side. Hence, from Fig.3:

$$L_f = 0;\ C_f = 0;\ V_{sx} = V_x;\ i_{sx} = i_x;\ x = a, b, c$$

It is assumed that the input source voltages are described by

$$\begin{cases} V_{sa} = V_m \cos\theta_a = V_m \cos(\omega_i t) \\ V_{sb} = V_m \cos\theta_b = V_m \cos(\omega_i t - \dfrac{2\pi}{3}) \\ V_{sc} = V_m \cos\theta_c = V_m \cos(\omega_i t + \dfrac{2\pi}{3}) \end{cases} \quad (5)$$

and the output currents are

$$\begin{cases} i_{su} = I_o \cos\theta_{oi} = I_o \cos(\omega_o t + \varphi_o) \\ i_{sv} = I_o \cos(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\ i_{sw} = I_o \cos(\omega_o t + \varphi_o + \frac{2\pi}{3}) \end{cases} \quad (6)$$

where ω_i and ω_o are the input and output angular frequencies, φ_o is the initial phase angle of the phase current. V_m and I_o are the amplitudes of input voltage and output current respectively.

A. S*ix switching intervals based on line side voltage*

Six intervals can be identified based on detection of the input voltage synchronization angle. During each interval, only one of the three-phase input voltages has the largest absolute value (see Fig. 7). For example, V_{sa} has the largest absolute voltage in interval 1, and V_{sc} has the largest absolute voltage in interval 2 and so forth.

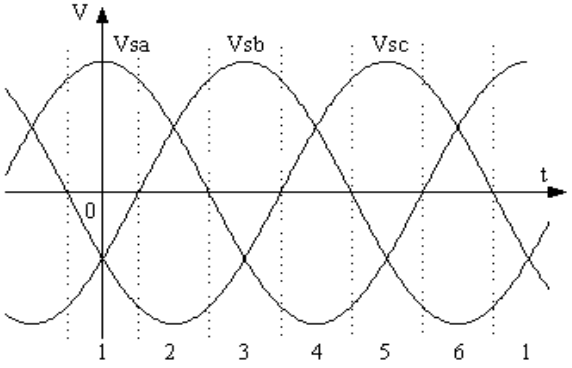


Fig. 7. Six intervals of a switching cycle

B. *Two portions in each switching cycle*

Each of the switching cycle is split into two portions. In each portion, the switching state of line side switch is fixed and the DC side voltage V_{dc} equals to one of the two highest positive line voltages.

For example, V_{sc} in interval 2 has the largest absolute voltage, the two largest positive line voltages are V_{sa} -V_{sc} and V_{sb} -V_{sc} respectively. The line side switching states in each portion can be determined by the following:

- In portion 1, S_{bpp}, S_{bpn}, S_{cnp}, and S_{cnn} remains turned on; all other line side switches remain turned off. The DC side voltage V_{dc} is then equal to V_{sb} -V_{sc}, the DC side current i_{dc} equals i_{sb} and $-i_{sc}$, and i_{sa} equals zero. The duty cycle of this portion is defined as $d_{bc.}$
- In portion 2, S_{app}, S_{apn}, S_{cnp}, and S_{cnn} remains turned on; all other line side switches remain turned off. The DC side voltage V_{dc} equals V_{ab} -V_{sc}, the DC side current i_{dc} equals i_{sa} and $-i_{sc}$, and i_{sa} equals zero. The duty cycle of this portion is defined by $d_{ac.}$

Figure 8 shows the equivalent circuits of the converter during these two portions of interval 2. The switching can be considered as an equivalent DC/AC inverter with different DC voltages in during each of the two portions.

Table. I show the switch states and DC voltages during the two portions for all six intervals. The same equivalent DC/AC inverter concept with different DC voltages remains valid for all six intervals.

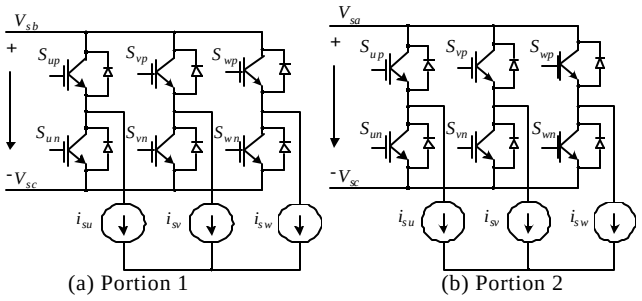


Fig. 8. Equivalent circuit in interval 2

C. *Commutation of the converter*

Because the converter is considered as a DC/AC inverter during each portion of each interval, switch commutation issues are largely simplified. (a) The commutation of load side switches become the same as a conventional DC/AC inverter; (b) Because the line side switches commutate only at the transition between adjacent portions, by setting zero voltage vector to occur at both the beginning and ending of each portion, the line side switch commutates at zero current. Thus, no overlap time is needed in the system. However, to prevent short circuit, dead-time should still be applied to each of the commutated switches.

Table. I Line side switch state and DC voltage in each interval

Interval	Portion 1		Portion2	
	On Switch	V_{dc}	On Switch	V_{dc}
1	S_{bnp}, S_{bnn} S_{apn}, S_{app}	V_{sa} - V_{sb}	S_{cnp}, S_{cnn} S_{apn}, S_{app}	V_{sa} - V_{sc}
2	S_{bpp}, S_{bpn} S_{cnp}, S_{cnn}	V_{sb} - V_{sc}	S_{app}, S_{apn} S_{cnp}, S_{cnn}	V_{sa} - V_{sc}
3	$S_{cnp,}$ S_{cnn} S_{bpn}, S_{bpp}	V_{sb} - V_{sc}	S_{anp}, S_{ann} S_{bpn}, S_{bpp}	V_{sb} - V_{sa}
4	S_{cpp}, S_{cpn} S_{anp}, S_{ann}	V_{sc} - V_{sa}	S_{bpp}, S_{bpn} S_{anp}, S_{ann}	V_{sb} - V_{sa}
5	S_{anp}, S_{ann} S_{cpn}, S_{cpp}	V_{sc} - V_{sa}	S_{bnp}, S_{bnn} S_{cpn}, S_{cpp}	V_{sc} - V_{sb}
6	S_{app}, S_{apn} S_{bnp}, S_{bnn}	V_{sa} - V_{sb}	S_{cpp}, S_{cpn} S_{bnp}, S_{bnn}	V_{sc} - V_{sb}

D. Space vector PWM control

Initially, it is useful to consider the conventional VSI with three-phase output voltage V_{su} , V_{sv} , and V_{sw} supplied by a DC voltage source $V_{dc} = 3 \cdot V_m / 2$. In complex form, the space vector of the desired output voltages is

$$\vec{V}_{o\_ref} = V_{su} + V_{sv}\cdot e^{j\frac{2\pi}{3}} + V_{sw}\cdot e^{-j\frac{2\pi}{3}} = k\cdot\frac{3V_m}{2}\angle\theta_o \qquad (7)$$

Where $0 < k < \sqrt{3}/2$ is a constant.

Supposing $0 < q_o < p/3$ and that the system operates in interval 2, this vector can be approximated by its two adjacent voltage vectors (V_1 and V_2) and the zero voltage vector V_0 as shown in Fig. 9. The duty ratios of these vectors are

$$d_1 = \frac{2k}{\sqrt{3}}\sin(\frac{\pi}{3}-\theta_o);\ d_2 = \frac{2k}{\sqrt{3}}\sin(\theta_o);\ d_0 = 1-d_1-d_2 \qquad (8)$$

The average DC current of the inverter with the above duty cycles is determined as

$$i_{dc} = k\cdot I_o\cdot\cos(\theta_o-\theta_{oi}) = I_{im} \qquad (9)$$

Because there are two portions during each switching cycle, the duty cycles V_1, V_2, and V_0 are also distributed to each portion. During the first portion, they are:

$$d_{1bc} = d_1\cdot|\cos\theta_b|; \qquad d_{2bc} = d_2\cdot|\cos\theta_b|$$
$$d_{0bc} = d_0/2; \qquad d_{bc} = d_{1bc}+d_{2bc}+d_{0bc} \qquad (10)$$

During the second portion,

$$d_{1ac} = d_1\cdot|\cos\theta_a|; \qquad d_{2ac} = d_2\cdot|\cos\theta_a|$$
$$d_{0ac} = d_0/2; \qquad d_{ac} = d_{1ac}+d_{2ac}+d_{0ac} \qquad (11)$$

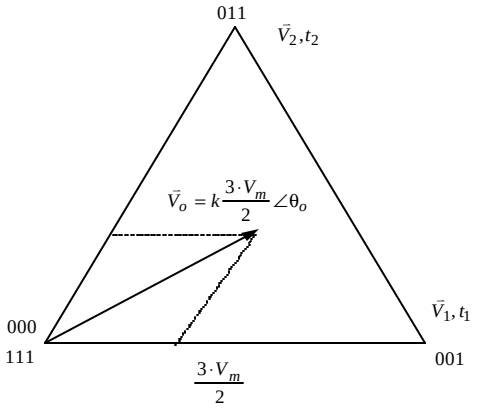


Fig. 9. Space vector PWM for inverter while $0 < \theta_o < \pi/3$

Combining Eqs. (7) to (11), the actual average output voltage vector and the input current can finally be obtained as

$$\vec{V}_o = k\cdot\frac{3V_m}{2}\angle\theta_o;\ i_{sa} = I_{im}\cdot\cos\theta_a$$
$$i_{sb} = I_{im}\cdot\cos\theta_b;\ i_{sc} = I_{im}\cdot\cos\theta_c \qquad (12)$$

This result demonstrates that the proposed space vector PWM control method generates the same actual output voltage as the reference voltage and that the line side power factor can inherently remain at unity.

Figure 10 shows the PWM sequence of the converter. The figure shows that the zero vectors are utilized while the line side switches are commutating; i_{dc}, i_{sa}, i_{sb} and i_{sc} are all equal to zero. Hence, the current of line side switches are all zero and the line side switches commutate at zero current.

When the system operates during the other intervals or when $\theta_o > \pi/3$, the same results can clearly be obtained.

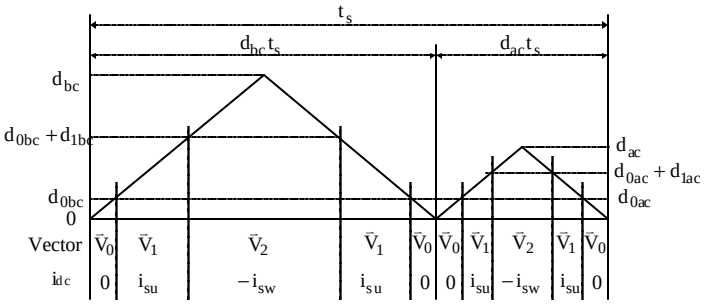
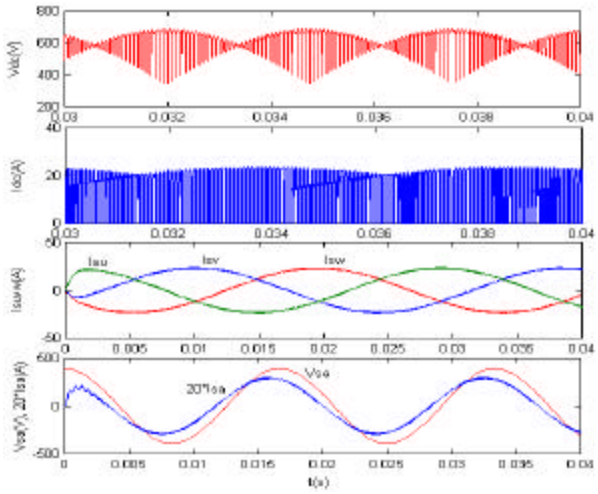


Fig. 10. PWM sequence of the converter in interval 2

VI. Simulation and Experimental Results

Figure 11 shows simulation results of the proposed matrix converter. The waveforms shown are DC voltage, DC current, output current, input phase voltage, and the input phase current. From Fig.11, the following statements can be made: (a) the DC voltage and DC current are both modulated at high frequency (switching frequency); (b) The three-phase output currents are essentially sinusoidal. Thus, there are no low order harmonics in the output voltage. (3) The waveforms of the input phase current are nearly sinusoidal. Because the existence of a line side filter, the phase current leads the phase voltage in this figure.



(a) Current and voltage waveform

Fig. 11. Simulation result for the proposed matrix converter

A hardware realization has been constructed to test these converters from 18-switch to 9-switch utilizing a three-phase inductive resistor. A digital signal processor (DSP56F805 from Motorola company) and a CPLD are used to control the converter. The switching frequency of the system is 5KHz.

Fig.12 shows an experimental result for a 9-switch dual-bridge matrix converter. Fig. 12 (a) shows both the line and load side waveforms. Beside unity power factor, it can also be observed from this figure that both line side current i_{sa} and load side current i_{su} are nearly sinusoidal, confirming that the dual-bridge matrix converter can provide high quality AC/AC waveforms

Figure 12 (b) shows the waveforms of DC voltage and clamp capacitor voltage. It can be determined that the clamp capacitor voltage equals to the peak value of the DC voltage as expected and that the clamp diode is generally anti-biased during the operation. Figure 12 (c) and (d) show the voltage and current of the line side switch S_{ap}. Figure 12 (d) verifies the zero current switching nature of the line side switches. Clearly no large commutation spikes are generated during their commutation.

VII. Conclusion

This paper investigates the performance of dual-bridge matrix converter topologies. In particular, the study focuses on the possibility of reducing the switch number from 18 to 15 with bi-directional power flow, and from 18 to 9 for single directional power flow. In addition it is demonstrated that conventional sine-triangle PWM control can be utilized for these new converters. The following results have been obtained:

- A 15-switch topology was derived for four quadrant operation
- A 12-switch and 9-switch topology were obtained for single directional power flow with output power factor on the load side greater than 0.866
- A simple clamp circuit with only one diode and one capacitor has been introduced and tested
- Space vector PWM with a variable DC link voltage has been employed. With this method, the converter exhibits high quality input/output waveforms.
- The commutation problem associated with matrix converters has been simplified. All line side switches are controlled to commutate at zero current and the load side switches commutate in the same manner as the conventional DC/AC inverter.

VIII Acknowledgement

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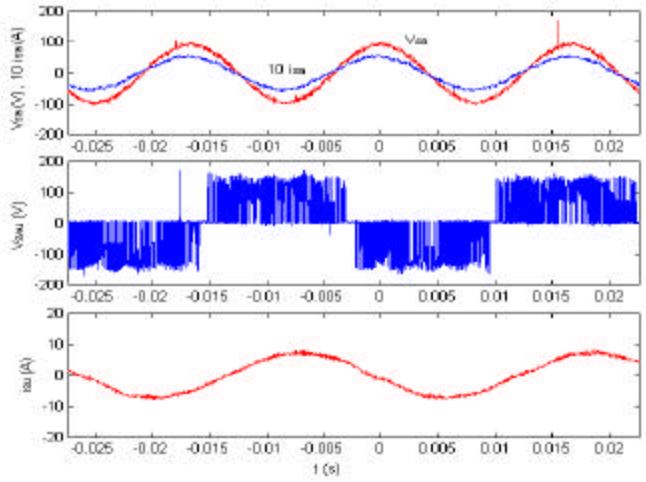
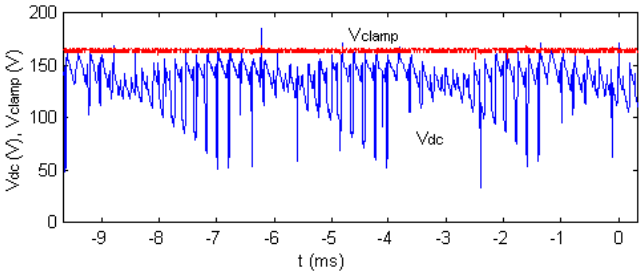
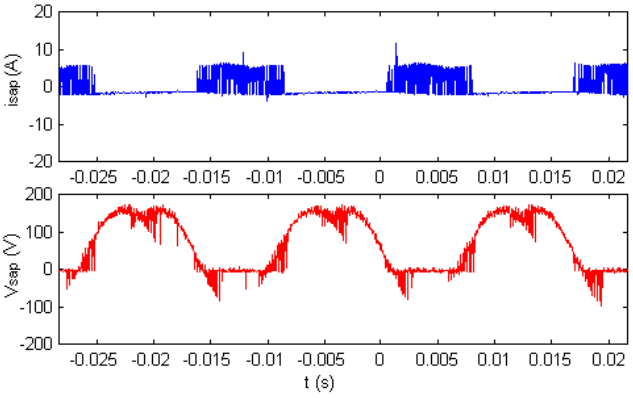


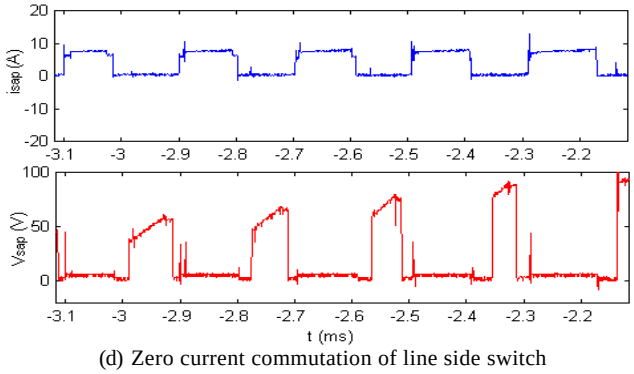
(a) Input / output voltage and current



(b) DC side voltage and clamp capacitor voltage



(c) Line side switch voltage / current (S_{ap})



(d) Zero current commutation of line side switch

Fig. 12 Experimental result obtained for the 9-switch matrix converter

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