Reduction of DC Bus Capacitor Ripple Current with PAM/PWM Converter

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***Abstract*—Electrolytic Capacitors are used in nearly all adjustable speed drives (ASD) and they are one of the components most prone to failure. The main failure mechanisms include the loss of electrolyte through outgassing and chemical changes to the oxide layer. All the degradation mechanisms are exacerbated by ripple current heating. Since the equivalent series resistance (ESR) of electrolytic capacitors is a very strong function of frequency it must be properly modeled to accurately calculate the power loss. In this paper a method to reduce the ripple current in a constant Volts/Hertz (V/f) Pulse Amplitude Modulation (PAM/PWM) converter driving an induction motor is investigated. The DC bus voltage amplitude is reduced in proportion to speed by a buck or current source rectifier (CSR) and the PWM modulation index is increased to achieve a reduced ripple current below base speed. It is shown that this mode of operation can lead to a significant reduction in capacitor power loss leading to increased capacitor lifetime or decreased capacitor size. The capacitor heating is analyzed using numerical and analytical techniques. Experimental results are provided to verify the analytical results.**

Keywords—Industrial drives; Current ripple; Electrolytic capacitor modeling; Buck Rectifier; PAM; PWM; Current Source Rectifiers; Voltage Source Inverter; ASD; ESR.

I. INTRODUCTION

Nearly all modern adjustable speed drives (ASD) use electrolytic capacitors to supply the stiff DC bus voltage for Voltage Source Inverters (VSI). The capacitors also decouple the rectifier from the inverter part of the drive by providing a low impedance path for the high frequency ripple current. The main sizing considerations for bus capacitors are ripple current rating and voltage holdup time during power failure. Voltage ripple specifications will typically be met when the previous two specifications are satisfied, thus it is not normally a primary concern for sizing.

Electrolytic capacitors have a relatively high ESR (equivalent series resistance) and must endure high current ripple from the inverter and often the rectifier as well. The focus of this paper is the inverter contribution, since with proper design the rectifier contribution to the ripple current can be made negligible (i.e. by adding a large enough AC or DC side reactor) [1, 2]. Operating temperature is the main factor causing degradation of the capacitor parameters, especially the ESR. The ripple current and ambient temperature are the main contributors to the temperature rise of the capacitor. Two of the causes of degradation due to heating are chemical changes in the oxide layer and the electrolyte [3] and electrolyte pressure increase allowing electrolyte gas to escape through the capacitor end seal. Both factors lead to an increase in ESR over the operating life of a capacitor. At some point the ESR will exceed the maximum recommended value (termed parameter drift failure [3]). This is considered the end of life for the capacitor in which case it should be replaced [2].

The RMS ripple current in the electrolytic capacitor from the inverter side is primarily a function of the load phase angle (ϕ) and the modulation index M_i. This assumes the machine transient inductance ($L\sigma$) is large enough so that the output switching frequency current ripple is negligible. The capacitor RMS ripple can then be considered to be entirely composed of segments of the three sinusoidal output currents chopped up at the switching frequency [4, 5]. To examine the power loss in the capacitor an estimate of all significant current harmonics is needed. The ESR model as a function of frequency is then multiplied at each harmonic frequency by the square of the current component and the resulting terms summed.

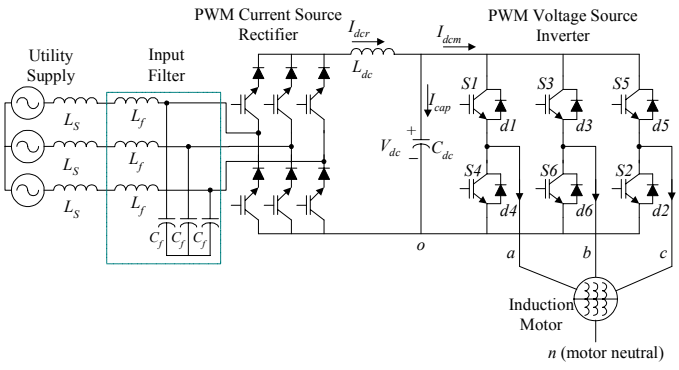

Figure 1. PAM/PWM converter with Current Source Rectifier and Voltage Source Inverter.

The standard mode of operation of an ASD is to maintain the link voltage (V_{dc}) at a constant value and adjust the modulation index to control the output voltage. The link

voltage in the majority of drives is created with three phase diode bridge rectifiers. Increasingly, due to Power Quality considerations, Voltage Source Rectifiers (VSR) are used to provide a unity PF utility interface. The Current Source Rectifier (CSR), as an alternative to the VSR, can also provide unity PF as well as a buck function for V_{dc}. This allows an alternate mode of controlling an ASD combining Pulse Amplitude Modulation (PAM) [6] and PWM. By reducing V_{dc} with a CSR, M_i can be increased which will then decrease the ripple current by changing the magnitude and distribution of harmonics.

The effects of this additional degree of freedom can be explored in the overall ASD in terms of efficiency, lifetime, dynamic response, etc. This paper explores the effect of varying V_{dc} and M_i on the electrolytic capacitor ripple current with an induction motor load. The reduced current ripple results in a reduction of power losses in the capacitor over most ranges of loading and speed. This in turn can lead to a reduction in the necessary bus capacitance or to an increase in capacitor lifetime. The PAM/PWM topology is shown in Fig. 1. A 7.5kVA prototype inverter driving a 10HP induction motor was used to obtain experimental results.

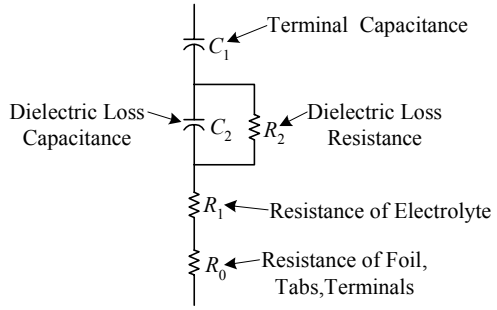

Figure 2. Electrolytic Capacitor Model.

II. ESR Model for Electrolytic Capacitor

In order to reasonably estimate the power loss in an electrolytic capacitor bank a good model is needed. The electrolytic capacitor model used in this analysis was introduced in [2] where it was shown to match well with experimental results, including lifetime prediction. The circuit diagram of the model is shown in Fig. 2. The physical meaning of each component is indicated in the figure. The complete equation for the real part of the impedance, which is the ESR, is shown below:

$$ESR = \frac{R_2}{1+\omega^2 C_2^2 R_2^2} + R_{1b}\, e^{(T_{base} - T_{core})/E} + R_0. \qquad (1)$$

The frequency dependence of the *ESR* is due to the dielectric and is provided in the model by the parallel combination of R_2 and C_2. The temperature dependent nature of the electrolyte resistance, R_1 is modeled with a base resistance, R_{1b} and an exponential temperature variation controlled by a temperature sensitivity factor E. T_{base} is the temperature at which the *ESR* was measured while T_{core} is the temperature of interest for the *ESR* calculation.

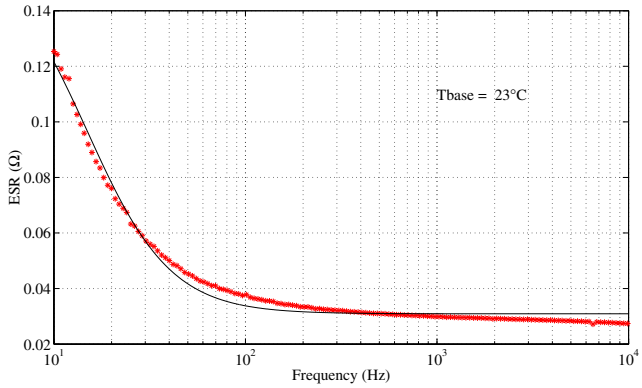

Figure 3. ESR vs. frequency of electrolytic capacitor bank: experimental data points (*), model with curve fit parametes (—).

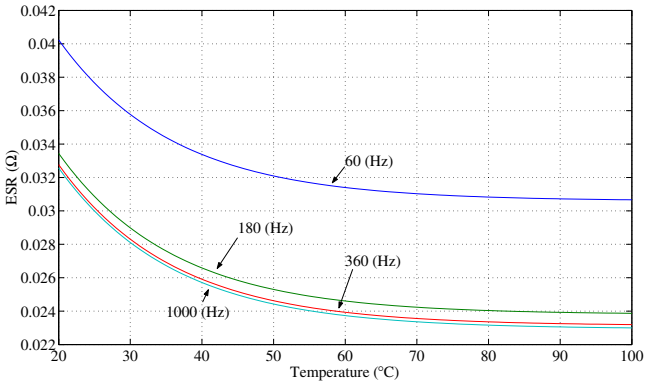

Figure 4. ESR vs. Temperature of electrolytic capacitor bank for several frequencies of interest.

TABLE I. Electrolytic Capacitor Parameters

R_0	22.9	mΩ
R_{1b}	8.0	mΩ
E	16.1	°K^{-1}
R_2	131	mΩ
C_1	2530	μF
C_2	81000	μF

The ripple current heating losses in the capacitor are estimated based on this model. The parameters for the capacitors used in the experimental setup have been determined by impedance measurements of the capacitor bank. The measured variation of ESR with frequency is shown in Fig. 3. A curve fit to the model, done in MATLAB, is also shown in the figure. More series parallel RC segments can be added to produce a better fit [2], but a single pair results in sufficient accuracy to judge the relative change in losses. The resulting parameter values are shown in Table I. The *ESR* change with temperature is shown in Fig. 4 for several frequencies of interest.

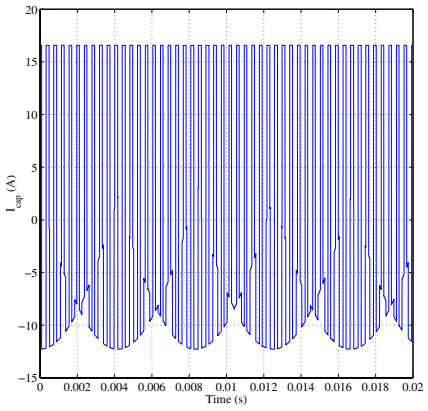

Figure 5. Calculated capacitor ripple current waveform: full V_{dc}, 40Hz fundamental, 75% rated motor torque load.

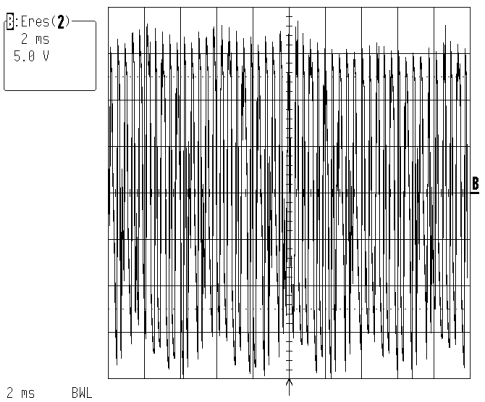

Figure 6. Experimental capacitor ripple current waveform: full V_{dc}, 40Hz fundamental, 75% rated motor torque load, 3bit enhanced res.

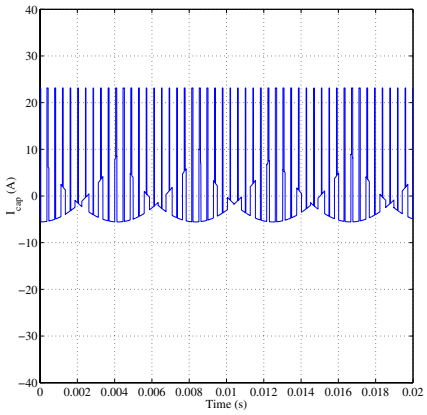

Figure 7. Calculated capacitor ripple current waveform: V_{dc} = 228V, 40Hz fundamental, 75% rated motor torque load.

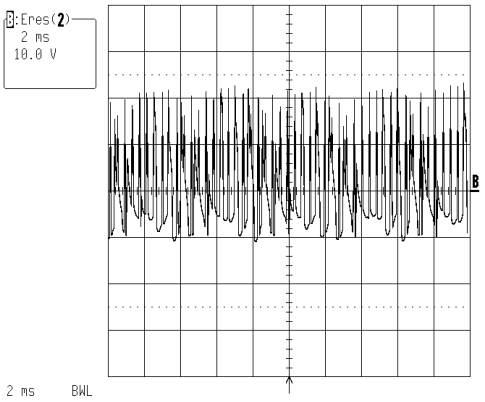

Figure 8. Experimental capacitor ripple current waveform: V_{dc} = 228V, 40Hz fundamental, 75% rated motor torque load, 3bit enhanced res.

III. Determination of Capacitor Current Spectrum of VSI Drive

The capacitor current spectrum can be estimated by chopping up the sinusoidal output currents going to the induction motor. The modulation method used to create the PWM device gate signals in the VSI was the regular sampled Space Vector PWM (SVPWM) ramp comparison method. This is equivalent to the direct digital method used in (SVPWM) [7]. The experimental setup uses a TI TMS320F240 DSP to produce the gate signals with an identical modulation method. The modulation index used in the calculations is defined as

$$V_1 = M_i \frac{V_{dc}}{2} \sin(\omega t) \qquad (2)$$

where V_1 is the fundamental output voltage and M_i is the inverter modulation index [8]. Defined this way the ideal limit of the linear modulation region for SVPWM is when M_i = 1.15. The capacitor current harmonics are calculated numerically in MATLAB as will be outlined below.

First the PWM pole voltage waveforms from Fig. 1 (v_{ao}, v_{bo}, v_{co}) are determined. A speed/frequency command is given and the modulation index is determined based on the DC bus voltage and the required induction motor terminal voltage. The three regular sampled voltage references are formed and then the intersections with the triangle carrier are computed. The resulting output voltage as well as the given load torque (as slip frequency) are fed into an induction machine model. This determines the output current magnitude and phase for all thee phases assuming a balanced three-phase set.

The following voltage and current variables follow the standard notation based on the nodes labeled in Fig. 1. The capacitor current is then calculated by first determining the pole currents in the upper diodes and switches of the inverter from the pole voltage switching instants and the phase currents

$$I_{pa} = I_{s1} - I_{d1}\,, \quad I_{pb} = I_{s3} - I_{d3}\,, \quad I_{pc} = I_{s5} - I_{d5}\,. \qquad (3)$$

The sum of the three upper pole currents than determine the DC link current to the motor as

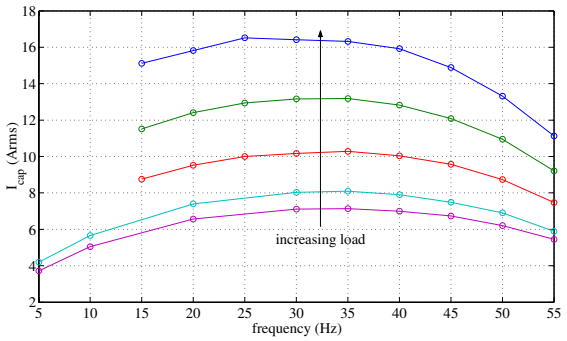

Figure 9. Calculated RMS electrolytic capacitor current with constant V_{dc} = 323V and varying modulation index.

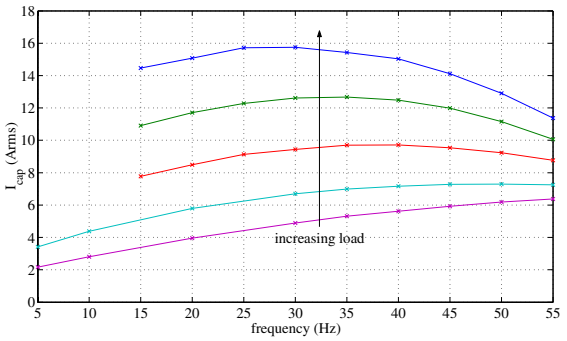

Figure 10. Experimental RMS capacitor ripple current with constant V_{dc} = 323V and varying modulation index.

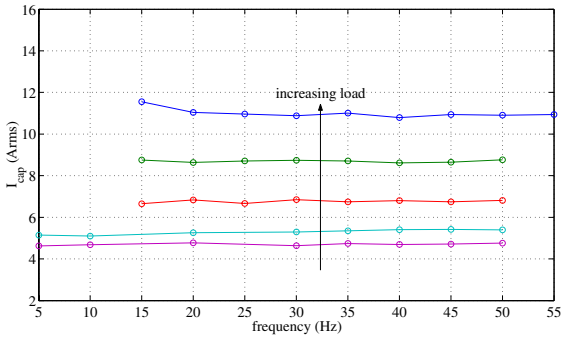

Figure 11. Calculated RMS capacitor current with varying V_{dc} and constant modulation index M_i = 1.07.

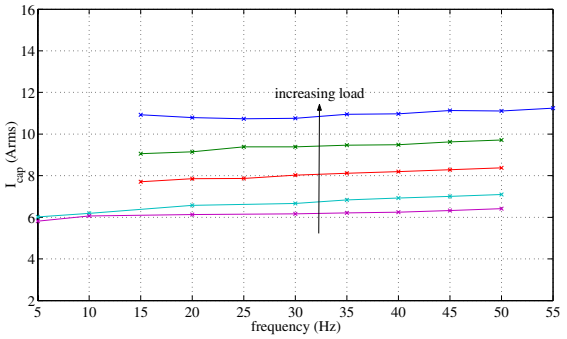

Figure 12. Experimental RMS capacitor ripple current with varying V_{dc} and constant modulation index M_i = 1.07.

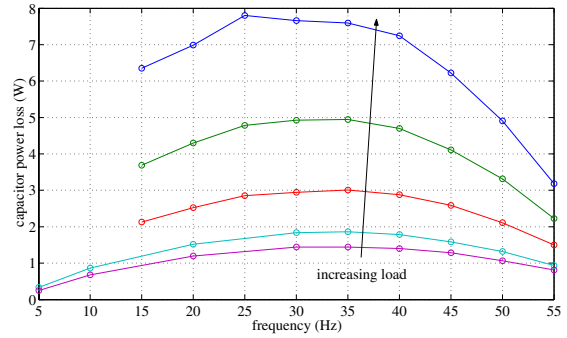

Figure 13. Calculated capacitor power loss with constant V_{dc} = 323V and varying modulation index.

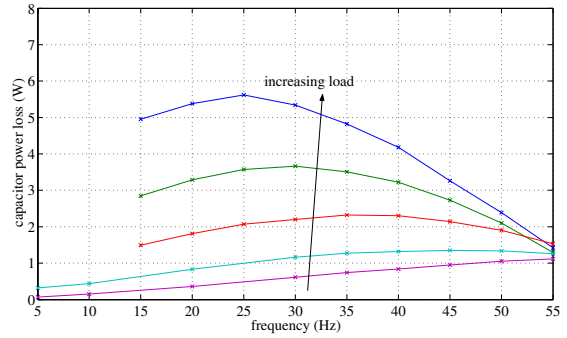

Figure 14. Experimental capacitor power loss with constant V_{dc} = 323V and varying modulation index.

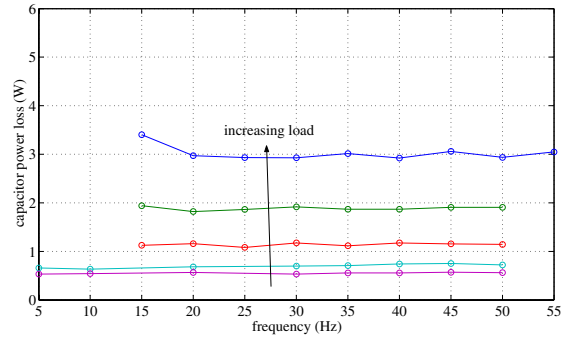

Figure 15. Calculated capacitor power loss with varying V_{dc} and constant modulation index M_i = 1.07.

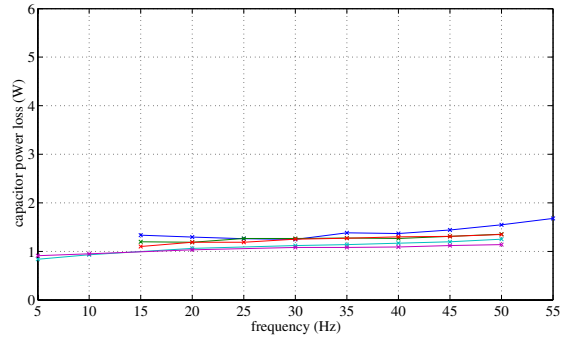

Figure 16. Experimental capacitor power loss with varying V_{dc} and constant modulation index M_i = 1.07.

$$I_{dcm} = I_{pa} + I_{pb} + I_{pc} \,. \tag{4}$$

Assuming the rectifier current is constant with negligible harmonic content (i.e. $I_{dcr} = I_{dcm(ave)}$), as mentioned previously [1] the capacitor current is

$$I_{cap} = I_{dcm(ave)} - I_{dcm} \,. \tag{5}$$

The calculated and experimental waveforms of I_{cap} for full and reduced V_{dc} are shown in Figs. 5-8 for the same speed and RMS fundamental output current. The measured waveform for I_{cap} was captured with a low insertion impedance coaxial current transformer put in the output DC link current path [9]. The inverted AC coupled waveform is shown on the oscilloscope trace after digital filtering (80kHz bandwidth) to remove the high frequency current spikes. This accurately represents the capacitor current as long as the rectifier contribution is negligible. The difference in magnitude can be attributed to the output AC current ripple due to the $L\sigma\, di/dt$ of the induction motor with the low switching frequency (1225 Hz).

From the time domain capacitor current calculated above the vector of RMS harmonic components are calculated using the MATLAB *fft*() function as

$$I_{caph} = \frac{|fft(I_{cap})|}{\sqrt{2}\cdot N/2} \,. \tag{6}$$

where N is the number of points in the time vector I_{cap} . The total ripple current RMS value can then be determined from the N_h frequency components in the harmonic spectrum as

$$I_{cap,rms} = \sqrt{\sum_{n=1}^{N_h} I_{caph,n}^2} \,. \tag{7}$$

This was then compared with the following per unit equation [4, 5] as a further verification of the calculations

$$I_{cap,rms,pu} = \frac{I_{cap,rms}^2}{I_{1rms}^2} = \frac{2\sqrt{3}}{\pi} M_i + \left(\frac{8\sqrt{3}}{\pi^2} - \frac{18}{\pi^2} M_i\right)\cdot M_i \cos^2(\phi) \tag{8}$$

where I_{1rms} is the fundamental induction motor current. The maximum error between the two calculations was approximately 4% at full speed and load for both the constant V_{dc} and varying V_{dc} cases.

The RMS capacitor currents are calculated for loads from zero to rated torque and excitation frequencies from 5 Hz to 55Hz. The minimum excitation frequency for each load condition was determined from the induction machine parameter calculated torque/speed curves by the torque at maximum slip. Since no voltage boosting was applied at low frequency the peak torque was reduced at lower speeds due to the increased relative effect of the rotor resistance.

The resulting current ripple from calculation and experimental measurements are shown in Figs. 9-12. The experimental and calculated results match quite well for both the constant and varying V_{dc} cases. Most importantly they match for the high load condition. In Figs. 11 and 12 it can be seen that when M_i was held constant the ripple current becomes nearly flat over the entire speed range. This is important from the perspective of capacitor sizing, since now one need only consider the ripple current at the rated speed and load. The maximum value was also reduced by about 40%.

It can be seen that reducing V_{dc} and increasing M_i to a high value result in much lower ripple current for the mid-range of frequencies. Experimentally the maximum modulation index was limited to about $M_i = 1.07$ due to dead time and minimum allowed pulse width considerations for the IGBTs in the VSI.

IV. Capacitor Loss Calculations

Using the capacitor current harmonic components from above the power loss is calculated by

$$P_{loss} = \sum_{n=1}^{N_h} I_{caph,n}^2 \cdot ESR(f_n) \,. \tag{9}$$

The heating losses were calculated for each set of harmonics calculated for the ripple current. In that way the full rated range of speed and load for the 10HP induction machine was covered. In the normal mode of operation the DC bus voltage was fixed at approximately 323V so that at full speed the modulation index would be the maximum of 1.07. During variable DC bus operation the modulation index was fixed at 1.07 while V_{dc} was varied from zero to 323V.

The experimental capacitor loss calculation was done using a LeCroy oscilloscope with mathematical functions to multiply the capacitor current and the AC part of the DC link voltage. The mean value of the instantaneous power was than averaged over 20 to 30 sweeps. The DC link voltage was measured using a precision high voltage differential amplifier AC coupled to the scope. The link voltage was controlled with a variac through a diode bridge and a DC side inductor. This setup will be replaced with a CSR when the control and converter are fully implemented.

The calculation and experimental results are shown in Figs 13-16. The full DC bus results match quite well in shape since the peak values occur at nearly the same frequency. The calculated results can be taken as a conservative estimate. For the varying DC bus results again all the curves are flat across the range of frequencies. The measured results are all lower than the calculated results due mainly to the temperature dependence of the electrolyte resistance, R_1, since it decreases with increasing temperature as shown in Fig.4. The calculations were all done assuming one temperature. In the experimental setup the temperature increased under larger load decreasing the ESR and reducing the losses while under less load the temperature decreased increasing the ESR and increasing the losses. This effect is especially noticeable in the varying DC bus power loss measurements where the range of losses with load is virtually collapsed.

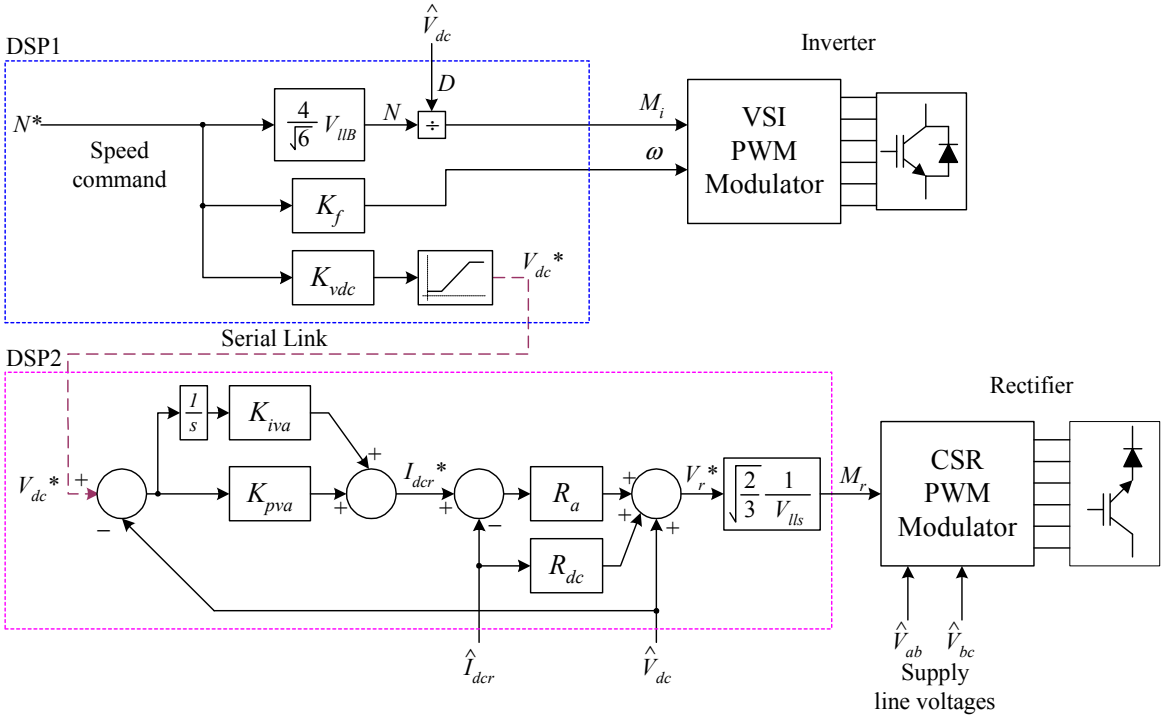

Figure 17. Proposed two DSP controller for PAM/PWM motor drive: VSI with V_{dc} compensation of modulation index for open loop V/f control and V_{dc}* generation, CSR with closed loop PI voltage regulator.

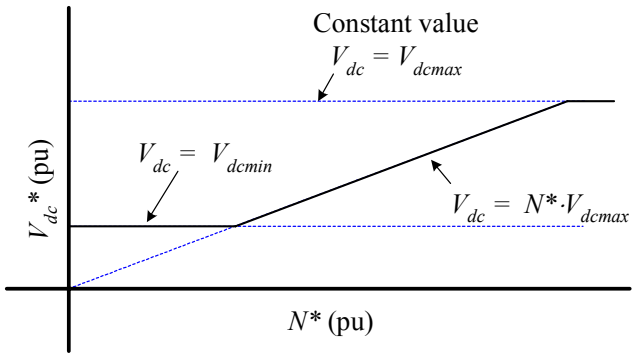

Figure 18. Per unit DC bus voltage command (V_{dc}*) vs. Speed (N*) generated in VSI controller and sent serially to CSR controller.

Similarly to the ripple current results it can be seen that in the mid-speed range from zero to full load the losses can be significantly reduced. The peak reduction for the calculated losses is about 55% and the peak reduction for the experimental results is about 70%. The ripple current rating of electrolytic capacitors is really a way of getting at the capacitor heating effect. Thus the power loss results give a better picture of the stresses on the capacitor.

V. Proposed PAM/PWM Controller

From the capacitor power loss results it can be seen that operation by varying the DC bus voltage with speed can be advantageous for the electrolytic capacitor lifetime or sizing requirements. The increase in lifetime will depend on the typical drive duty cycle and whether it requires operation below base speed for a significant fraction of time. In terms of sizing considerations the reduction in peak capacitor losses depends on the range of modulation indices the drive will command. Based on these conclusions a PAM/PWM drive based on Fig. 1 will be implemented with the proposed controller shown in Fig. 17.

The DC link voltage command will essentially be linearly proportional to commanded speed. Assuming there is a minimum reasonable DC bus voltage based on rectifier limitations or other concerns the commanded bus voltage (V_{dc}*) will have a lower limit greater than zero. The upper limit will be determined by the utility line voltage and the need to operate the CSR in the linear modulation region. Power quality requirements for unity power factor and minimal current distortion will decide the importance of the second condition. The general form of the voltage command is shown in Fig. 18.

The hardware controller will be based on two TI DSP boards, one for the rectifier and one for the inverter. The inverter will need to give the DC link voltage command based on the commanded speed. In order to minimize the amount of communication between the DSPs the modulation index is adjusted automatically based on the desired output voltage and the measured bus voltage $\hat{V}_{dc}$ according to

$$M_i = N^* \cdot \frac{4}{\sqrt{6}} \cdot \frac{V_{llB}}{\hat{V}_{dc}} \qquad (10)$$

where V_{llB} is the base line to line machine voltage and N^* is the per unit speed command.

In the rectifier the voltage command received from the inverter, V_{dc}^*, will drive the controller. An outer loop proportional (K_{pva})/integral (K_{iva}) regulator will be used to control the DC link voltage. The inner loop consists of an active resistance proportional (R_a) controller on the rectifier current I_{dcr} . The parasitic resistance of the DC bus inductor R_{dc} and the link voltage V_{dc} are also decoupled from the command voltage V_r^* so the PI voltage controller only responds to voltage errors [10]. The '^' indicates a measured or estimated value. Finally the modulation index, M_r is produced from the rectifier voltage command, V_r^*, by the equation [11]:

$$M_r = V_r^* \cdot \sqrt{\frac{2}{3}} \cdot \frac{1}{V_{lls}} \tag{11}$$

where V_{lls} is the line to line supply voltage.

The maximum value of M_r depends on how much distortion is acceptable to the utility. To have the least distortion M_r should be limited to 1.0. This also limits the maximum DC bus voltage to around 280V with a line to line utility supply voltage of 230Vrms. This can be increased by going into overmodulation as with a VSI, but at the price of input current distortion. The operation of the full converter with this controller will be demonstrated in a future paper.

VI. CONCLUSION

Investigations have been made into the effect of varying the link voltage V_{dc} with speed and holding the modulation index M_i constant in an induction motor V/f drive. It has been shown through numerical calculations that the peak ripple current in the DC bus electrolytic capacitor can be significantly reduced. Further it has been shown that the effective heating due to the power loss in the ESR can be reduced even further because of the strong frequency dependence of the ESR. These results were verified by measurements made on a 7.5kW motor drive.

The reduced heating stresses on the electrolytic capacitor bank can lead to increased lifetime. Depending on the driving factors for a particular drive the capacitance of the electrolytic capacitor bank can instead be reduced.

Finally a topology for realizing the varying DC bus voltage has been described. A standard controller has been proposed for the overall PAM/PWM converter as well. The applications where this mode of operation could be useful would operate below base speed for a significant portion of their load profile. Some examples include: electric vehicles, off road electric construction equipment and compressor pumps.

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ACKNOWLEDGMENT

The authors would like to thank the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) and specifically Rockwell Automation for their support of the research presented in this paper.