Reduced Common Mode Carrier-Based Modulation Strategies for Cascaded Multilevel Inverters

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***Abstract* - This paper presents carrier-based modulation strategies for cascaded multilevel inverters that substantially eliminate common mode voltage on the output phases. The paper begins by developing generic multilevel inverter reference waveforms that use only "allowed" space vectors to achieve reduced common mode voltage. A graphical technique is then proposed that allows various carrier disposition modulation strategies for a diode clamped inverter to be converted to equivalent modulation of a cascaded inverter for any fundamental reference waveform. This graphical technique is confirmed for both APOD and PD equivalent modulation of a cascaded inverter, and is then used to create reduced common mode modulation strategies for cascaded inverters from their equivalent counterparts for diode-clamped inverters under both continuous and discontinuous switching conditions. The strategies have been confirmed by both simulation and experimental results obtained using a cascaded five-level inverter.**

I. Introduction

Multilevel inverters have been attracting increasing interest recently, particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage waveforms. The two most common multilevel inverter topologies, shown in Figure 1, are diode-clamped or neutral-point-clamped (NPC) inverters, and cascaded inverters. For these inverters, a variety of modulation strategies have been reported, with the most popular being carrier-based [1-7] and Space Vector Modulation (SVM) [6-8].

Carrier-based modulation strategies for diode-clamped inverters are most commonly based on carrier disposition techniques, and are well established [2-4, 6, 7]. For cascaded inverters, phase-shifted carrier-based modulation strategies are the most widely used [1, 2, 5], with some derived strategies being recently reported that offer improved harmonic performance [2, 4]. These two forms of modulation have also been recently shown to be equivalent by comparing analytical solutions of their switched waveforms, derived using Double Fourier Series (DFS) analysis [2].

Space Vector Modulation involves switching between the three nearest space vectors from the available states of an inverter. Several approaches have been presented to show how these space vectors can be selected for particular operating conditions [8]. However, it is likely that the carrier-based strategies will remain widely adopted because of their inherent simplicity and reduced computational requirements compared to SVM, particularly with recent work showing that carrier-based and SVM strategies for multi-level inverters are equivalent [7].

For applications such as AC motor drives, it is desirable to minimise common mode voltage to prevent premature bearing failure and reduce EMI levels. Several modulation variations that achieve this result have been reported for both

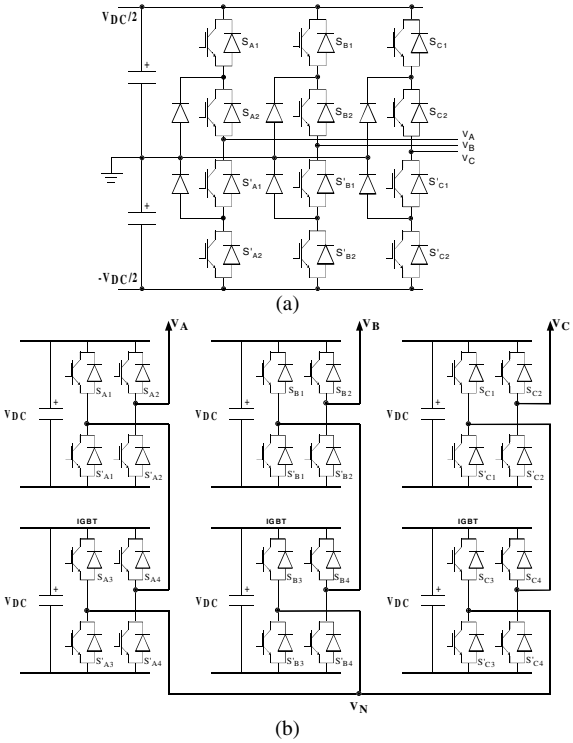

Figure 1: Topological arrangements of (a) three-level neutral-point-clamped and (b) five-level cascaded inverters.

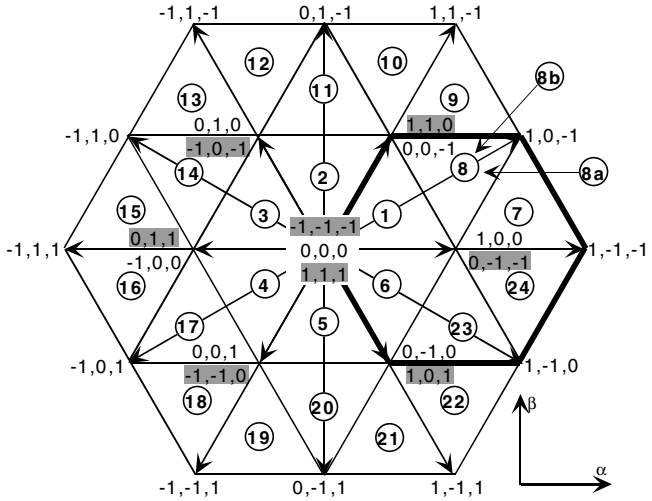

Figure 2: Space vector diagram of a three-level inverter (state indexes normalised with V_{dc}).

carrier-based and SVM schemes [1, 6, 9]. However, most of these strategies are limited to three-level diode-clamped inverters and have many unresolved issues, such as the relationship between the required command references and the "allowed" space vectors that achieve reduced common mode voltage, generalisation to higher level inverters and the matching of equivalent modulation strategies between diode-clamped and cascaded inverters. These issues are addressed systematically in this paper through the derivation of both continuous and discontinuous reduced common mode carrier-based modulation strategies for cascaded inverters. The principles presented have been verified by both detailed MATLAB simulation and experimental investigations.

II. Modified PWM References for Common Mode Reduction

Common mode voltages are reduced by avoiding those inverter switching states that have a common offset voltage. This can be achieved by adding offsets to the fundamental sinusoidal references of a carrier-based modulation system to avoid these switching states, as follows:

A. *Partial Common Mode Elimination (PCME)*

NOTE: While the analysis presented here is for a three-level inverter for simplicity and ease of understanding, it is equally applicable to higher level inverters. In addition, the carrier disposition PWM strategy (commonly used for diode-clamped inverters) is used for illustration, with the equivalent PWM strategy for cascaded inverters presented in Section III.

The space vector diagram of a three-level inverter and typical vector sequences under PD modulation are illustrated in Figures 2 and 3 respectively. In total, there are 27 possible switching states, of which 20 will generate common mode voltage, defined as $V_{cm} = (V_{AN} + V_{BN} + V_{CN})/3$, ranging from $-V_{dc}$ to $+V_{dc}$.

Previous approaches [9] limit the common mode voltage to within $\pm V_{dc}/3$ by using only 19 switching states (the "avoided" states are shaded out in Figure 2). The vector diagram is then divided into many sub-triangles and offsets for the sinusoidal references are derived for each sub-triangle. However, this approach creates different offset equations for each sub-region and hence its generalisation to higher level inverters is not obvious.

An improved approach is now presented here that results in one offset equation for all regions on the vector diagram. It can also be equally applied to higher level inverters.

Other work has already shown that multilevel modulation can be viewed as conventional two-level modulation with an appropriate reference null shift [6, 8, 10]. For example, for a three-level inverter, this means that when θ (the phase angle of the reference phasor) is between $-30^o \le \theta < 30^o$, the reference null shifts from ({−1, −1, −1}; {0, 0, 0}; {1, 1, 1}) to ({0, −1, −1}; {1, 0, 0}), to create the effective two-level hexagon bolded in Figure 2. The switching effect is shown in detail in Figure 3 where the vector sequences start and end

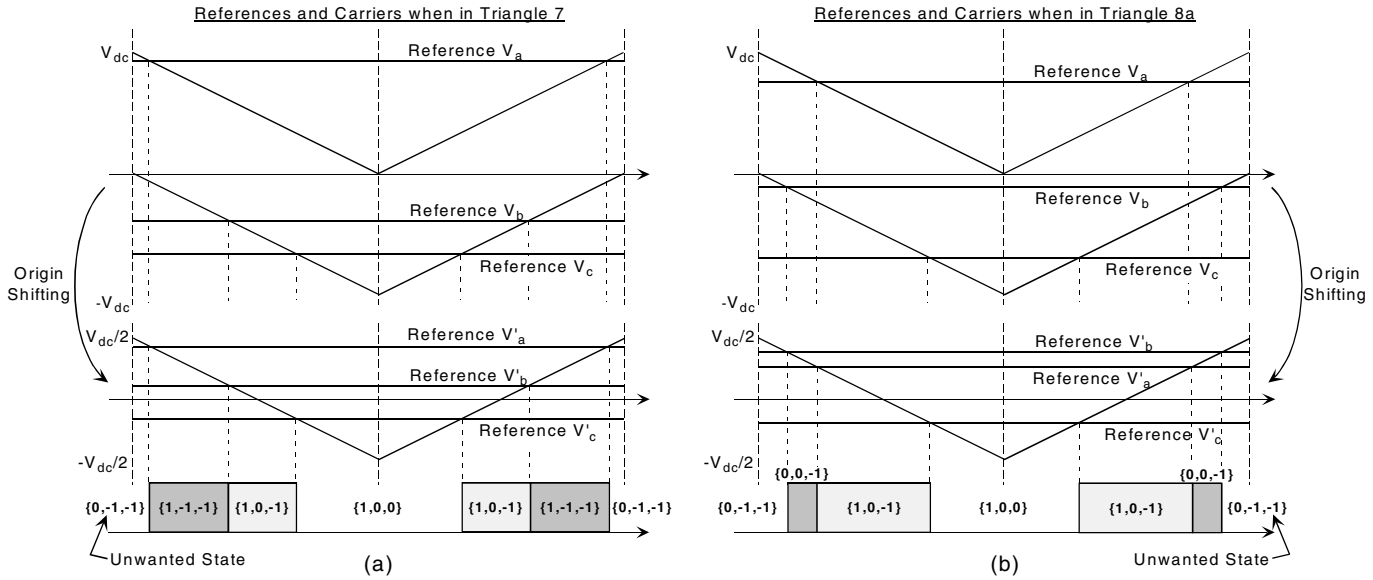

Figure 3: Typical vector sequences when reference phasor is in (a) triangle 7 and (b) triangle 8a.

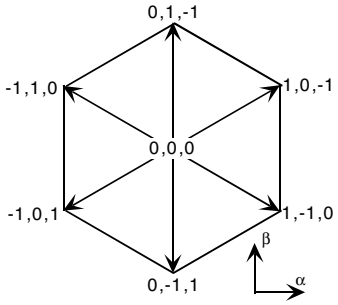

Figure 4: Reduced space vector diagram of a three-level inverter.

with either states {0, −1, −1} or {1, 0, 0}.

For carrier-based modulation, this strategy can be explained as adding appropriate offsets to the command references V_a, V_b and V_c, to create modified references V'_a, V'_b and V'_c that exist within a single common carrier region spanning $-V_{dc}/2$ and $V_{dc}/2$, as illustrated in Figure 3. One possible way of generating the modified references is as follows:

$$V'_x = \begin{cases} V_x - \left(N/2 - 1\right)V_{dc}, & \text{if } V_x > V_m \\ \left(V_x + \dfrac{(N-1)}{2}V_{dc}\right) \bmod (V_{dc}) - \dfrac{V_{dc}}{2}, & \text{if } -V_m \le V_x \le V_m \\ V_x + \left(N/2 - 1\right)V_{dc}, & \text{if } V_x < -V_m \end{cases} \quad x = a, b \text{ or } c \tag{1}$$

where: $V_m = (N-1)V_{dc}/2$, $V_a = V_{ref}\cos(\omega t)$, $V_b = V_{ref}\cos(\omega t - 2\pi/3)$, $V_c = V_{ref}\cos(\omega t + 2\pi/3)$

The major advantage of this transformation is that it then allows the rich pool of knowledge that is available regarding two-level modulation to be immediately applied to multilevel modulation. For example, it is now immediately clear that the inverter switching can be limited to those 19 "allowed" states that have $|V_{cm}| < V_{dc}/3$, by adding an additional common mode offset to the references so as to eliminate the effective null {0, −1, −1} shown in Figure 3. (This is similar in concept to conventional two-level discontinuous modulation.)

From Figure 3, the required offset can be determined to be:

$$V_{off} = sign(V'_{\max}) * V_{dc}/2 - V'_{\max} \tag{2}$$

$$V'_{\max} = \begin{cases} V'_a, & \text{if } |V'_a| \ge |V'_b|, |V'_c| \\ V'_b, & \text{if } |V'_b| \ge |V'_c|, |V'_a| \\ V'_c, & \text{if } |V'_c| \ge |V'_a|, |V'_b| \end{cases} \tag{3}$$

which in fact is the same equation as is used for 60°-discontinuous two-level modulation [11]. (For interest, it is also noted that by applying the appropriate offset equation for continuous two-level SVM to the modified references, continuous multilevel centered SVM as proposed in [7] can be achieved.)

The final reference signals V''_x ($x = a,b,c$) are then created by adding the triplen offset to the original references, i.e.

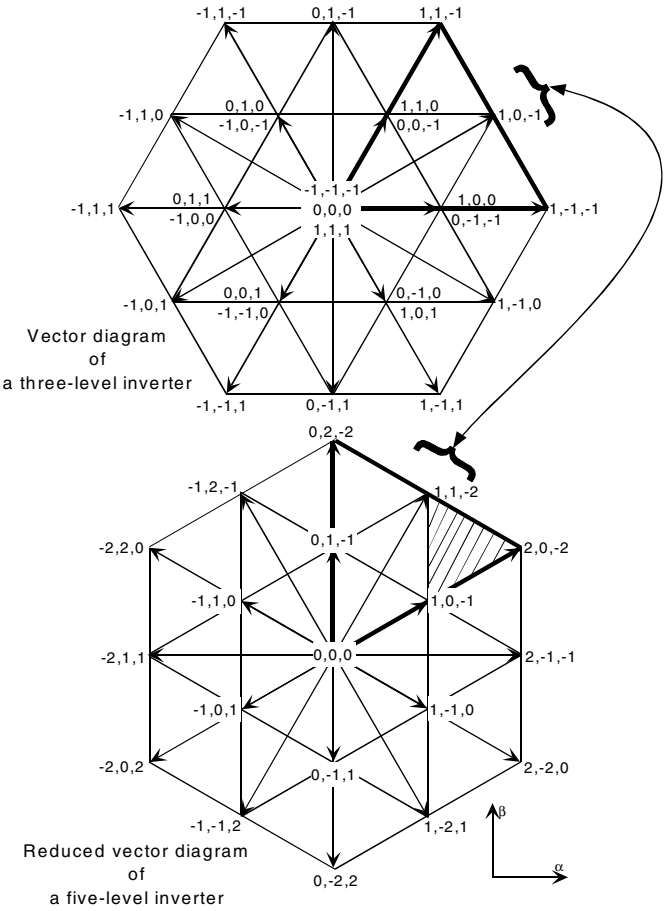

Figure 5: Linkage between vector diagrams of three-level and reduced common mode five-level inverters.

$$V''_x = V_x + V_{off} \tag{4}$$

The same offset equations can obviously be readily applied to higher level inverters, to ensure that only the redundant switching states with the minimum generated common mode voltages are used for each possible space vector. Hence the approach is general for any level inverter.

B. Complete Common Mode Elimination (CCME)

Although effective, the previous technique achieves only partial reduction of common mode voltage. However, for multilevel inverters with an odd number of levels, the common mode voltage can be completely eliminated by further restricting the inverter switching to those states that have no common mode voltage, albeit at the cost of a slight modulation depth limitation and some harmonic degradation [6, 10]. For a three-level and a five-level inverter, the constrained switching states under these conditions are shown in Figures 4 and 5 respectively.

These constraints have been applied to modulation of a three-level NPC inverter by developing an "averaged" reference waveform that combines the three phase sinusoidal references to constrain the switching processes [6]. But the approach does not link the derived reduced common mode PWM strategy to its associated space vector switching

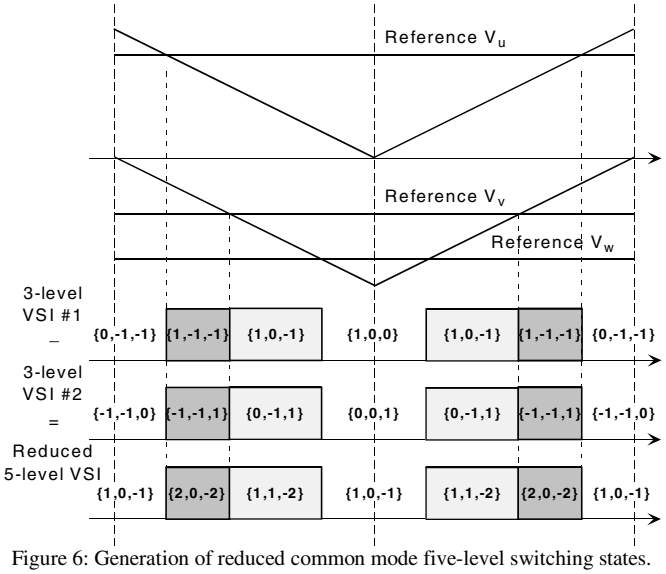

Figure 6: Generation of reduced common mode five-level switching states.

patterns. In this paper, a more general approach is presented which can again be applied to higher-level inverters without difficulty.

As can be seen from Figures 4 and 5, it can in general be stated that the reduced common mode vector diagram of a *N*-level inverter simplifies to that for a conventional $((N+1)/2)$-level inverter with a 30° phase displacement. Each of these reduced space vectors are also now related to only a single switching state, with no redundancy. As well, for carrier disposition PWM, the number of carrier bands must be reduced to $(N-1)/2$, to accommodate the reduced number of switching states remaining.

If the vector diagrams of a conventional three-level inverter and a reduced common mode five-level inverter are compared, as in Figure 5, it is observed that switching states on the reduced five-level diagram can be derived by taking the differences between adjacent state indexes of their matched counterparts on the conventional three-level diagram. For example, state {1, 0, -1} on the reduced five-level diagram can be obtained by subtracting between the state indexes of either {1, 0, 0} or {0, -1, -1}. Hence the required phase leg states of the reduced common mode inverter can be determined by simple combinational subtraction of the switching outputs created by modulation of the equivalent conventional lower order inverter.

For diode-clamped inverter, this subtraction must be implemented explicitly because of a lack of phase-leg redundancies (i.e. possible switch combinations to achieve each output state). One approach would be to logically recombine the output states of the lower order modulator to create gating signals for the inverter that is operating under reduced common mode switching. (Similar to the transformation of modulation states of a VSI to those of a CSI proposed in [12].)

For a cascaded inverter, the subtraction can be done implicitly by taking advantage of the increased number of redundancies available with this converter topology.

For example, for the 5-level cascaded inverter shown in Figure 1(b), two three-level three-phase modulators can be used, with the first modulator controlling phase-legs S_{A2} and S_{A4}, S_{B2} and S_{B4}, and S_{C2} and S_{C4} for each reference phase respectively, and the second modulator controlling phase-legs S_{A1} and S_{A3}, S_{B1} and S_{B3}, and S_{C1} and S_{C3} similarly. Both modulators use the same carriers and phase rotated three-phase command references, i.e. if the first modulator is controlled such that $V_u \rightarrow$ phase A, $V_v \rightarrow$ phase B, and $V_w \rightarrow$ phase C, then the second modulator is controlled such that $V_v \rightarrow$ phase A, $V_w \rightarrow$ phase B, and $V_u \rightarrow$ phase C,

where: $V_u = V_{ref} \cos \omega t$

$$V_v = V_{ref} \cos(\omega t - 2\pi/3)$$

$$V_w = V_{ref} \cos(\omega t + 2\pi/3).$$

By using the same carriers, both modulators switch at the same time instants, while rotating the references effectively rotates the switching state indexes. Hence if, for example, the output state of the first modulator is {1,0,0} then the output state of the second modulator will be {0,0,1} starting at the same time instant and lasting for the same time duration.

Using this approach, the output of the overall five-level cascaded inverter, which is the difference between these two three-level inverters, will always be constrained to the "allowed" switching states of Figure 5. Figure 6 illustrates this process for one switching cycle, and shows the mapping between switching states of a conventional three-level inverter and the reduced common mode five-level inverter. (Note that the fundamental references of the five-level inverter are now given by V_{uv} (= V_u – V_v), V_{vw} and V_{wu} which explains the 30° phase displacement between the two vector diagrams in Figure 5.) The approach is obviously applicable to higher level inverters and as for conventional carrier-based approach, other variations through the addition of suitable triplen offsets are also possible. These issues are relatively straightforward and will not be pursued any further in here.

III. Graphical Mapping of Carrier Disposition PWM to Cascaded Inverters

In this section, a simple graphical technique is presented that maps the switching transitions of any carrier disposition PWM strategy for a NPC inverter directly to a cascaded inverter without requiring complex mathematics. The technique is verified using conventional carrier disposition modulation, and is then applied to determine the switching instances for the previously developed reduced common mode PWM strategies, applied to cascaded inverters.

A. Phase-Shifted Carrier PWM derived from Carrier Disposition PWM

Carrier disposition PWM for a *N*-level diode-clamped inverter arranges *N*-1 carriers with the same frequency and magnitude so that they fully occupy contiguous bands

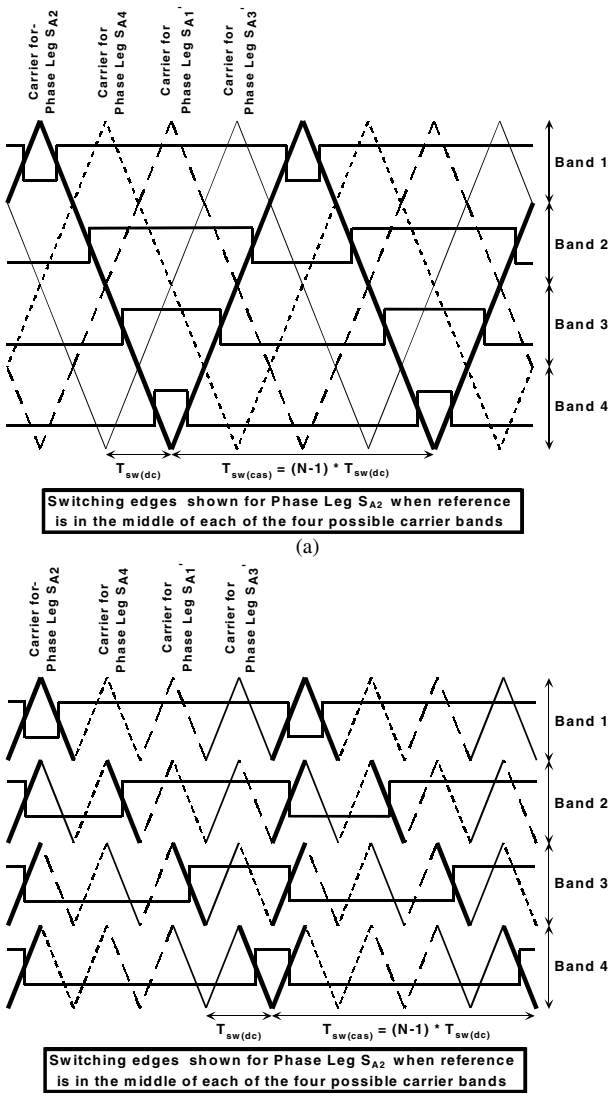

Figure 7: Derivation of cascaded inverter PWM from NPC carrier disposition PWM (a) APOD strategy (b) PD strategy.

spanning the DC link voltage, as shown in Figure 7 for the Alternative Phase Opposition Disposition (APOD – 180° phase shift between adjacent carriers) and Phase Disposition (PD – no phase shift between carriers) strategies. It is generally accepted that the PD strategy creates the lowest line voltage harmonic distortion [2, 3].

With carrier disposition modulation, every intersection of each phase-leg reference with a falling carrier segment causes the output to switch up by one voltage level, while every intersection of the phase-leg references with a rising carrier segment causes the output to switch down by one voltage level. For a diode-clamped inverter, all switching transitions within each carrier band are assigned to a complementary switch pair which increments or decrements the output by one DC level depending on their status.

To achieve the same modulation strategy for a cascaded inverter, each switching transition needs to be assigned to the inner H-bridge phase-legs so as to increment or decrement the output voltage in the same way as for the diode-clamped inverter. In addition, the redundant switching alternatives of a cascaded inverter mean that a further allocation criterion must also be used, and this is typically to balance switching transitions across all switching devices (i.e. across the inner H-bridge phase-legs).

One possible allocation is to cyclically assign switching transitions within each carrier band to successive H-bridge phase-legs of the cascaded inverter; i.e. to the rising and immediate falling carrier segments of band 1, the rising and second falling segments of band 2, the rising and third falling segments of band 3, and the rising and fourth falling segments of band 4. This is shown in Figure 7(a) for the APOD carrier disposed strategy, with the carrier segments and switch transitions associated with phase-leg S_{A2} bolded, and the assigned carrier segments of the other phase-legs shown in different dash patterns. Note that the switching transitions for phase-legs S_{A1} and S_{A3} are assigned to the complementary switches S'_{A1} and S'_{A3}. This reflects the need to invert the switching of these phase-legs to produce the same voltage step directions in the overall phase-leg output.

Allocating the switching transitions in this way produces the well-established phase-shifted carrier strategy for a cascaded inverter, with a carrier phase shift between the internal H-bridges of 180°/(no. of H-bridges) [5]. (Note that the carrier/reference comparisons for phase-legs S_{A1} and S_{A3} for three-level H-bridge modulation are normally achieved by comparing the unshifted carriers for phase-legs S_{A2} and S_{A4} against a 180° phase-shifted reference – this achieves the same result as for the 180° shifted carrier/same reference comparisons that create the switching transitions allocated in a complementary fashion to phase-legs S'_{A1} and S'_{A3}, as shown in Figure 7(a)).

An alternative switching edge allocation is shown in Figure 7(b) for the PD disposed carrier modulation strategy reported in [4]. This produces a PD equivalent modulation for a cascaded inverter with each inner phase-leg switching continuously. This modulation strategy has no easy mathematical equivalent, which in turn demonstrates the usefulness of the graphical approach for matching diode-clamped inverter modulation strategies to cascaded inverter modulation strategies. Note also that such carrier arrangement cannot be easily implemented with a DSP configured to do continuous UP/DOWN counting and can introduce additional switching or commutation difficulties at carrier breakpoints.

B. Cascaded Inverter Discontinuous PWM derived from Carrier Disposition PWM

Another graphical approach to derive PWM strategies for cascaded inverters can be adopted if cyclic distribution of switching stresses among power devices within $T_{sw(cas)}$ is not required. In this case, the allocation is arranged so that only one H-bridge phase-leg switches within each disposed carrier band as shown in Figure 8. Consequently, each H-bridge now switches in a discontinuous modulation strategy, identically

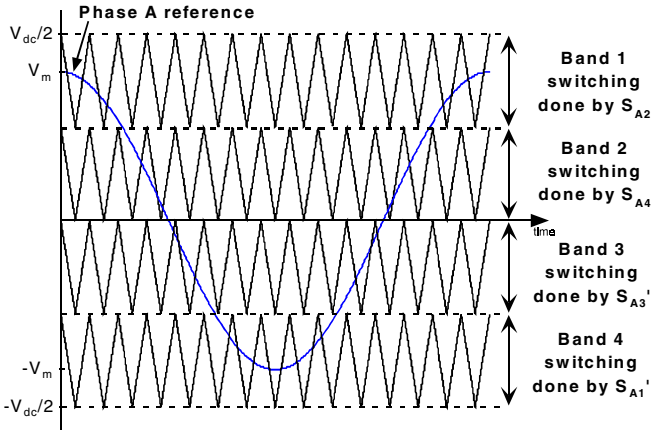

Figure 8: Derivation of discontinuous PD strategy: switching band allocation for each H-bridge phase-leg.

to the strategy developed in [2] for the PD disposed carrier strategy. Of course, such an allocation could equally be applied to other carrier disposition strategies to derive a range of discontinuous equivalent strategies for cascaded inverters. And as expected, all these discontinuous strategies will have the same switch utilization as for the diode-clamped topology.

Note also that it would be a straightforward variation to rotate the discontinuous switching cyclically across multiple H-bridge phase-legs to equalise the switching losses. This is a relatively trivial extension and is not discussed further. But in passing, it is commented that this approach might be appealing with the PD strategy as it is more easily implemented as compared to the phase-shifted version as presented in Figure 7(b). On the other hand, for the APOD strategy, both phase-shifted and discontinuous approaches are equally feasible and preference should be given to the phase-shifted approach in Figure 7(a) as it achieves a more uniform distribution of switching stresses.

C. Reduced Common Mode PWM for Cascaded Inverters

For the PCME modulation approach presented in Section II(A), the number of NPC inverter carrier bands needed (N-1) is the same as for conventional modulation and hence the cascaded-inverter switching instants are also given by Figures 7 and 8.

For the CCME approach presented in Section II(B), the number of NPC carrier bands reduces to ((N-1)/2) but the same graphical analysis approach is still applicable. For example, if the switching transitions produced by the comparison of the three-phase references against reduced APOD carrier bands are allocated to the cascaded inverter inner phase-legs, the result is again phase-shifted carrier PWM, but with a carrier phase shift of 360^o/(no. of H-bridges) instead of 180^o/(no. of H-bridges) as before. (The mathematical verification of this phase shift has been confirmed using Double Fourier Series analysis but is not presented here because of space limitations.)

The reference/carrier comparisons used to determine the switching transitions with a reduced PD carrier pattern are shown in Figure 9, with the transitions directly matched to

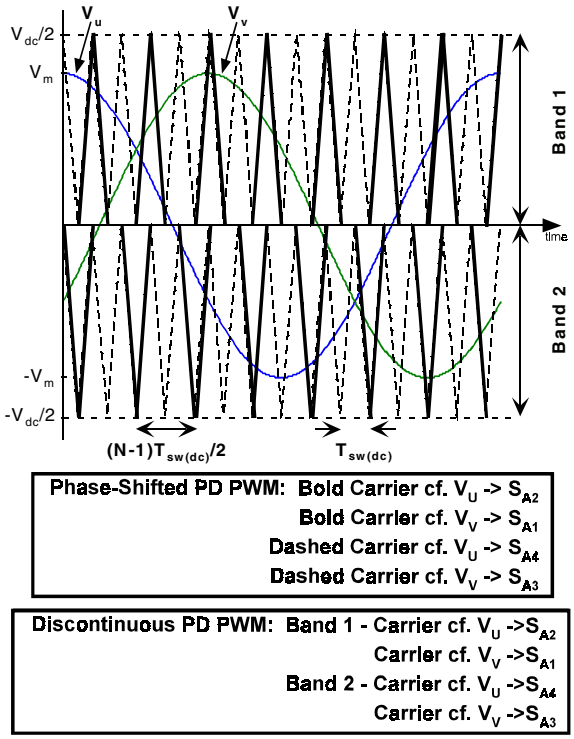

Figure 9: Derivation of carrier placements for phase-shifted and discontinuous CCME-PD for cascaded five-level inverter.

the modulation of each H-bridge phase-leg as listed. Once again, both a continuous and a discontinuous switching arrangement are possible. An interesting observation with the CCME approach is that for a cascaded inverter with ($4k$ – 1) DC levels, where k is an integer, there will be a carrier band centered along the zero reference line. This is quite unlike conventional PWM for odd-level inverters, where the carrier bands are always either above or below the zero line.

IV. Simulation and Experimental Results

The modulation strategies derived above have been verified both in simulation and experimentally. All simulation studies were developed using MATLAB and included practical effects such as regular sampling and dead-time delays to match the expected experimental system performance as closely as possible. The experimental results were obtained using a cascaded five-level inverter, with each H-bridge being driven from a separate DSP controller. The PWM operation of each controller was very carefully synchronised to maintain an exact phase relationship between their carriers and fundamental references, as is required of course to achieve the expected harmonic cancellation.

Figures 10 and 11 show the simulated waveforms and harmonic spectrum using conventional discontinuous PD PWM at 90% modulation. Note in particular the substantial common mode voltage that is generated with a concentration of energy at the carrier harmonic. This carrier harmonic will be cancelled in the line voltage spectrum and is the main reason for the improved performance of PD strategy as compared to APOD as mentioned in [2]. But unfortunately,

the carrier component remains in the common mode spectrum and must be considered when selecting modulation strategies from a common mode perspective.

Figures 12 and 13 show the simulated waveforms and common mode spectrum for phase-shifted PCME-APOD strategy under the same modulation conditions. Note the substantial reduction of common mode voltage and the absence of the carrier harmonic (due to the use of APOD). In passing, it is commented that the baseband low frequency harmonics are due to the adding of triplen offsets for the PCME approach.

Figures 14 and 15 show the experimental waveforms and common mode spectrum using phase-shifted CCME-APOD while Figures 16 and 17 show the results with discontinuous CCME-PD. The third traces of Figures 14 and 16 confirm that the common mode voltage has been virtually eliminated with only common mode switching spikes occurring during dead-time intervals. (The origin of these common mode spikes is the need to simultaneously switch both phase-legs, which cannot always be guaranteed during dead-time.) Note also that for CCME strategies, baseband, carrier and sideband common mode harmonics are removed regardless of whether APOD or PD is used. PD should therefore be the preferred strategy as it also achieves a better line voltage performance. Finally, it is commented that with the same switching frequency, the first harmonic sidebands of the CCME strategies occur at half the frequency of conventional strategies, because every state transition now requires the switching of two phase-legs.

V. Conclusion

This paper presents reduced common mode carrier-based PWM strategies for cascaded inverters. Two approaches are presented with fundamental reference offsets determined using constrained space vectors and switching transitions graphically matched from the well-established carrier disposition PWM strategies. Both continuous and discontinuous switching strategies are presented and have been verified by simulation and experimental results to be very effective in substantially reducing common mode voltage.

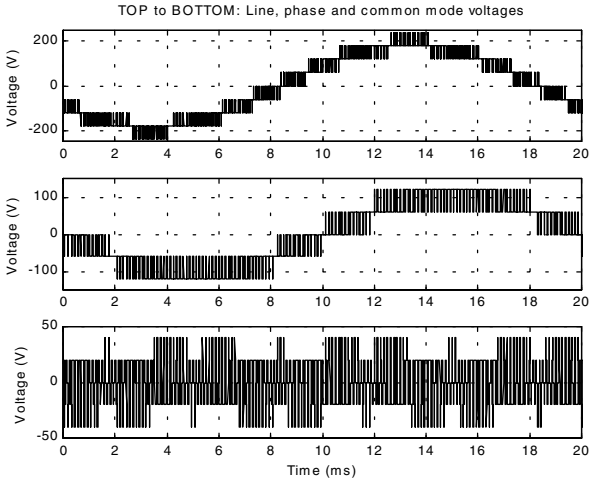

Figure 10: Simulated waveforms using conventional discontinuous PD – *(1) line voltage, (2) phase-leg voltage, (3) common mode voltage.*

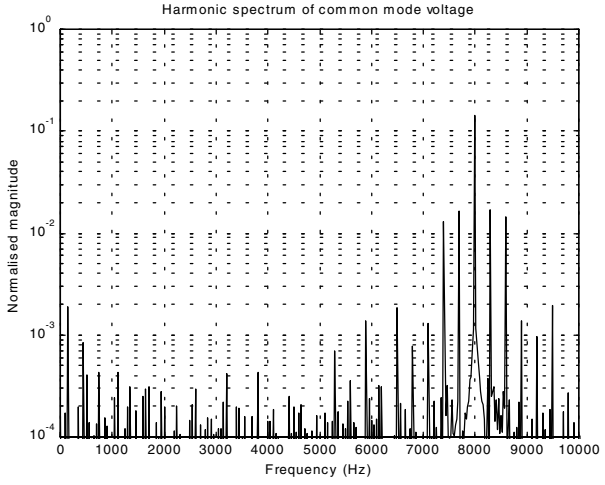

Figure 11: Simulated spectrum of common mode voltage using conventional discontinuous PD – normalised to line fundamental voltage magnitude.

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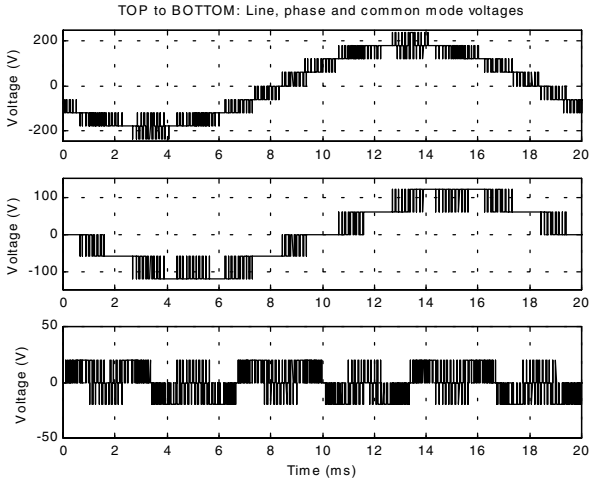

Figure 12: Simulated waveforms using phase-shifted PCME-APOD – *(1) line voltage, (2) phase-leg voltage, (3) common mode voltage.*

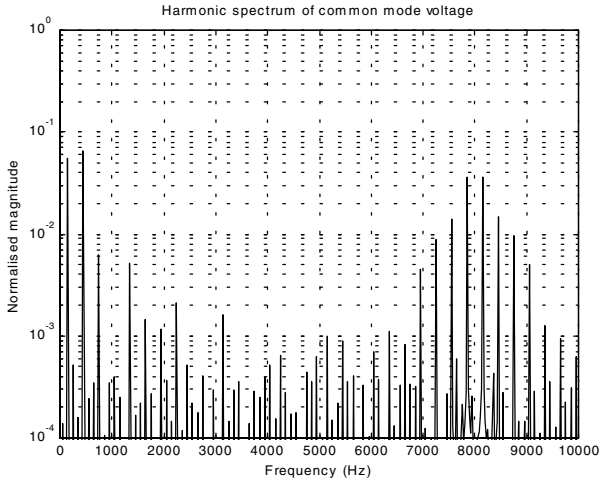

Figure 13: Simulated spectrum of common mode voltage using phase-shifted PCME-APOD – normalised to line fundamental voltage magnitude.

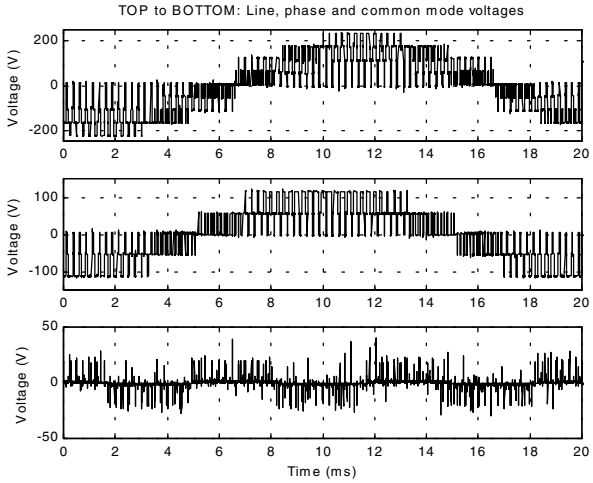

Figure 14: Experimental waveforms using phase-shifted CCME-APOD – *(1) line voltage, (2) phase leg voltage, (3) common mode voltage.*

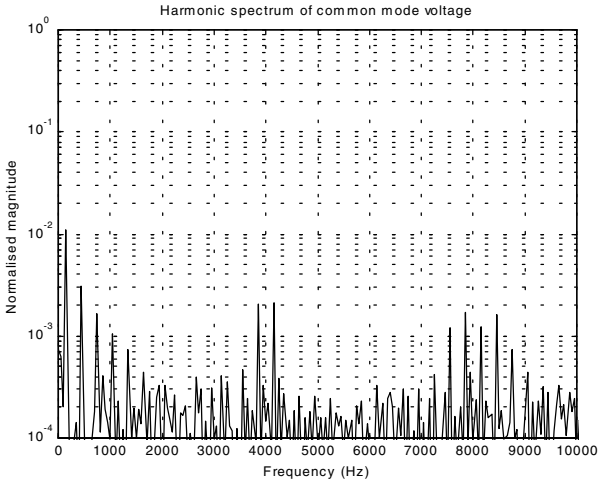

Figure 15: Experimental spectrum of common mode voltage using phase-shifted CCME-APOD – normalised to line fundamental voltage magnitude.

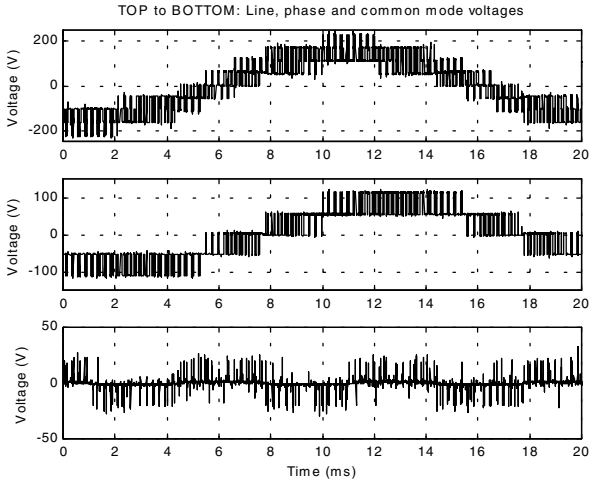

Figure 16: Experimental waveforms using discontinuous CCME-PD – *(1) line voltage, (2) phase leg voltage, (3) common mode voltage.*

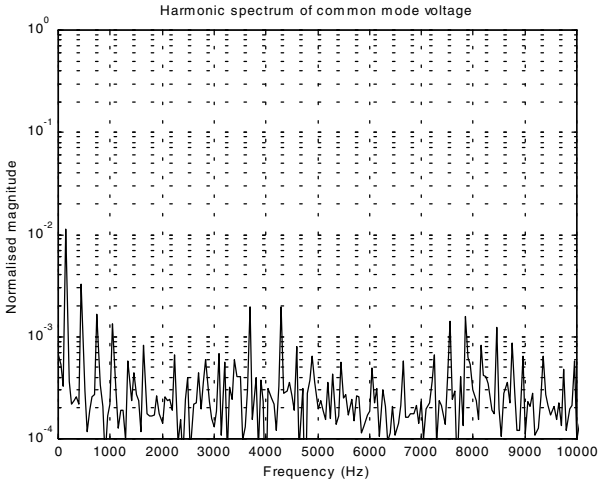

Figure 17: Experimental spectrum of common mode voltage using discontinuous CCME-PD – normalised to line fundamental voltage magnitude.