A Time-Based Double-Band Hysteresis Current Regulation Strategy for Single-Phase Multilevel Inverters

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***Abstract*—Most multilevel inverter hysteresis current regulators use either multiple hysteresis bands, or a time-based switching logic that forces the current error back to zero by recursively stepping through successive voltage levels. Of these two alternatives, the time-based approach has the merit of only requiring simple analog circuitry and digital logic to implement the voltage level selection process for inverters of any number of voltage levels. However, the approach can be less stable and has a poorer dynamic response than a multiple hysteresis band system. This paper presents a double-band regulator that uses the slope of the current error to help determine the appropriate steady state voltage level to keep this error within the inner hysteresis band, while still allowing switching to the extreme inverter states during transient conditions to reduce the current error as rapidly as possible. The regulator achieves better stability and dynamic performance than previously reported schemes. The paper also presents an adaptation of the system to control a hybrid seven-level inverter. Theory, simulation, and experimental results are presented.**

***Index Terms*—Current control, digital logic synthesis, hybrid inverters, hysteresis, multilevel inverters.**

I. Introduction

MULTILEVEL inverters are now becoming an established topology for use in higher power applications, where they offer the advantage of substantially lower harmonic content in the output voltage for a given switching frequency, together with significantly reduced switching stresses. Furthermore, multilevel topologies can achieve, by cascading switching levels, an increased range of power levels that cannot be matched by any two-level inverter topology.

Modulation control of a multilevel inverter is usually achieved using open-loop pulsewidth-modulation (PWM) strategies, which are well established with the merits of the various alternatives well reported. These strategies can be readily used with a synchronous frame proportional plus integral (PI) regulator or a deadbeat regulation strategy to create a current regulated multilevel system, in much the same way that a two-level inverter can be current regulated.

An alternative way to regulate current through a multilevel inverter is to use hysteresis comparison to determine the switching instants of each phase leg. As with all hysteresis systems, this approach would be expected to have a fast dynamic response and a continuous spread harmonic spectrum [1]–[11]. Various strategies are available also to vary the hysteresis band to narrow the switching frequency range for applications where this is desirable [1], [2]. However, in all cases, the essential problem is to select the appropriate inverter phase-leg voltage level that forces the current error back toward zero once it exceeds certain bounding limits.

One approach is to use multiple hysteresis bands, with each band representing switching between two adjacent voltage levels [1], [3]–[9] and where the number of bands required is one less than the number of dc levels of the inverter. The approach is robust and has a fast response but requiring increasingly complex analog circuitry for implementing the multiple bands and offset compensation as the number of inverter dc voltage levels increases [3], [5].

An alternative time-based approach is to use only one hysteresis band to detect an out-of-bounds current error, with digital logic added to help select the appropriate switched voltage level to reduce this error. Both minimum time delay between successive voltage steps [3], and detection of reversal of the slope of the current error [10], have been used in this context. These strategies require only simple analog circuitry, with any complexity caused by an increasing number of inverter dc levels easily incorporated within the programmable logic device used for implementing the voltage selection logic. However, the approaches reported so far lack robustness and/or have a poor dynamic response to transient changes in the current error.

This paper presents an improved time-based current regulator, which uses a double hysteresis band strategy to achieve excellent steady state control together with a fast dynamic response. The inner hysteresis band and the slope of the current error are used to select the appropriate inverter voltage level to force the error back toward zero without overshoot and oscillation under normal operating conditions. However, during transient events the outer hysteresis band forces the use of the ex-

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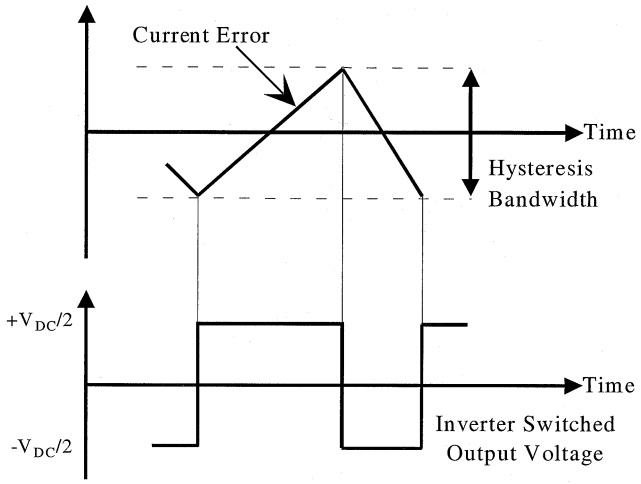

Fig. 1. Conventional two-level hysteresis current regulation.

treme dc levels so as to drive the current error back to within the inner hysteresis band as fast as possible.

The approach has also been applied to a hybrid seven-level inverter [12], where the logic after the hysteresis comparisons must select from redundant inverter states as particular voltage level transitions occur. The principles presented have been verified by both detailed MATLAB simulation and experimental investigations.

II. Multilevel Hysteresis Current Regulation

A. Two-Level Hysteresis Current Regulation

Conventional two-level hysteresis current control operates by comparing a current error (i.e., the difference between measured and demanded phase currents) against a fixed hysteresis band. When the error falls below the lower hysteresis limit, the inverter phase-leg output is switched high, and when the error rises above the upper hysteresis limit, the inverter output switches low. This process is illustrated in Fig. 1

As only two dc voltage levels are available, two-level hysteresis current regulation is relatively straightforward with each hysteresis boundary being mapped essentially to one inverter phase-leg switched state.

B. Multilevel Hysteresis Current Regulation

For a multilevel inverter, when the current error exceeds a hysteresis boundary, the next higher (or lower) voltage level should be selected in order to ensure a single switch commutation to the new inverter state. However, this new inverter state may not be adequate to force the current error to begin to return to zero. In this case, the inverter should switch to the next higher (or lower as appropriate) voltage level, and the process should cease only when the "correct" voltage level is selected that reverses the current error direction.

One possible technique that can be used to assist the current regulator in selecting the "correct" voltage level is the use of multiple hysteresis bands. For an N-level inverter, $N-1$ bands are required with each band representing the switching between two adjacent voltage levels. A possible double-band arrangement for controlling a three-level inverter is shown in Fig. 2.

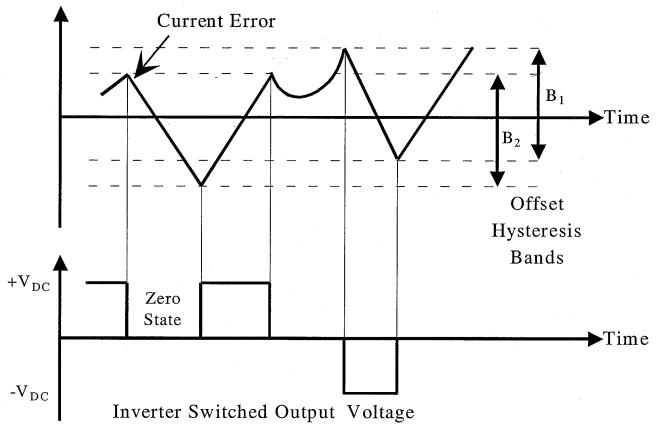

Fig. 2. Multiband multilevel hysteresis current regulation.

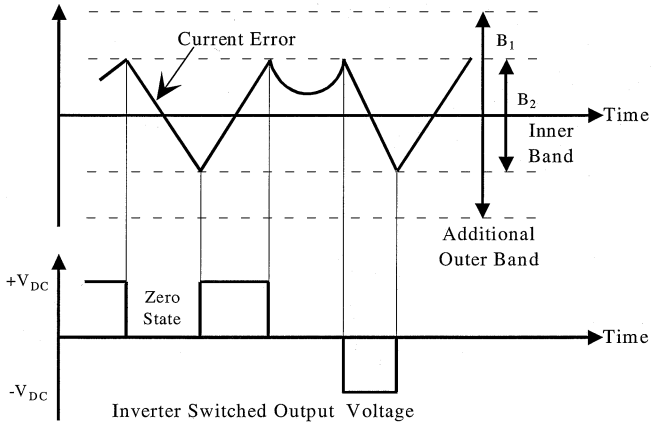

Fig. 3. Time-based multilevel hysteresis current regulation.

As can be seen from Fig. 2, one disadvantage of this scheme is that the offset placements of hysteresis bands about zero error introduce a steady-state tracking error, and an offset compensation strategy to ensure zero average current error within each switching period is required for improved performance [3], [5]. The technique is robust but has the general limitation of requiring increasingly complex analog circuitry for implementing the multiple hysteresis bands and offset compensation as the number of voltage levels increases.

An alternative (time-based) technique is to use only one hysteresis band to detect a current error out of bounds, with digital logic to select the "correct" voltage level in response when this occurs [3], [10]. A possible current error trajectory and inverter switched output for a three-level inverter are shown in Fig. 3. From this figure, it is obvious that the technique does not create the steady-state tracking error of the multiple band approach and will also require significantly simpler circuitry irrespective of the number of inverter voltage levels. However, with a simple implementation, the technique lacks robustness and has a poor transient response.

III. Improved Time-Based Current Regulation

A. Steady-State Performance Analysis

The first time-based hysteresis regulator was reported by Marchesoni *et al.* [3], and has the structure shown in Fig. 4(a) (Path (1) only). The regulator uses a single hysteresis band

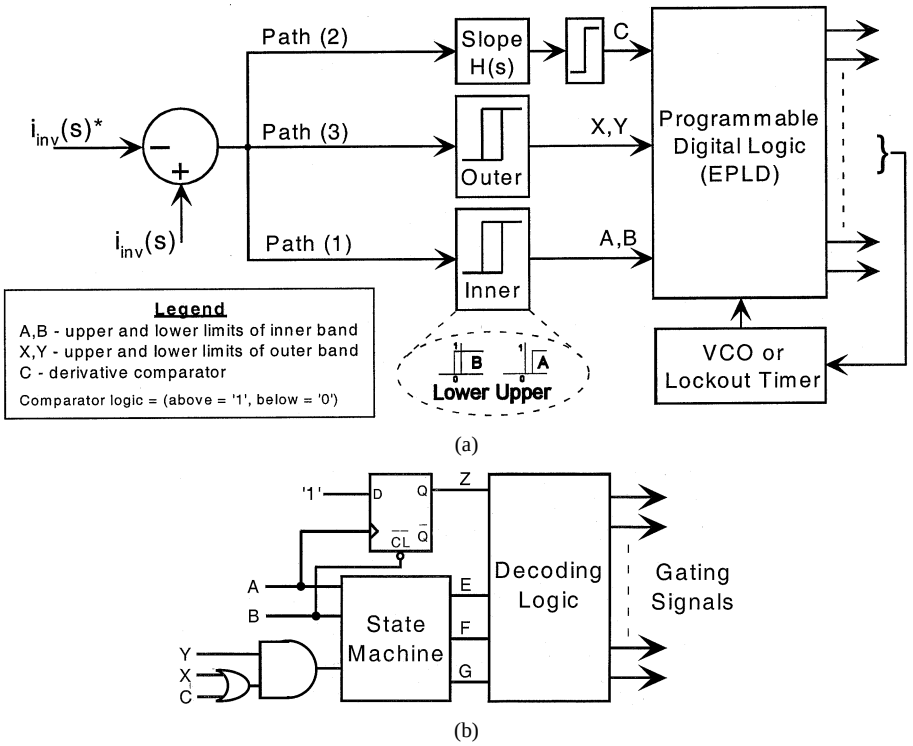

Fig. 4. Time-based hysteresis current regulator. (a) General layout. (b) Digital logic.

to detect when the inverter should switch, together with a voltage-controlled oscillator (VCO) that periodically increases (current error below the lower limit) or decreases (current error above the upper limit) the switched output voltage by one level after a fixed time period $t_{\rm step}$. The voltage level stepping ceases when the current error is driven back within the bounding hysteresis limits.

This approach can cause oscillations of the output voltage when $t_{\rm step}$ is too short, especially when transiting from switching between two dc levels to switching between the next two levels. Precise tuning of $t_{\rm step}$ is, therefore, required to achieve stable steady-state operation and the regulator generally lacks robustness.

An improved approach was proposed by the authors [10], based on detecting the slope of the current error [Path (2) in Fig. 4(a)]. With this approach, when the current error exceeds the upper (or lower) boundary, the digital logic switches the inverter down (or up) one voltage level so as to return the error back to zero, as before. However, if the new inverter switched state is inadequate to reverse the error back to zero, it will need to be further switched down (or up) until the current error direction reverses. This point can be detected by a change in the current error slope.

It should be noted that a lockout delay is still needed with this regulator to freeze the switching process for a fixed duration immediately after an inverter state change to compensate for short delay between the generation of gating signals and sensing of the current error and its derivative. This delay, however, is small and can be easily tuned based on the parameters of the selected sensing device and differentiator logic.

The state sequence logic transitions for this scheme for a three-level, a five-level and a seven-level inverter are shown in Fig. 5 with the output logic bits *E*, *F*, and *G* indicating the switched state of the inverter. These bits are subsequently passed into decoding logic as illustrated in Fig. 4(b) to generate the appropriate gate signals for the selected multilevel topology.

B. Transient Performance Analysis

Since the switching process ceases immediately upon reversal of the error slope, the earlier discussed slope detection approach will usually switch only between adjacent voltage levels, with smooth transitions from switching between two adjacent levels to switching between the next two levels as appropriate. However, the transient response is poor, since to have a fast step response the inverter must step rapidly to the extreme switching states so as to reduce the current error as quickly as possible. Stopping at the first voltage level that reverses the slope of the error also reduces the transient performance, since the inverter does not continue to its extreme voltage levels when it should.

A further proposed improvement is therefore to ensure that the process that ceases switching upon selecting the first voltage level to reverse the slope of the current error, is inhibited during transient conditions. Switching then continues out to the extreme voltage levels, and the current error is reduced much more quickly.

An effective way of implementing transient detection is to include an additional outer hysteresis band, as illustrated in Figs. 3 and 4(a) [Path (3)], whose role is to distinguish between steady-state and transient events. Under steady-state conditions, the current error will be confined within the inner band by the slope detection algorithm. When the commanded current step changes so that the current error exceeds the outer hysteresis band, the slope detection algorithm is inhibited by ANDing the derivative

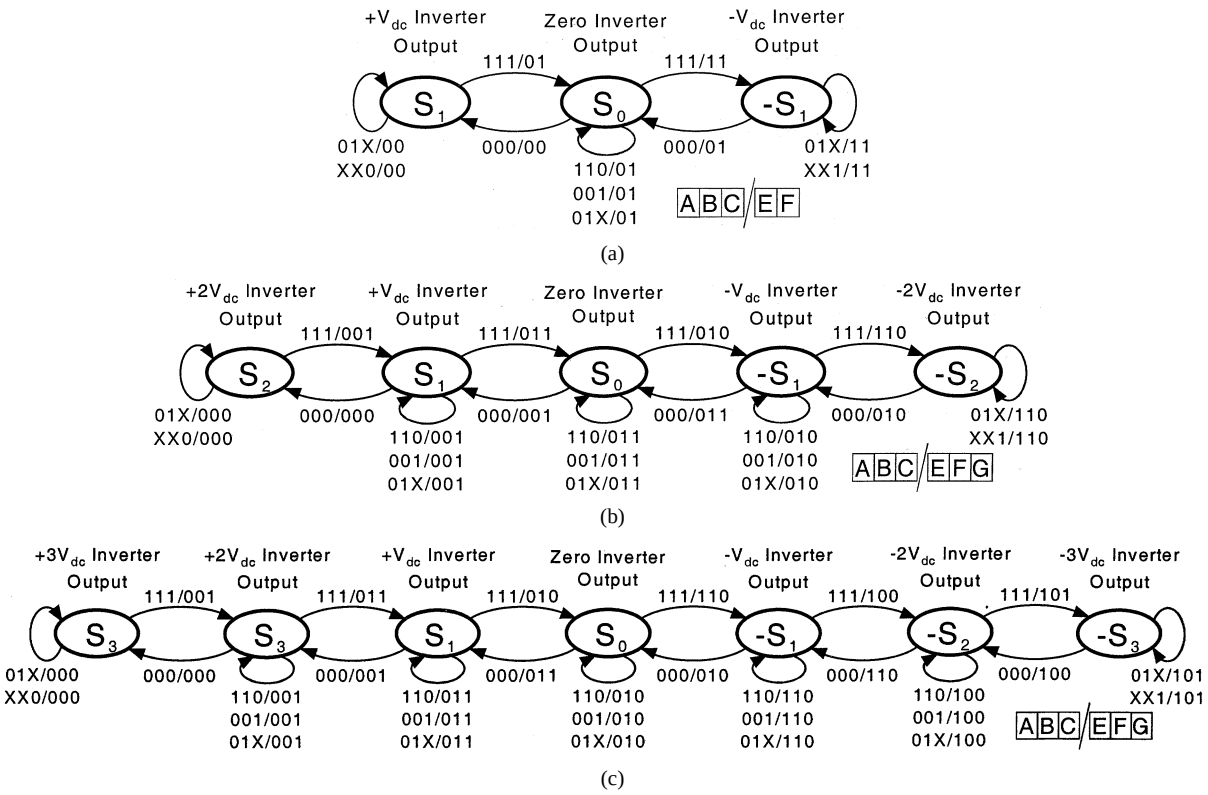

Fig. 5. State machine transitions for (a) a three-level system, (b) a five-level system, and (c) a seven-level system. A, B, and C represent the comparator outputs while E, F, and G represent the logic state bits.

comparator output *C* with the outer band comparator outputs *X* and *Y*, as shown in Fig. 4(b). Hence, the inverter steps rapidly out to the extreme voltage level provided the current error remains outside the outer boundary.

One possible concern is the separation between the inner and outer hysteresis bands. However, since the primary role of the outer band is to detect transient events, the tuning of this separation needs not be as accurate as that needed by the multiple band regulator, where precise offset tuning is required to achieve accurate steady-state reference tracking. Generally, good performance with this scheme can be achieved by simply having an outer band that is twice as wide as the inner band.

IV. Application of Time-Based Double Band Regulation to Hybrid Inverters

The hybrid inverter is basically a cascaded structure that has been modified such that the full bridge inverters that comprise each phase leg utilize different power devices and are supplied from dc sources with different potentials. The topological layout of a single-phase hybrid seven-level inverter is shown in Fig. 6 [12] with its possible switching states given in Table I.

As can be seen, the upper integrated gate commutated thyristor (IGCT) bridge is supplied with $2V_{\rm DC}$ and is referred to as the high-voltage (HV) stage while the lower insulated gate bipolar transistor (IGBT) bridge, supplied with $V_{\rm DC}$, is referred to as the low-voltage (LV) stage. Due to its limited switching ability, the HV bridge is generally controlled to switch at fundamental frequency (quasi-square modulation) and simply reinforces the pulsewidth-modulated LV bridge whenever the latter hits its modulation limit. The HV bridge

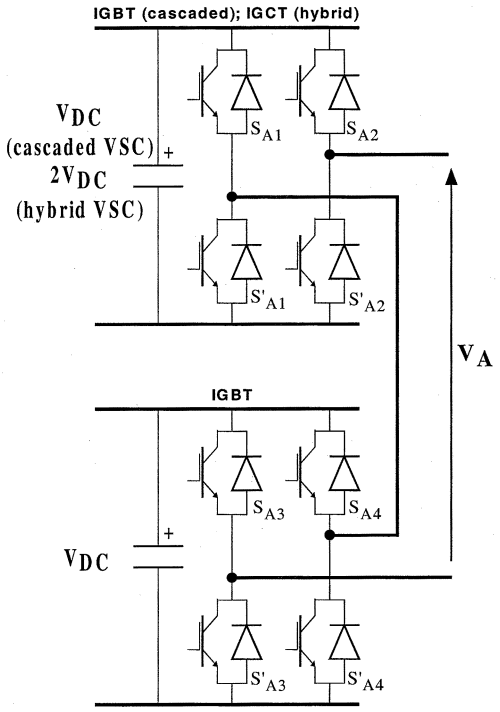

Fig. 6. Single-phase hybrid inverter.

is therefore expected to generate the bulk of the required fundamental voltage, with a significant amount of harmonics produced in the process. The LV bridge produces the remaining fundamental voltage together with harmonics of the opposite polarity to nullify those created by the HV bridge.

From Table I, it can be seen that the hybrid inverter has less redundant switching states than a cascaded seven-level inverter.

TABLE I
SWITCHING STATES OF HYBRID INVERTER

State no.	Phase leg voltage	Switch S_{A2} (!S'_{A2})	Switch S'_{A1} (!S_{A1})	Switch S'_{A3} (!S_{A3})	Switch S_{A4} (!S'_{A4})
1	$3V_{DC}$	1	1	1	1
2	$2V_{DC}$	1	1	1	0
3	$2V_{DC}$	1	1	0	1
4	V_{DC}	1	1	0	0
5	V_{DC}	1	0	1	1
6	V_{DC}	0	1	1	1
7	0	0	1	0	1
8	0	0	1	1	0
9	0	1	0	0	1
10	0	1	0	1	0
11	$-V_{DC}$	1	0	0	0
12	$-V_{DC}$	0	1	0	0
13	$-V_{DC}$	0	0	1	1
14	$-2V_{DC}$	0	0	0	1
15	$-2V_{DC}$	0	0	1	0
16	$-3V_{DC}$	0	0	0	0

Also, restrictions exist in the selection of the redundant states that produce $V_{\rm DC}$ and $-V_{\rm DC}$. For switching between $V_{\rm DC}$ and $2V_{\rm DC}$, the HV stage is tied to $2V_{\rm DC}$ and the LV stage switches between $-V_{\rm DC}$ and 0. Only state 4 can, therefore, be used to produce $V_{\rm DC}$. On the other hand, when switching between 0 and $V_{\rm DC}$, the HV stage is tied to 0 while the LV stage switches between 0 and $V_{\rm DC}$. Hence, only states 5 and 6 can be used. In addition, states 5 and 6 should be cyclically selected (as for the other redundant states) so as to uniformly distribute switching stresses among the switches. Similar restrictions hold for states that produce $-V_{\rm DC}$, with only state 13 being available for switching between $-2V_{\rm DC}$ and $-V_{\rm DC}$, and states 11 and 12 available for switching between $-V_{\rm DC}$ and 0.

The double-band regulation strategy can easily be extended to hybrid inverters if minor additional logic is implemented into the digital logic block to distinguish between the redundant states of $V_{\rm DC}$ and $-V_{\rm DC}$. This logic is easily derived from Fig. 7(a) and (b), which shows how the error trajectory varies within the inner hysteresis band when switching between $V_{\rm DC}$ and $2V_{\rm DC}$, and between 0 and $V_{\rm DC}$. From this diagram, state 4 should be selected when boundary *A* is hit, to achieve the required output of $V_{\rm DC}$, while either states 5 or 6 should be selected when boundary *B* is hit and the output of $V_{\rm DC}$ is again required. Similarly, when switching between $-2V_{\rm DC}$ and $-V_{\rm DC}$, and between $-V_{\rm DC}$ and 0, state 13 must be selected when boundary *B* is hit while states 11 or 12 should be used when boundary *A* is hit.

The logic extension to achieve this result is simple, and requires only an additional D-flip-flop as shown in Fig. 4(b), The output of this flip-flop (Z) identifies which boundary has been exceeded, and is then used with the switching state bits E, F, and G to generate the hybrid inverter gating signals.

V. PHYSICAL IMPLEMENTATION OF CURRENT REGULATOR

The proposed current regulator can be conveniently implemented with low-cost analog op-amps, comparators, and a digital programmable logic device. The general block diagram representation of the regulator is given in Fig. 4(a) with each hysteresis band being implemented with an "upper" and a "lower" comparator (LM311), and the digital logic being implemented in the *Lattice Semiconductor* in-system programmable complex programmable logic device (CPLD) (ispLSI2128E).

The main complication associated with the regulator is its susceptibility to noise amplification while taking the derivative of the current error. Derivative inputs are essentially high-pass filters, and noise injected through these filters can cause the implemented state machine to oscillate rapidly between possible states. This can cause high-frequency limit cycles at the inverter terminal output.

To avoid such complication, a differentiator with a second-order roll-off is adopted for this work. The mathematical formulation of the selected differentiator can be written as

$$\frac{Y(s)}{X(s)} = \frac{Ks}{(s+\omega_1)(s+\omega_2)} \tag{1}$$

where

$Y(s)$ output of the differentiator;

$X(s)$ input to the differentiator;

K gain constant;

ω_1, ω_2 selected decibel cutoff frequencies.

Unfortunately, the two additional poles cause a phase lag in the detection of change of error direction. However, this lag can be compensated within the digital logic state machine by incorporating an appropriate lockout logic to prevent further state changes for a short time interval after a switching event. This allows enough time for any changes to the current error slope caused by a switching event to propagate through the sensor and differentiator before the next switching decision is made. In practice, this lockout delay also defines the maximum allowable switching frequency of the inverter, since an inverter state time cannot be less than this lockout period. Conveniently, this also protects the switching devices from the high switching frequencies, which can occur in a fixed-band hysteresis current control strategy under some load conditions.

VI. SIMULATION AND EXPERIMENTAL RESULTS

The double-band hysteresis current regulation strategy has been simulated using MATLAB Simulink, with major practical limitations such as dead time and system delays taken into consideration so as to match the experimental system as closely as possible. Figs. 8 and 9 show the simulated logic sequences and inverter switched output obtained during the initial regulator design. In these figures, the logic variable *LOCK* represents the signal output from the lockout timer which switches to "0" instantaneously upon inverter state transitions ("0" = lock, "1" = unlock), and logic C (*nonideal*) indicates the direction of the current error using the second order differentiator described in Section V. To clearly illustrate the delay introduced by the

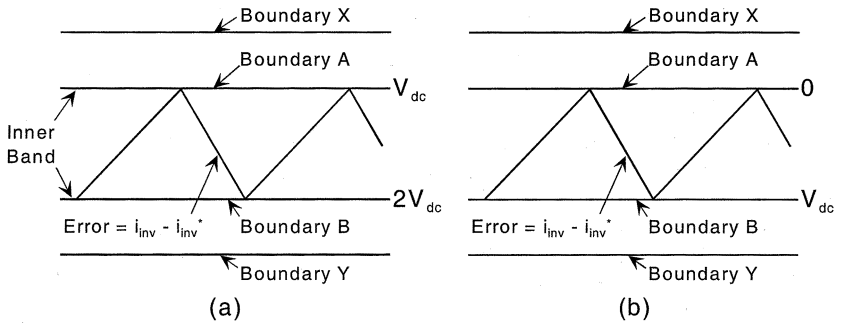

Fig. 7. Current error trajectory within the inner hysteresis band. (a) Switching between $V_{\rm DC}$ and $2V_{\rm DC}$. (b) Switching between 0 and $V_{\rm DC}$.

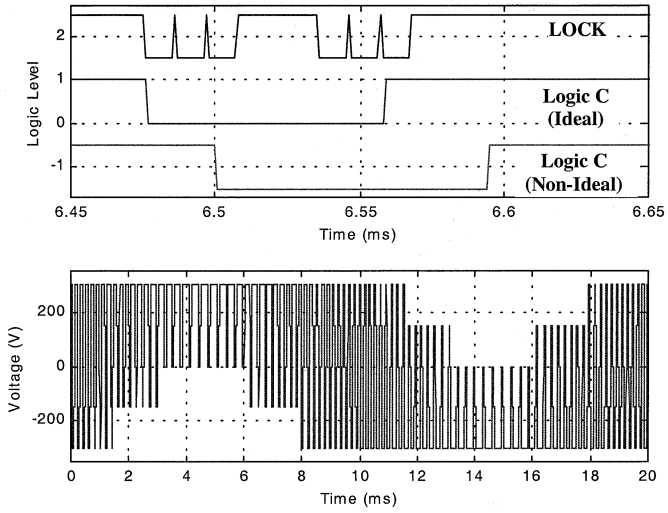

Fig. 8. System performance using a lockout time of 10 μs (five-level inverter). Top: lockout logic LOCK, Logic C without delays (ideal), Logic C with delays (nonideal); bottom: output voltage.

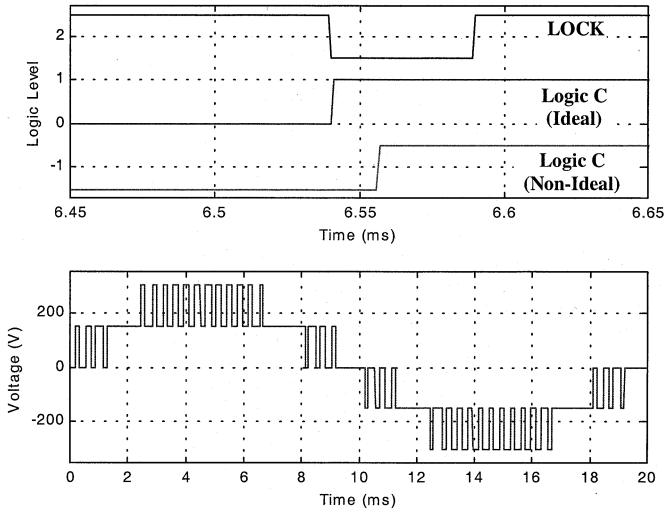

Fig. 9. System performance using a lockout time of 50 μs (five-level inverter). Top: lockout logic LOCK, Logic C without delays (ideal), Logic C with delays (nonideal); bottom: output voltage.

second-order differentiator, the logic signal C (*ideal*) obtained using an ideal differentiator is also included in the figures although this signal is not physically used by the current regulator.

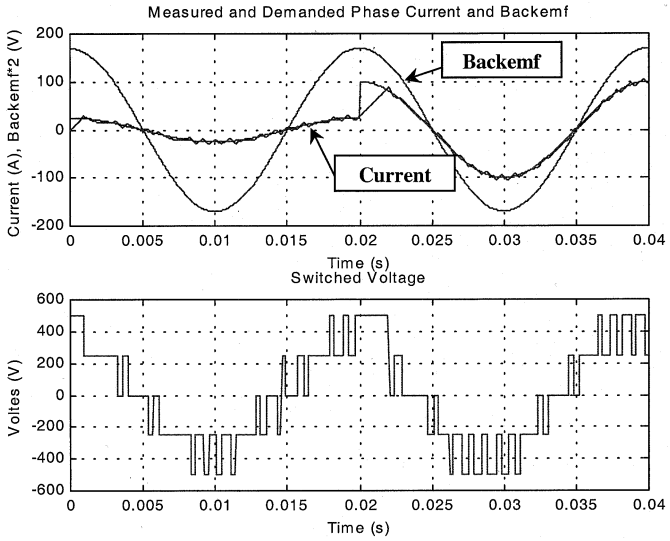

Fig. 10. Simulated transient performance for the case of demanded current in phase with the back EMF (five-level inverter).

In Fig. 8, the logic lockout time is set to 10 μs which is shorter than the combined delay of $\approx$ 30 μs introduced by the current sensor and second-order differentiator. The digital state machine is therefore "unlocked" before the change in current error direction is detected. This causes the inverter to switch unnecessarily, hence, giving rise to the nonideal inverter switched output shown in Fig. 8. By increasing the lockout time to 50 μs, Fig. 9 shows that the inverter achieves optimal single-level switching since the digital state machine is now "unlocked" only after the change in current error direction is detected.

Fig. 10 [commanded current in phase with back electromotive force (EMF)] and Fig. 11 (commanded current in quadrature with back EMF) show the simulation results of a five-level inverter, controlled with the double-band regulator, supplying a load consisting of a resistance $R = 0.5\ \Omega$, an inductance $L = 5$ mH, and a 340 V (peak) back-EMF source. The results show the excellent transient performance of the regulator under a demanded current step from 50 to 100 A.

Figs. 12–14 show the experimental results of the regulator controlling a three-level, a five-level, and a hybrid seven-level inverter, respectively. Note that, for this set of results, the switching frequency has been considerably reduced to clearly illustrate the switching process within a fundamental cycle. It is particularly interesting to observe how the algorithm manages

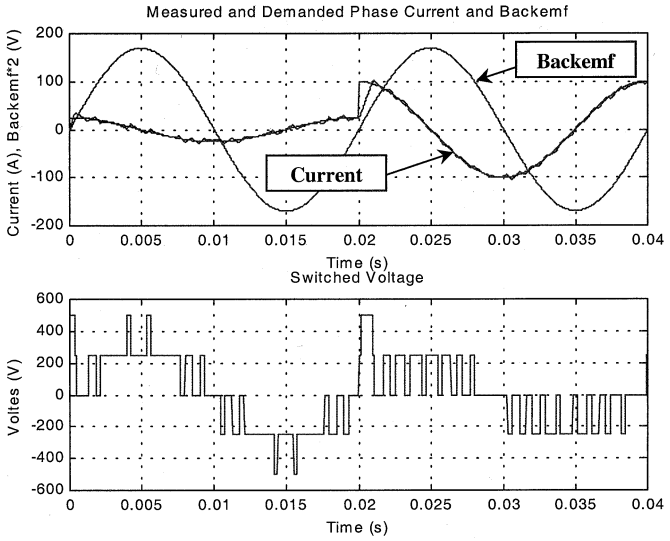

Fig. 11. Simulated transient performance for the case of demanded current in quadrature with the back-EMF (five-level inverter).

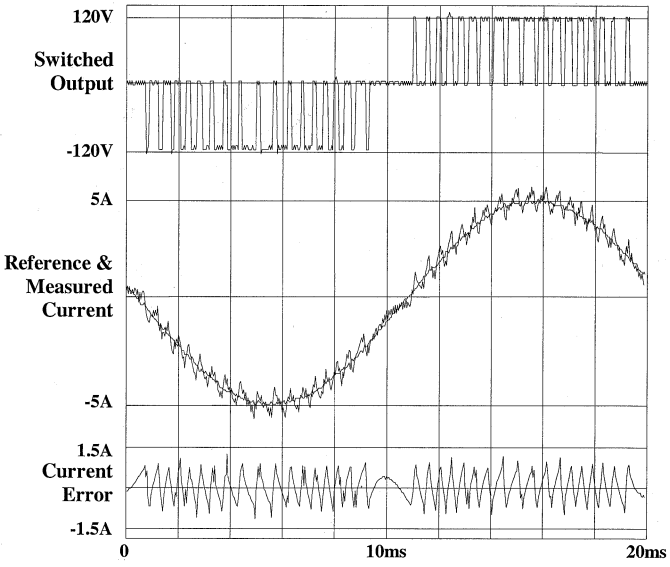

Fig. 12. Experimental steady-state performance (three-level inverter).

the current tracking at instants of transition from switching between two adjacent voltage levels to switching between the next two levels, where the current error direction reverses without any switching. The correct response here is to freeze the inverter switching while the measured current drifts to follow the reference, and this is exactly the approach taken by the algorithm. The excellent tracking performance of the regulator is further confirmed in Fig. 15 which shows the experimental harmonic spectrum of the load current supplied with the hybrid inverter, with no significant lower order harmonics.

Figs. 16 and 17 show the transient performance of the implemented three-level system for the cases of no outer band control and outer band control, respectively, under a step change from no load to full load. As a no load to full load change for a three-level system involves the stepping of only one voltage level (0 to $+V_{\mathrm{DC}}$), no prominent performance difference can be observed in this case. The effectiveness of the outer band control

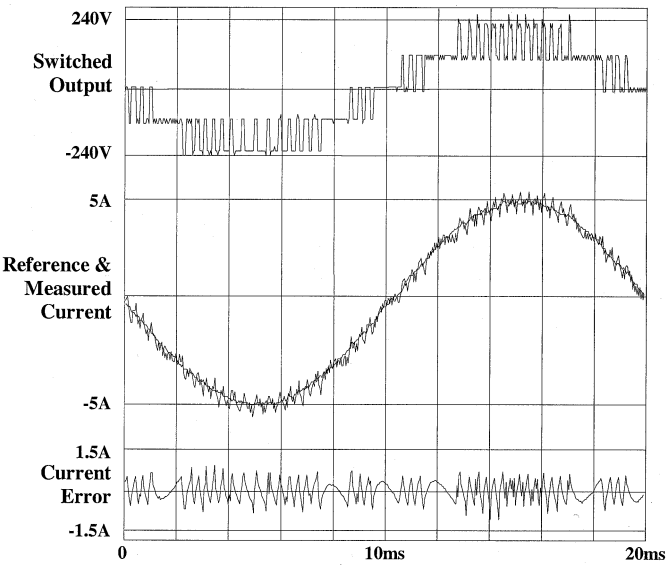

Fig. 13. Experimental steady-state performance (five-level inverter).

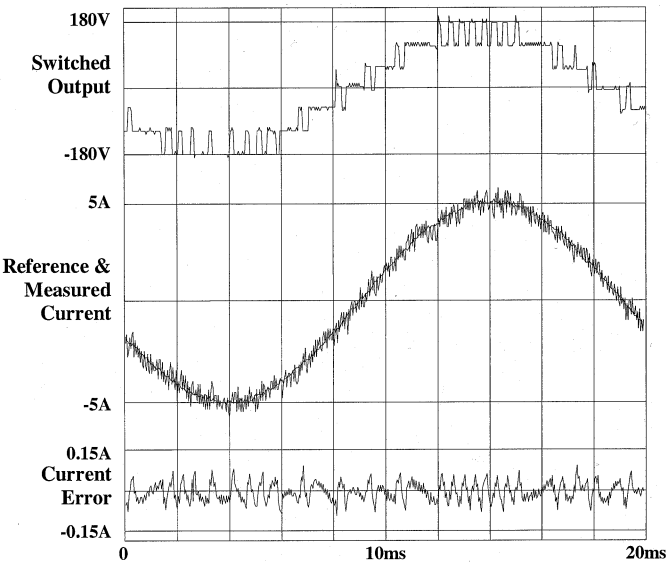

Fig. 14. Experimental steady-state performance (hybrid inverter).

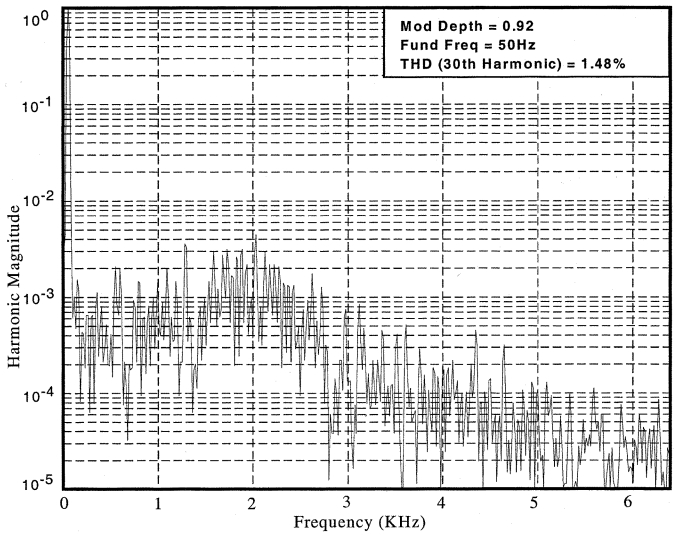

Fig. 15. Experimental load current harmonic spectrum (hybrid inverter).

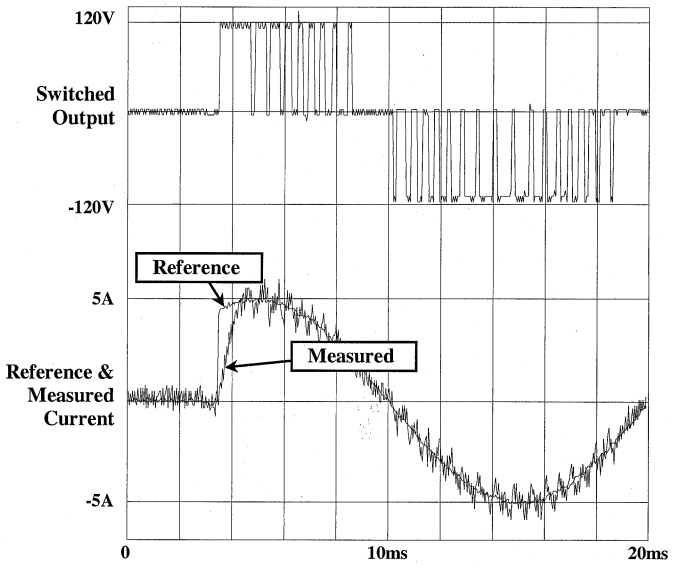

Fig. 16. Experimental transient performance without outer hysteresis band (three-level inverter).

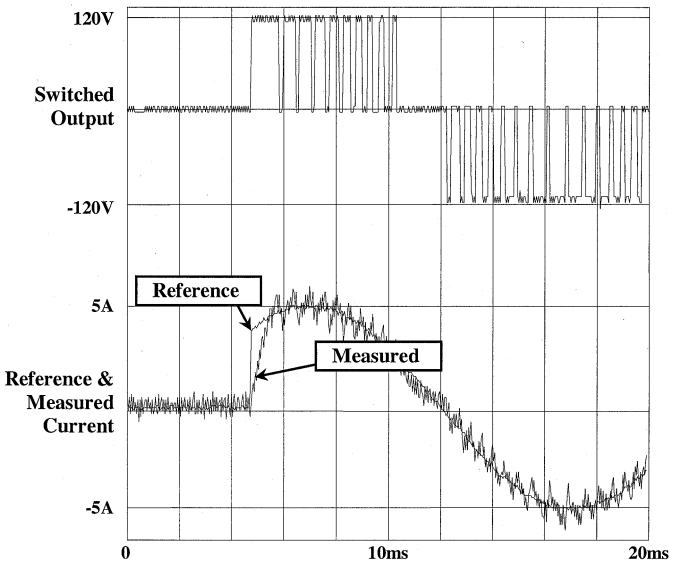

Fig. 17. Experimental transient performance with outer hysteresis band (three-level inverter).

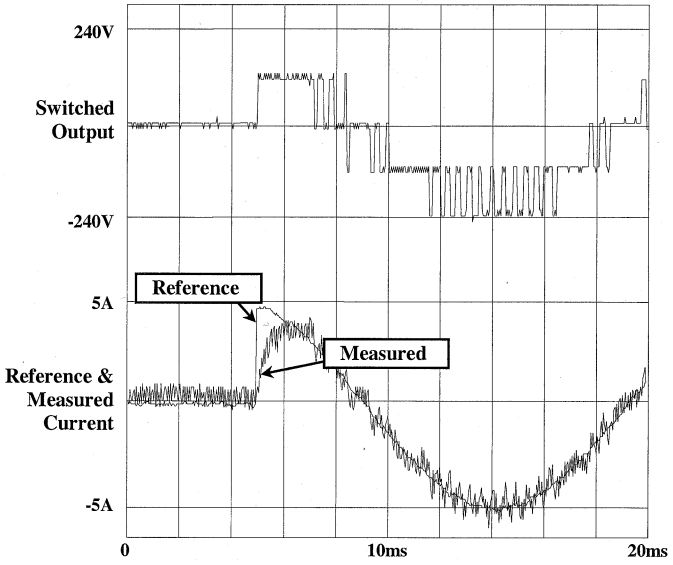

Fig. 18. Experimental transient performance without outer hysteresis band (five-level inverter).

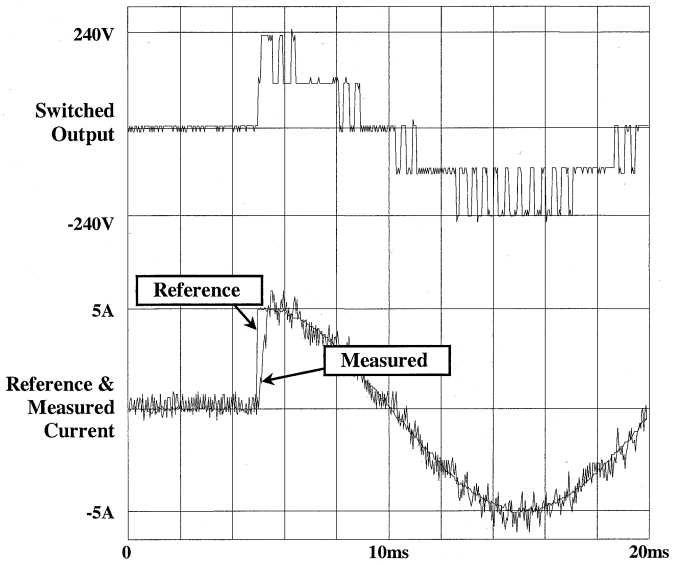

Fig. 19. Experimental transient performance with outer hysteresis band (five-level inverter).

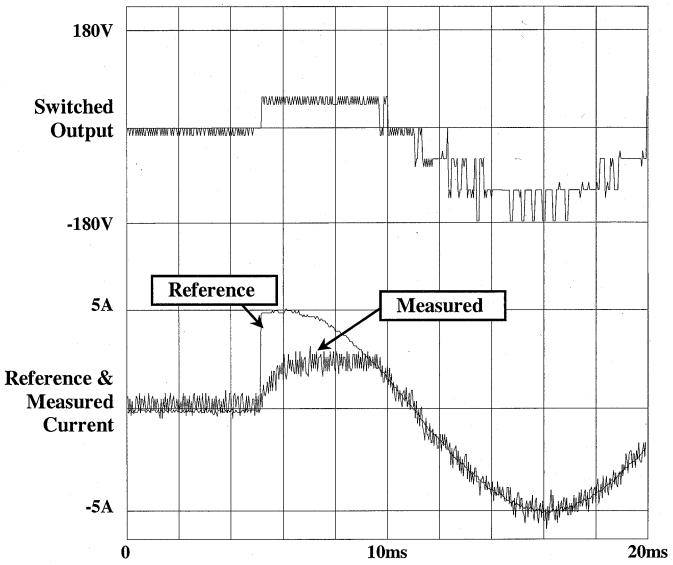

Fig. 20. Experimental transient performance without outer hysteresis band (hybrid inverter).

can, however, be seen in Figs. 18 and 19 which show the transient performance for a five-level inverter, and Figs. 20 and 21 which show the performance of a hybrid inverter. Figs. 19 and 21 show switching to the extreme voltage level, triggered by the outer band control, to rapidly force the current error back within the inner hysteresis band. This improvement in performance is expected to be more significant as the number of voltage levels increases. This is clearly highlighted by the much improved response with outer band control for a hybrid seven-level inverter relative to that of three-level and five-level inverters.

VII. Conclusion

This paper has presented an improved time-based double-band hysteresis current regulation strategy for the control of multilevel inverters. During steady-state operation, the current error is confined within the inner hysteresis band

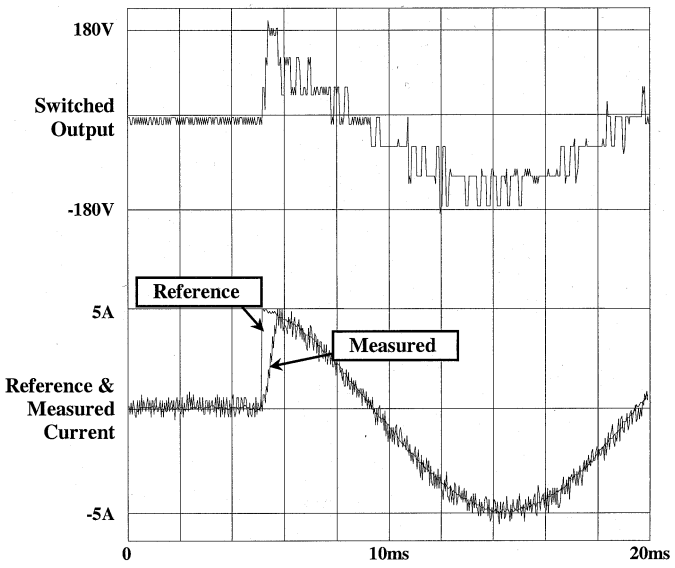

Fig. 21. Experimental transient performance with outer hysteresis band (hybrid inverter).

by a slope detection algorithm that inhibits the level switching process immediately upon reversal of the slope of the current error. This always ensures switching between two adjacent voltage levels of the inverter without oscillation. When a transient event is detected by the outer hysteresis band being exceeded, the slope detection algorithm is deactivated so that the inverter can continuously switch to the extreme voltage states and rapidly reduce the current error as quickly as possible. The proposed regulator exhibits excellent reference tracking, increased robustness, fast dynamic response, and can easily be adapted to control multilevel inverters of any topology. In particular, the additional logic needed to control a hybrid inverter was presented and verified.

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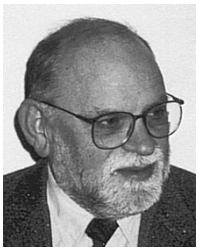
Dr. Holmes regularly reviews papers for all major IEEE TRANSACTIONS in his area. He is an active member of the Industrial Power Converter and Industrial Drives Committees of the IEEE Industry Applications Society.



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