

Research Report

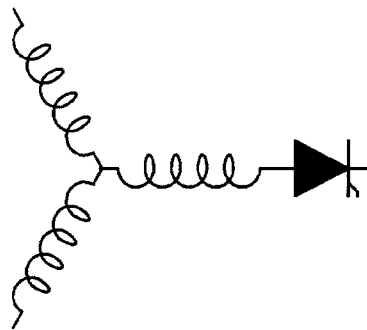
2003-04

**A Reduced Common Mode Hysteresis Current Regulation
Strategy for Multilevel Inverters**

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A Reduced Common Mode Hysteresis Current Regulation Strategy for Multilevel Inverters

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Abstract - This paper presents a new hysteresis current regulation technique with reduced common mode switching for three-phase multilevel inverters. The proposed technique uses three independent multilevel hysteresis current regulators to generate three sets of complementary gating signals through the comparison of the measured current errors with implemented hysteresis limits. These gating signals are then distributed to each complementary switch pair of the multilevel inverter structure to switch with reduced common mode voltage. Additionally, by intelligently compensating for transition delays during dead-times, common mode voltage can essentially be eliminated completely.

Two versions of the common mode regulation technique are derived by using either the line currents or differences between the line currents, known as delta currents, as the control variables. A detailed investigation is presented to determine that the delta currents are the optimal control variables. The performance of the proposed strategy is confirmed through both simulation and experimental investigations.

Index Terms – Multilevel inverters, hysteresis, current regulation, common mode voltages.

I. INTRODUCTION

The many inherent benefits of multilevel inverters have led to their recent increased interest amongst both industry and utilities. At present, the two most commonly used multilevel topologies are the three-level Neutral-Point-Clamped (NPC) and cascaded topologies illustrated in Figure 1 [1, 2]. Various techniques have been developed to control these inverters, with the most popular being open-loop carrier and Space Vector (SVM) modulation strategies [1, 3], and closed-loop hysteresis current regulation [4, 5, 6]. Open-loop carrier and SV based modulation schemes are now well established and can be readily used with a synchronous PI or predictive compensator to create a linear current regulator for a multilevel inverter with a fixed switching frequency.

Alternatively, to achieve an improved dynamic performance, various hysteresis current regulation strategies have been reported and can broadly be classified as using either a multiple band or a digital time-based technique [5, 6]. These strategies can further be developed with band-varying

algorithms for applications that prefer a near constant switching frequency [7, 8, 9].

Although demonstrating good performance, these various control strategies generally give rise to a non-zero common mode voltage. This can be undesirable for applications such as adjustable speed AC drives where common mode voltage has been suggested to cause premature motor bearing failure, and/or leakage currents to ground which can cause electromagnetic interference (EMI) and false tripping of ground current protection relays.

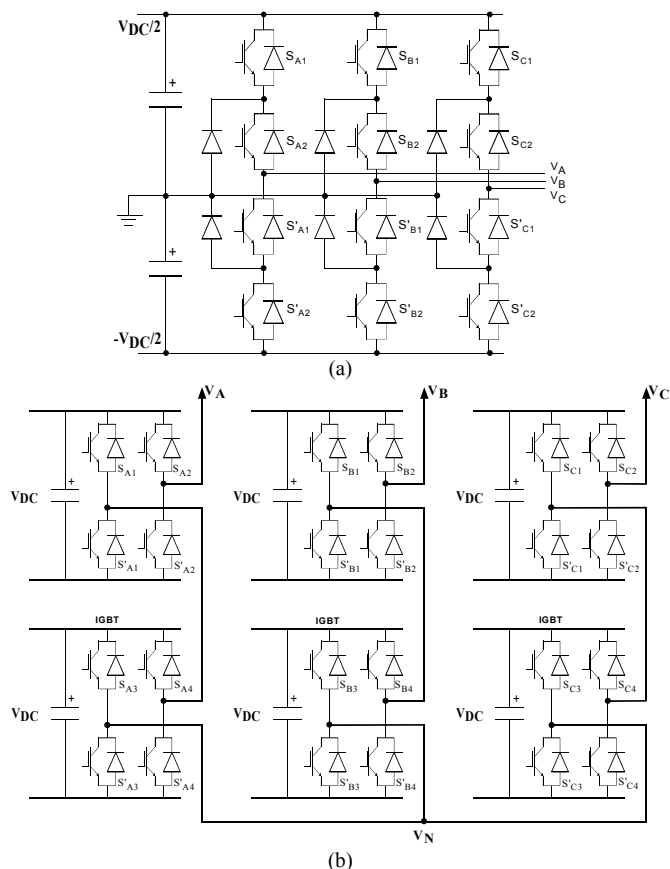


Figure 1: Topological arrangements of (a) three-level neutral-point-clamped and (b) five-level cascaded inverters.

To mitigate these problems, various carrier and SV based PWM strategies have recently been reported for controlling multilevel inverters that have an odd number of DC voltage levels, to reduce the switched common mode voltages [1, 2, 3]. These strategies constrain the inverter to assume only selected switching states that have zero common mode potential and have been shown to be a highly effective and low cost solution for eliminating common mode voltage with no additional hardware. And not unexpectedly, these modulators can readily be used with a front-end compensator to create a linear current regulator with reduced common mode switching.

This paper now presents an alternative reduced common mode approach for hysteresis current regulation that integrates the fast dynamic response of a hysteresis regulator with the concept of reduced common mode switching to create a new high performance current regulator. A further refinement in the form of dead-time compensation is then presented that reduces common mode voltage spikes caused by commutation. Finally, from simulation studies, it is shown that the delta current errors (i.e. the differences between the line current errors) are the optimum control variables for this system. (This conclusion is in fact equally relevant to all types of current regulators.) The principles presented have

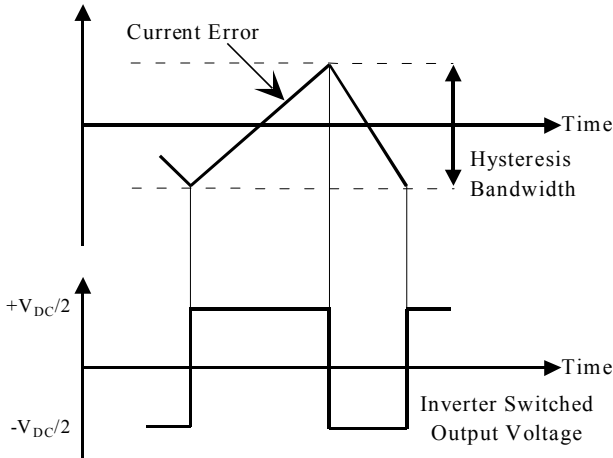


Figure 2: Conventional two-level hysteresis current regulation.

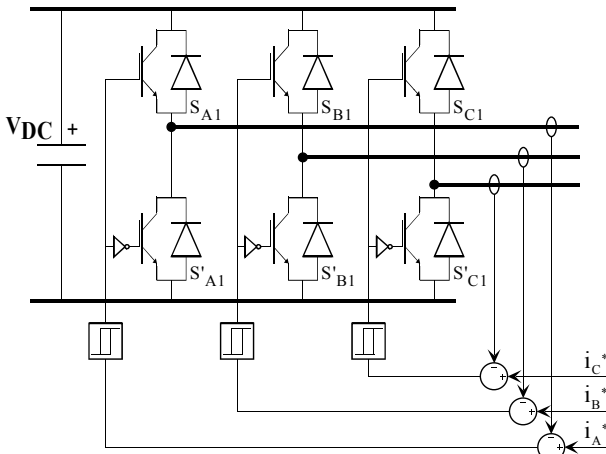


Figure 3: Three-phase two-level hysteresis current regulation.

been verified by both detailed MATLAB simulation and experimental investigations.

II. CONVENTIONAL TWO-LEVEL HYSTERESIS CURRENT REGULATION

Conventional two-level hysteresis current control operates by comparing a current error (i.e. the difference between measured and demanded phase currents) against a fixed hysteresis band. When the error falls below the lower hysteresis limit, the inverter phase-leg output is switched high, and when the error rises above the upper hysteresis limit, the inverter output switches low. This process is illustrated in Figure 2.

Two-level hysteresis current regulation with only two DC voltage levels is relatively straightforward, with each hysteresis boundary being mapped essentially to one inverter phase-leg switched state. A three-phase system can also be simply implemented using three independent single-phase hysteresis current regulators as illustrated in Figure 3.

III. MULTILEVEL HYSTERESIS CURRENT REGULATION – DC VOLTAGE SELECTION

Unlike conventional two-level inverters, multilevel inverters use numerous DC levels for the synthesis of their output voltage waveforms. Hysteresis current control of multilevel inverters therefore requires additional logic to select the appropriate voltage level at any time instant so as

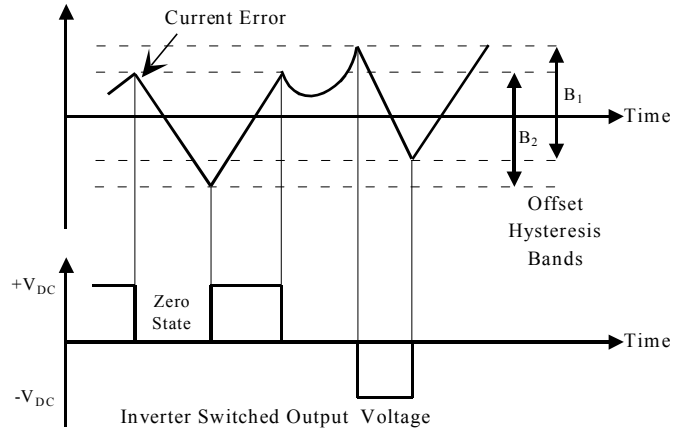


Figure 4: Three level multi-band hysteresis current regulation.

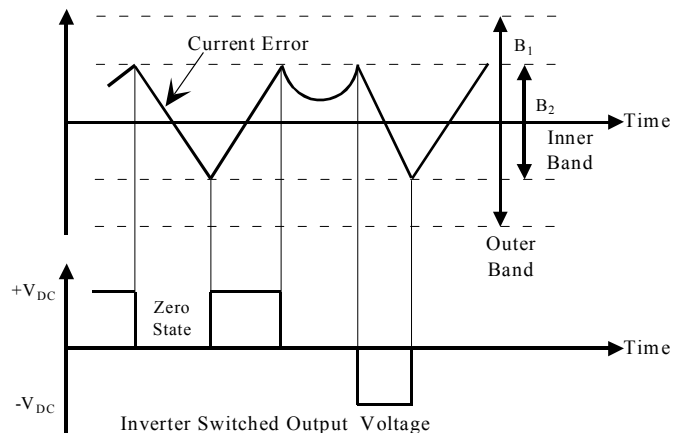


Figure 5: Time-based hysteresis current regulation.

to confine the current error within the hysteresis band.

One approach is to use multiple hysteresis bands to control the switching between two adjacent DC voltage levels [4, 5, 6]. In total, $(N-1)$ bands are required for the control of a N -level inverter. The placement of these bands is illustrated in Figure 4 for a three-level inverter, where the upper band represents switching between the two adjacent DC levels of $-V_{DC}$ (upper boundary hit) and 0 (lower boundary hit) while the lower band represents switching between 0 (upper boundary hit) and $+V_{DC}$ (lower boundary hit). The disadvantage of this approach is that the number of bands increases as the number of inverter voltage levels increases.

An alternative approach is to have only one single (inner) hysteresis band to detect the switching instants, with digital logic used to select the appropriate voltage levels to switch to at those instants [5, 6]. This approach is illustrated in Figure 5. Whenever a hysteresis boundary is exceeded, the inverter terminal voltage switches down (upper boundary hit) or up (lower boundary hit) until a voltage level is selected that will reverse the current error back to within the hysteresis band. This current error reversal can easily be detected by measuring its derivative.

An additional outer band can also be incorporated as shown in Figure 5. Upon exceeding this outer band during transient events, the derivative detection algorithm is

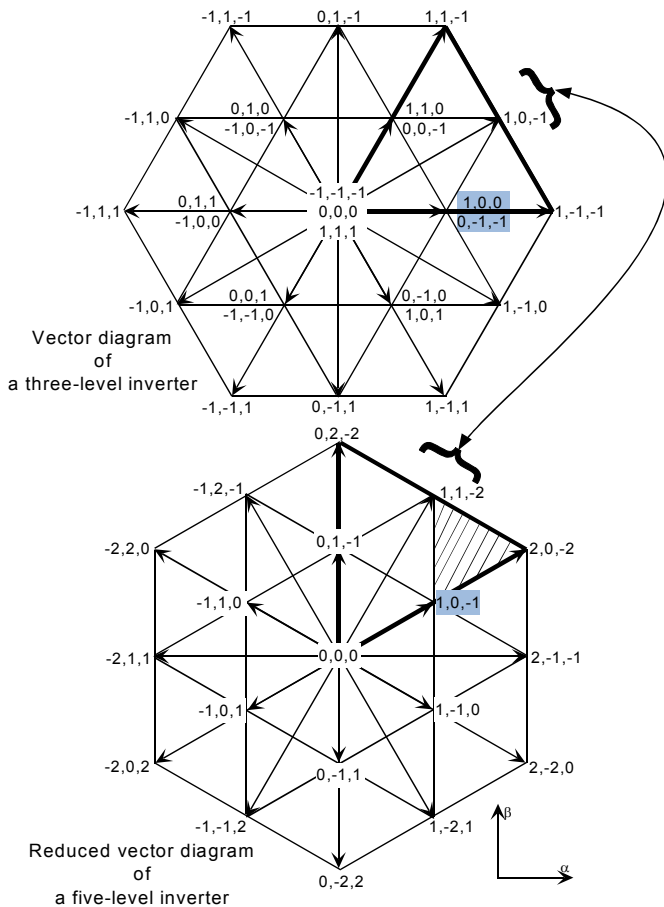


Figure 6: Linkage between vector diagrams of three-level and reduced common mode five-level inverters.

inhibited, and the inverter switches directly to the extreme voltage levels. This forces the current error back to zero at the fastest possible rate [6]. This strategy can equally be extended to a three-phase system as illustrated in Figure 3 with each two-level phase-leg replaced by a multilevel phase-leg. However, the resulting current regulated system generates a non-zero common mode voltage. In the next section, a method of implementing three-phase current regulated systems that achieves reduced common mode switching is presented.

IV. REDUCED COMMON MODE HYSTERESIS CURRENT REGULATION

As presented in [1], the space vector diagram of a N -level inverter under reduced common mode switching is equivalent to that of a $((N+1)/2)$ -level inverter with a 30° phase displacement and no associated redundant states. Figure 6 illustrates this with an example of a reduced five-level vector diagram and its conventional three-level matched counterpart, with the switching state indexes normalised to the DC voltage step of V_{DC} . Reduced common mode switching therefore is achieved by using three independent $((N+1)/2)$ -level regulators as illustrated in Figure 7 (one for each phase) and then matching the generated inverter switched states to the reduced states of a N -level inverter that

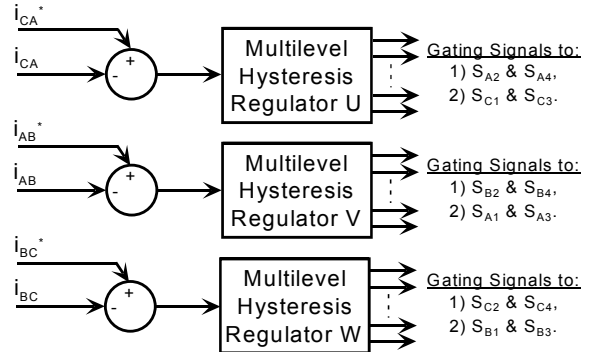


Figure 7: General layout of proposed hysteresis current regulation.

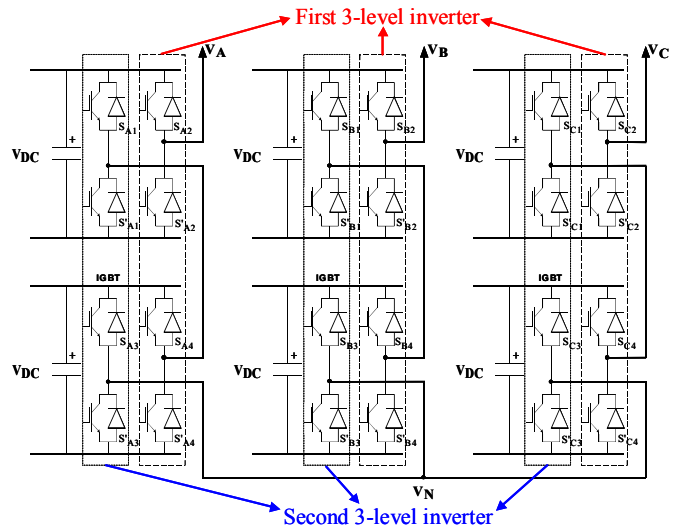


Figure 8: Division of a five-level inverter to two three-level inverters.

ensure zero common mode voltage. Note that the 30° shift in the switched phasors generated by this SV matching process is compensated by the hysteresis process, and does not cause any problems. Also, for the multiple band hysteresis scheme, the approach reduces the number of hysteresis bands to $((N-1)/2)$, similar to the reduction of carriers achieved by the reduced common mode carrier-based PWM proposed in [1].

For a N -level NPC inverter, the generated switching states have to be explicitly matched by logic to the correct gating signals to control the inverter. However, for a N -level cascaded inverter, the appropriate gating signals can be more simply derived using redundant switching states within a cascaded phase-leg. Comparing the space vector diagrams in Figure 6, it is observed that the switching state for any node on the reduced five-level diagram can be derived by taking the differences between the adjacent phase states of their matched counterparts on the conventional three-level diagram. For example, state $\{1, 0, -1\}$ on the reduced five-level diagram is obtained by subtracting the adjacent phase states of $\{1, 0, 0\}$ or $\{0, -1, -1\}$. Such subtractions between phase states can easily be implemented with the cascaded topology by dividing a cascaded inverter into two sub-inverters. For a cascaded five-level inverter, this means dividing it into two three-level sub-inverters as shown in Figure 8, with the first sub-inverter comprising inner phase-legs S_{x2} and S_{x4} and the second sub-inverter comprising S_{x1} and S_{x3} ($x = A, B$ or C). By controlling the first sub-inverter with the sequence of $\{\text{Regulator U, V, W}\} \rightarrow \{\text{Phase A, B, C}\}$ and the second sub-inverter with a rotated sequence of $\{\text{Regulator V, W, U}\} \rightarrow \{\text{Phase A, B, C}\}$, the overall terminal output of the inverter is always constrained to those switching states with zero common mode potential. The gating signal allocation for this method of control is shown in Figure 7.

V. DEAD-TIME COMPENSATION TECHNIQUE

Complete elimination of common mode voltage is only achieved if the terminal outputs of both phase-legs controlled by a regulator, change voltage levels simultaneously. This however cannot be guaranteed during dead-time intervals when the output level of a phase-leg is determined by the direction of current through it. Common mode spikes equal to the dead-time intervals can therefore exist during this period, with a magnitude of one-third the DC voltage step size. However, these common mode spikes can be eliminated with this proposed hysteresis regulation technique by intelligently compensating for output transition delays during dead-times, as shown in Figure 9.

As shown in this figure, the switching ON of S_{A1} and S_{B2} , controlled by regulator V, passes through an additional intermediate state of $\{S_{A1} = 0 \text{ and } S_{B2} = 1\}$ during the dead-time interval if the currents drawn from both switches are of opposite polarities. A narrow common mode voltage spike would therefore occur during this interval. However, this spike can be avoided by sensing the directions of currents drawn from both switch pairs and delaying the gating of the

switches whose output changes instantaneously upon gate transition, as shown in Figure 9. Note that this technique compensates for dead-time delays to eliminate commutation spikes through the coordination of gating signals to **two** multilevel phase-legs based on currents flowing through **both** phase-legs. This is unlike previously reported dead-time compensation strategies [7, 8], usually associated with a variable hysteresis band algorithm, where gating signals to only a **single** phase-leg are adjusted to compensate for volt-second error caused by dead-time delays.

VI. CONTROL VARIABLE SELECTION

The control variables of either the three-phase line currents or delta currents (defined as the differences between any two of the three line currents [8, 9]) are commonly used with two-level current regulators. Both sets of control variables are equally applicable to the proposed reduced common mode hysteresis regulation strategy. However, the use of delta currents achieves significantly lower low-order harmonic distortion. The reasons for this can be explained by considering the general representation of a power electronic system as shown in Figure 10.

The state equations for the system can be written as (considering only **fundamental** components):

$$v_A = v_U - v_V = e_A + L \frac{di_A}{dt}; \quad (1)$$

$$v_B = v_V - v_W = e_B + L \frac{di_B}{dt}; \quad (2)$$

$$v_C = v_W - v_U = e_C + L \frac{di_C}{dt} \quad (3)$$

where v_U , v_V and v_W are outputs implicitly generated by regulators U, V and W respectively. Rearranging (1), (2) and (3) gives:

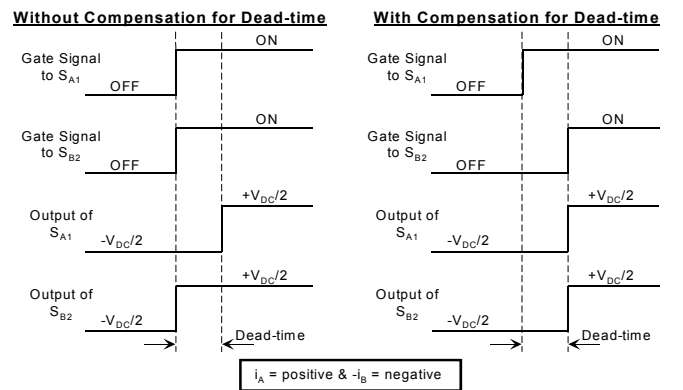


Figure 9: Compensation for dead-time delay.

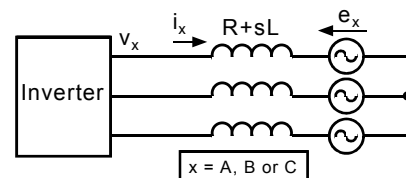


Figure 10: General representation of power electronic system.

$$v_A - v_B = v_U + v_W - 2v_V = e_A - e_B + L \left\{ \frac{di_A}{dt} - \frac{di_B}{dt} \right\} \quad (4)$$

$$v_B - v_C = v_U + v_V - 2v_W = e_B - e_C + L \left\{ \frac{di_B}{dt} - \frac{di_C}{dt} \right\} \quad (5)$$

$$v_C - v_A = v_V + v_W - 2v_U = e_C - e_A + L \left\{ \frac{di_C}{dt} - \frac{di_A}{dt} \right\} \quad (6)$$

Since $v_U + v_V + v_W = 0$, (4), (5) and (6) can be expressed in term of the line currents as:

$$[v_V, v_W, v_U]^T = \frac{1}{3} \left\{ M \cdot [i_A, i_B, i_C]^T - [e_{AB}, e_{BC}, e_{CA}]^T \right\} \quad (7)$$

$$\text{where } M = \begin{bmatrix} -Lp & Lp & 0 \\ 0 & -Lp & Lp \\ Lp & 0 & -Lp \end{bmatrix} \text{ and } p = d/dt.$$

From (7), if the line currents are used as control variables, each regulator fundamental output is dependent on two control variables (because of the non-zero off-diagonal elements in M). Hence there will be cross-coupling interactions between any two current regulators.

On the other hand, if the delta currents are used as the control variables, (4), (5) and (6) become:

$$[v_V, v_W, v_U]^T = \frac{1}{3} \left\{ M' \cdot [i_{AB}, i_{BC}, i_{CA}]^T - [e_{AB}, e_{BC}, e_{CA}]^T \right\} \quad (8)$$

$$\text{where } M' = \begin{bmatrix} -Lp & 0 & 0 \\ 0 & -Lp & 0 \\ 0 & 0 & -Lp \end{bmatrix}.$$

The presence of diagonal terms only in M' clearly implies the removal of fundamental cross-coupling effects, and the output of each regulator is now solely determined by a single delta current variable. Note that this analysis is equally applicable for a linear current regulator and is similar to the removal of phase coupling effects within a synchronous PI compensator used for uninterruptible power supplies [10, 11].

VII. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the current regulation strategy presented above has been verified in simulation for a three-level and a five-level inverter, and experimentally for a three-level inverter. The simulation investigations were performed with MATLAB Simulink and with practical effects such as sampled three-phase references (generated experimentally using a DSP for convenience) and dead-time delays taken into consideration so as to match the experimental system closely. Note also that for the results presented, the term HLCR (Hysteresis Line Current Regulator) refers to the proposed current regulator using the line currents as the control variables while HDCR (Hysteresis Delta Current Regulator) refers to the regulator using the delta currents as the control variables.

Figure 11 shows the experimental switched waveforms of a three-level inverter controlled with the HDCR current regulator without dead-time compensation while Figure 12

shows an enlarged view of the common mode voltage. As anticipated, in addition to achieving excellent reference tracking performance, the regulator reduces the common mode voltage to only transitional spikes of $2\mu\text{s}$ duration (i.e. the dead-time interval) and has a magnitude of $V_{DC}/3 \approx 45\text{V}$. Figure 13 shows the experimental switched waveforms with the proposed dead-time compensation technique incorporated to the HDCR regulator. Note the further reduction of common mode spikes as compared to Figure 11. Figure 14 shows the experimental harmonic spectrum of the common mode voltage under these conditions, with no significant harmonics at all. Figure 15 shows the experimental transient performance of the HDCR current regulator under a no-load to full-load step change, which confirms the excellent dynamic performance of the proposed regulator. Figure 16 shows the simulated switched waveforms for the case of a five-level inverter, which clearly shows the easy application of the technique to higher level inverters with the same level of effectiveness in eliminating common mode voltage.

To verify the performance improvement that can be achieved through the use of the delta currents as the control variables, Figure 17 and Figure 18 show the simulated output current harmonic spectra when using the HLCR and HDCR current regulators respectively to control a three-level inverter. Figure 19 and Figure 20 show the obtained spectra with the regulators controlling a five-level inverter. Note the significantly improved harmonic performance (both low order and switching performances) of the HDCR regulator with much lower output current THD values.

VIII. CONCLUSION

This paper presents a new reduced common mode hysteresis current regulation technique for the control of multilevel inverters. The proposed technique is based on restricting the inverter phase-leg switching states to achieve reduced common mode voltages. By further compensating for dead-time delays across two phase-legs, common mode transitional spikes can also be eliminated. In addition, by selecting the delta current errors as the control variables, cross-couplings between independent control loops are removed and an improved low order harmonic performance is achieved.

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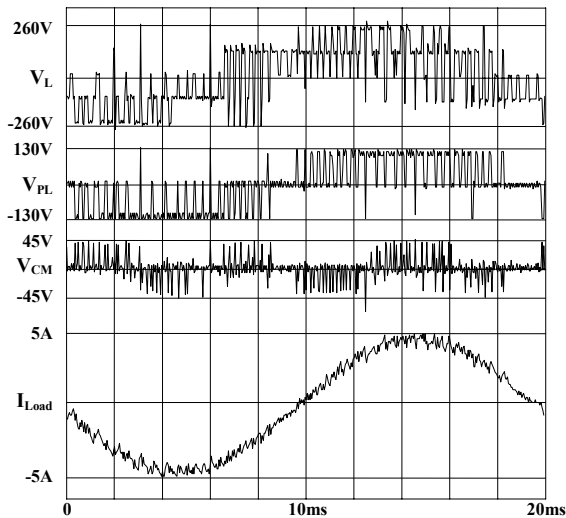


Figure 11: Experimental switched waveforms using HDCR regulation of a three-level inverter without dead-time compensation: V_L , V_{PL} , V_{CM} = line, phase-leg and common mode voltages; I_{LOAD} = current.

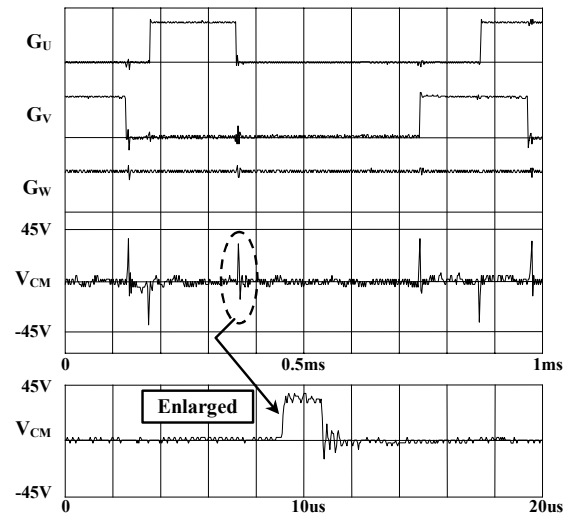


Figure 12: Zoomed IN view of common mode spikes: G_U , G_V , G_W = current regulator outputs; V_{CM} = common mode voltage.

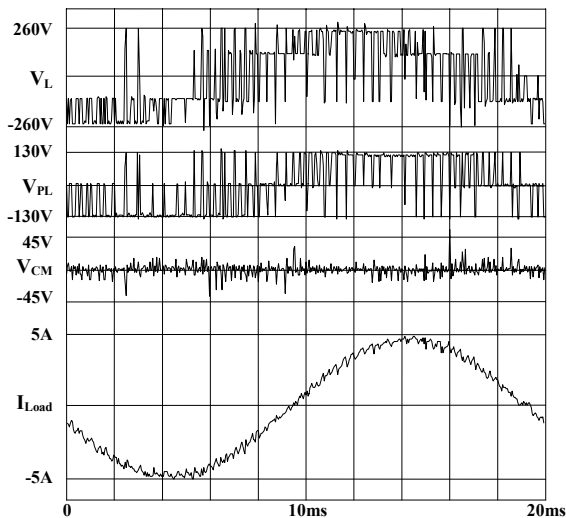


Figure 13: Experimental switched waveforms using HDCR regulation of a three-level inverter with dead-time compensation: V_L , V_{PL} , V_{CM} = line, phase-leg and common mode voltages; I_{LOAD} = current.

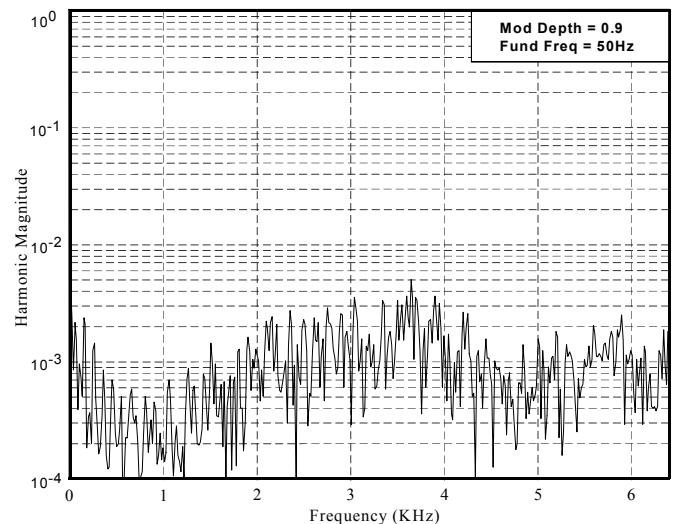


Figure 14: Experimental spectrum of common mode voltage using HDCR regulation of a three-level inverter with dead-time compensation.

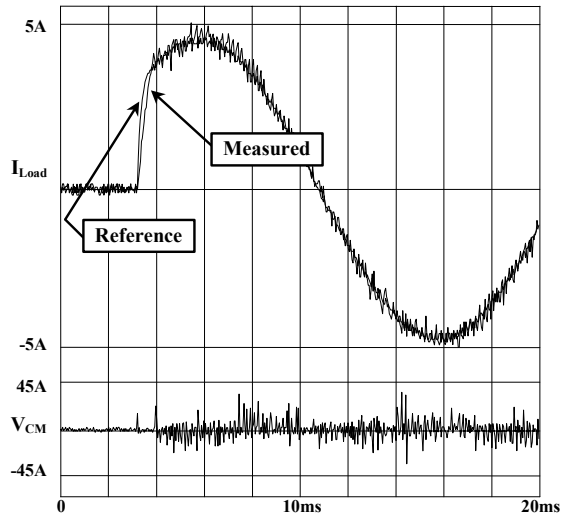


Figure 15: Experimental transient performance using HDCR regulation of a three-level inverter: I_{LOAD} = current; V_{CM} = common mode voltage.

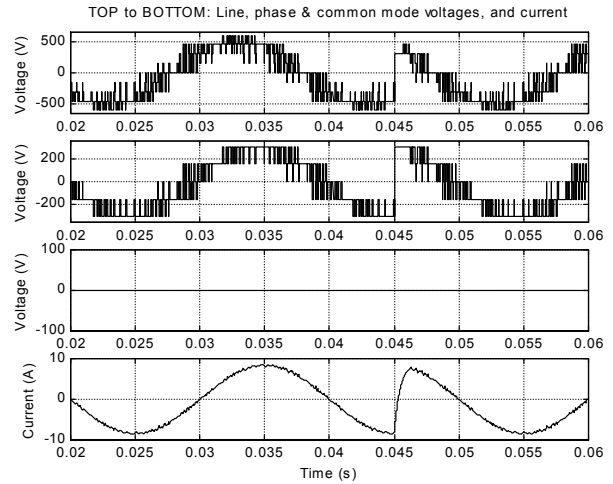


Figure 16: Simulated switched waveforms using HDCR regulation of a five-level inverter with dead-time compensation.

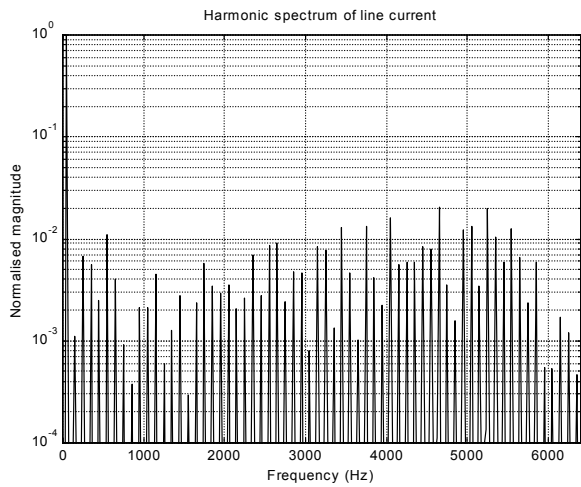


Figure 17: Simulated current spectrum using HLCR regulation of a three-level inverter: THD (120th harmonic) = 5.6402.

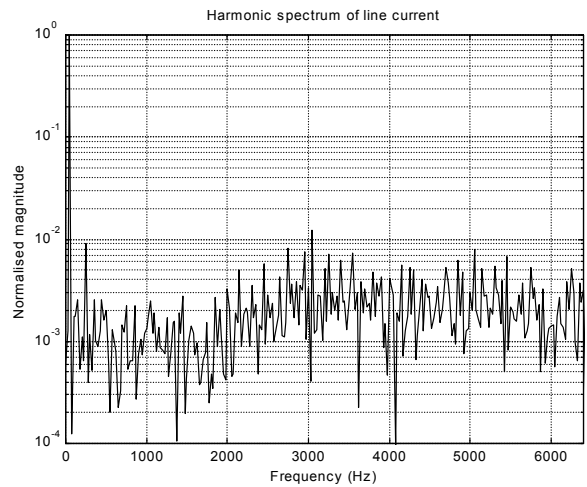


Figure 18: Simulated current spectrum using HDCR regulation of a three-level inverter: THD (120th harmonic) = 3.8937.

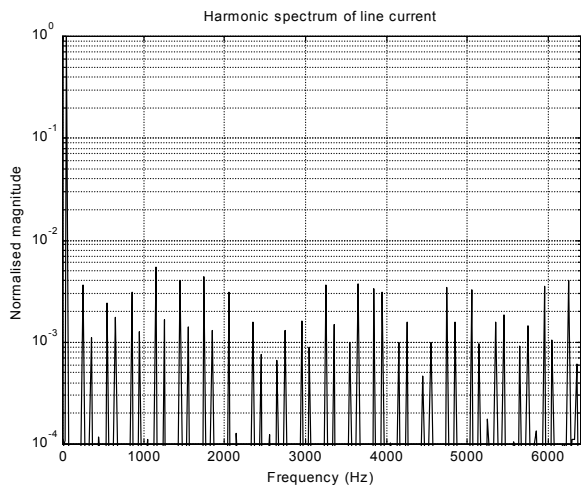


Figure 19: Simulated current spectrum using HLCR regulation of a five-level inverter: THD (120th harmonic) = 1.5054.

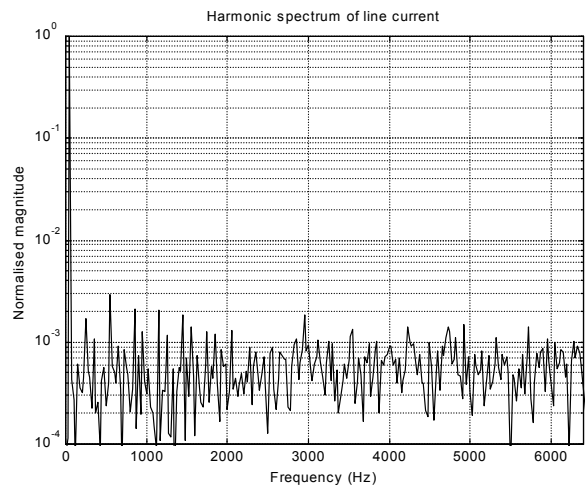


Figure 20: Simulated current spectrum using HDCR regulation of a five-level inverter: THD (120th harmonic) = 0.8845.