A Reduced Common Mode Hysteresis Current Regulation Strategy for Multilevel Inverters

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***Abstract*—This paper presents a new hysteresis current regulation technique with reduced common mode switching for three-phase multilevel inverters. The proposed technique uses three independent multilevel hysteresis current regulators to generate three sets of complementary gating signals through the comparison of the measured current errors with implemented hysteresis limits. These gating signals are then distributed to each complementary switch pair of the multilevel inverter structure to switch with reduced common mode voltage. Additionally, by intelligently compensating for transition delays during dead-times, common mode voltage can essentially be eliminated completely.**

Two versions of the common mode regulation technique are derived by using either the line currents or differences between the line currents, known as delta currents, as the control variables. A detailed investigation is presented to determine that the delta currents are the optimal control variables. The performance of the proposed strategy is confirmed through both simulation and experimental investigations.

***Index Terms*—Common mode voltages, current regulation, hysteresis, multilevel inverters.**

I. Introduction

THE MANY inherent benefits of multilevel inverters have led to their recent increased interest amongst both industry and utilities. At present, the two most commonly used multilevel topologies are the three-level neutral-point-clamped (NPC) and cascaded topologies illustrated in Fig. 1, [1], [2]. Various techniques have been developed to control these inverters, with the most popular being open-loop carrier and space vector (SVM) modulation strategies [1], [3], and closed-loop hysteresis current regulation [4]–[6]. Open-loop carrier and SV based modulation schemes are now well established and can be readily used with a synchronous PI or predictive compensator to create a linear current regulator for a multilevel inverter with a fixed switching frequency.

Alternatively, to achieve an improved dynamic performance, various hysteresis current regulation strategies have been reported and can broadly be classified as using either a multiple band or a digital time-based technique [5], [6]. These strategies can further be developed with band-varying algorithms for applications that prefer a near constant switching frequency [7]–[9].

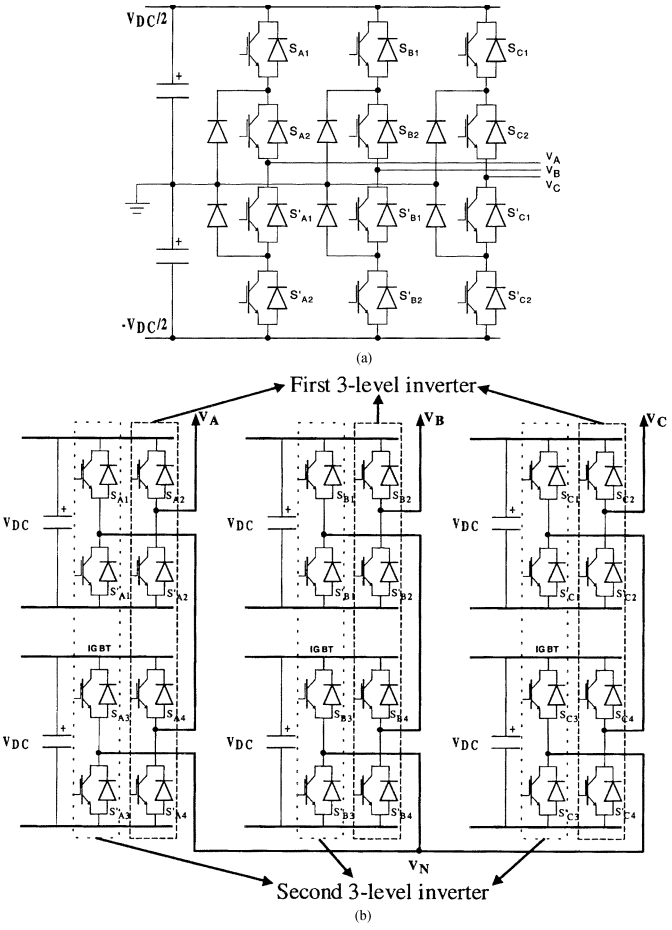

Fig. 1. Topological arrangements of: (a) three-level neutral-point-clamped and (b) five-level cascaded inverters.

Although demonstrating good performance, these various control strategies generally give rise to a nonzero common mode voltage. This can be undesirable for applications such as adjustable speed ac drives where common mode voltage has been suggested to cause premature motor bearing failure, and/or leakage currents to ground which can cause electromagnetic interference (EMI) and false tripping of ground current protection relays.

To mitigate these problems, various carrier and SV based PWM strategies have recently been reported for controlling

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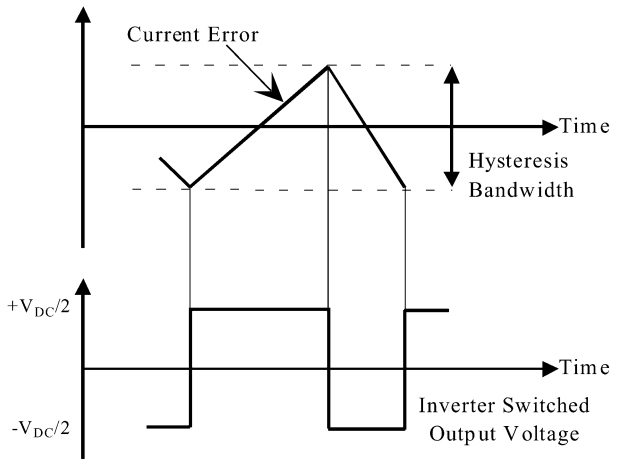

Fig. 2. Conventional two-level hysteresis current regulation.

multilevel inverters that have an odd number of dc voltage levels, to reduce the switched common mode voltages [1]–[3]. These strategies constrain the inverter to assume only selected switching states that have zero common mode potential and have been shown to be a highly effective and low cost solution for eliminating common mode voltage with no additional hardware. And not unexpectedly, these modulators can readily be used with a front-end compensator to create a linear current regulator with reduced common mode switching.

This paper now presents an alternative reduced common mode approach for hysteresis current regulation that integrates the fast dynamic response of a hysteresis regulator with the concept of reduced common mode switching to create a new high performance current regulator. A further refinement in the form of dead-time compensation is then presented that reduces common mode voltage spikes caused by commutation. Finally, from simulation studies, it is shown that the delta current errors (i.e., the differences between the line current errors) are the optimum control variables for this system. The principles presented have been verified by both detailed MATLAB simulation and experimental investigations.

II. Multilevel Hysteresis Current Regulation-DC Voltage Selection

Conventional two-level hysteresis current control operates by comparing a current error (i.e., the difference between measured and demanded phase currents) against a fixed hysteresis band. When the error falls below the lower hysteresis limit, the inverter phase-leg output is switched high, and when the error rises above the upper hysteresis limit, the inverter output switches low. This process is illustrated in Fig. 2. Two-level hysteresis current regulation with only two dc voltage levels is therefore relatively straightforward, with each hysteresis boundary being mapped essentially to one inverter phase-leg switched state. A three-phase system can also be simply implemented using three independent single-phase hysteresis current regulators.

Unlike conventional two-level inverters, multilevel inverters use numerous dc levels for the synthesis of their output voltage waveforms. Hysteresis current control of multilevel inverters

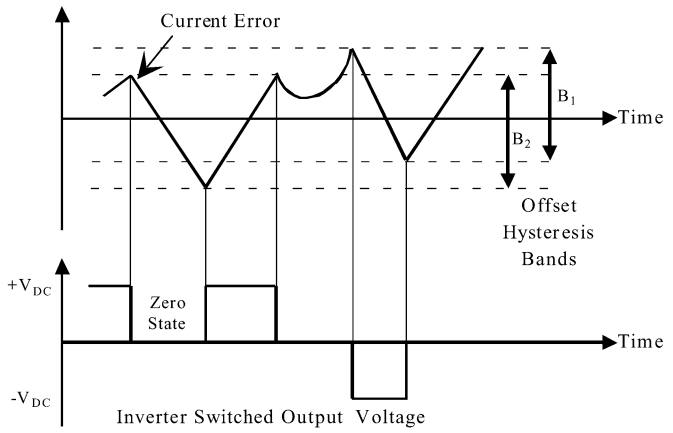

Fig. 3. Three level multiband hysteresis current regulation.

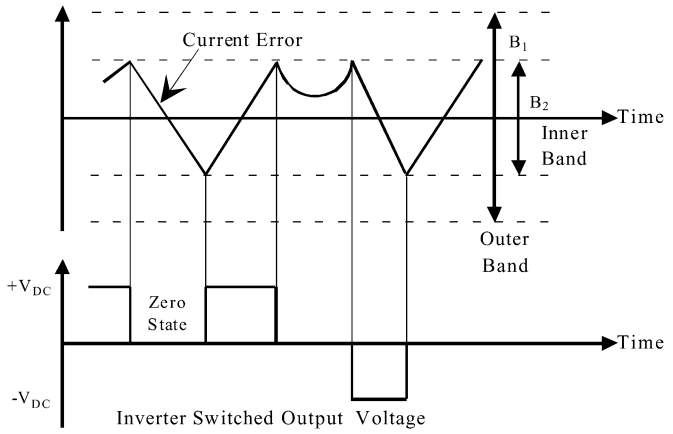

Fig. 4. Time-based hysteresis current regulation.

therefore requires additional logic to select the appropriate voltage level at any time instant so as to confine the current error within the hysteresis band.

One approach is to use multiple hysteresis bands to control the switching between two adjacent dc voltage levels [4]–[6]. In total, $(N-1)$ bands are required for the control of a N-level inverter. The placement of these bands is illustrated in Fig. 3 for a three-level inverter, where the upper band represents switching between the two adjacent dc levels of $-V_{\rm DC}$ (upper boundary hit) and 0 (lower boundary hit) while the lower band represents switching between 0 (upper boundary hit) and $+V_{\rm DC}$ (lower boundary hit). The disadvantage of this approach is that the number of bands increases as the number of inverter voltage levels increases.

An alternative approach is to have only one single (inner) hysteresis band to detect the switching instants, with digital logic used to select the appropriate voltage levels to switch to at those instants [5], [6]. This approach is illustrated in Fig. 4. Whenever a hysteresis boundary is exceeded, the inverter terminal voltage switches down (upper boundary hit) or up (lower boundary hit) until a voltage level is selected that will reverse the current error back to within the hysteresis band. This current error reversal can easily be detected by measuring its derivative.

An additional outer band can also be incorporated as shown in Fig. 4. Upon exceeding this outer band during transient events, the derivative detection algorithm is inhibited, and the

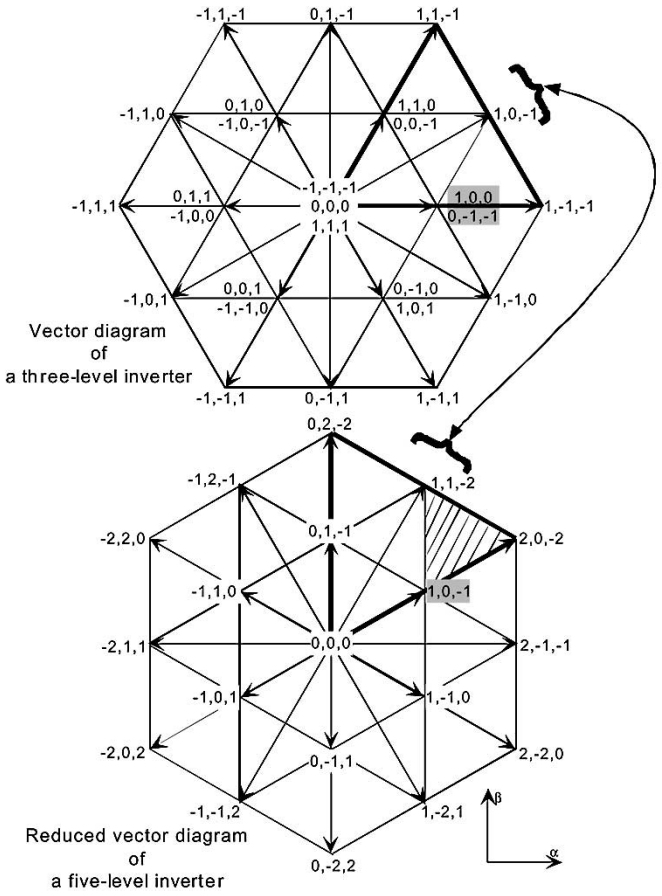

Fig. 5. Linkage between vector diagrams of three-level and reduced common mode five-level inverters.

inverter switches directly to the extreme voltage levels. This forces the current error back to zero at the fastest possible rate [6]. This strategy can equally be extended to a three-phase system using three independent multilevel hysteresis current regulators. However, the resulting current regulated system generates a nonzero common mode voltage. In the remaining sections, the theoretical development and implementation of a new three-phase dead-time compensated current regulation technique that achieves reduced common mode switching is presented.

III. Reduced Common Mode Hysteresis Current Regulation

As presented in [1], the space vector diagram of a N-level inverter under reduced common mode switching is equivalent to that of a $((N+1)/2)$-level inverter with a 30° phase displacement and no associated redundant states. Fig. 5 illustrates this with an example of a reduced five-level vector diagram and its conventional three-level matched counterpart, with the switching state indexes normalized to the dc voltage step of V_{DC}. Reduced common mode switching therefore is achieved by using three independent $((N+1)/2)$-level regulators as illustrated in Fig. 6 (one for each phase) and then matching the generated inverter switched states to the reduced states of a N-level inverter that ensure zero common mode voltage. Note

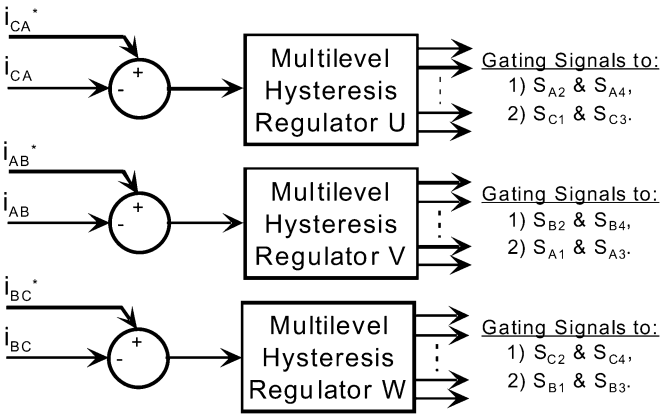

Fig. 6. General layout of proposed hysteresis current regulation.

that the 30 ^{0} shift in the switched phasors generated by this SV matching process is compensated by the hysteresis process, and does not cause any problems. Also, for the multiple band hysteresis scheme, the approach reduces the number of hysteresis bands to $((N-1)/2)$, similar to the reduction of carriers achieved by the reduced common mode carrier-based PWM proposed in [1].

For a N-level NPC inverter, the generated switching states have to be explicitly matched by logic to the correct gating signals to control the inverter. However, for a N-level cascaded inverter, the appropriate gating signals can be more simply derived using redundant switching states within a cascaded phase-leg. Comparing the space vector diagrams in Fig. 5, it is observed that the switching state $\{a,b,c\}$ for any node on the reduced five-level diagram can be derived by taking the differences between their matched counterparts $\{u,v,w\}$ on the conventional three-level diagram and logically left-shifted states $\{v,w,u\}$ derived from these three-level states. Mathematically, these differences can be expressed as: $\{a,b,c\}=\{u,v,w\}-\{v,w,u\}$.

As an example, state $\{1,0,-1\}$ on the reduced five-level diagram (shown shaded in Fig. 5) can be obtained by taking the difference between the three-level state $\{1,0,0\}$ and its left-shifted state $\{0,0,1\}$, or between state $\{0,-1,-1\}$ and its left-shifted state $\{-1,-1,0\}$ (i.e., $\{a,b,c\}=\{1,0,0\}-\{0,0,1\}$ or $\{0,-1,-1\}-\{-1,-1,0\}$). Such subtractions can easily be implemented with the cascaded topology by dividing a cascaded inverter into two subinverters. For a cascaded five-level inverter, this means dividing it into two three-level subinverters as shown in Fig. 1(b), with the first subinverter comprising inner phase-legs S_{x2} and S_{x4} and the second subinverter comprising S_{x1} and S_{x3} (x = A, B, or C). By controlling the first subinverter with the sequence of $\{\mathrm{Regulator\ U,V,W}\}\ \rightarrow\ \{\mathrm{Phase\ A,B,C}\}$ and the second subinverter with a rotated sequence of $\{\mathrm{Regulator\ V,W,U}\}\ \rightarrow\ \{\mathrm{Phase\ A,B,C}\}$, the output of the first subinverter will be $\{u,v,w\}$ while the output of the second subinverter will be $\{v,w,u\}$, starting at the same time instant and lasting for the same time duration. The overall terminal output of the inverter, which is the difference between these two subinverters, will then be always constrained to those switching states with zero common mode potential. The gating signal allocation for this method of control is shown in Fig. 6.

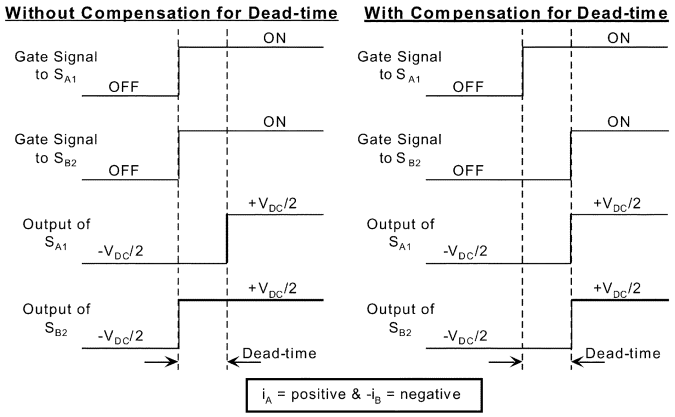

Fig. 7. Compensation for dead-time delay.

IV. Dead-Time Compensation Technique

Complete elimination of common mode voltage is only achieved if the terminal outputs of both phase-legs controlled by a regulator, change voltage levels simultaneously. This however cannot be guaranteed during dead-time intervals when the output level of a phase-leg is determined by the direction of current through it. Common mode spikes equal to the dead-time intervals can therefore exist during this period, with a magnitude of one-third the dc voltage step size. However, these common mode spikes can be eliminated with this proposed hysteresis regulation technique by intelligently compensating for output transition delays during dead-times, as shown in Fig. 7.

As shown in this figure, the switching ON of S_{A1} and S_{B2}, controlled by regulator V, passes through an additional intermediate state of $\{S_{A1} = 0 \text{ and } S_{B2} = 1\}$ during the dead-time interval if the instantaneous currents drawn from both switches are of opposite polarities. A narrow common mode voltage spike would therefore occur during this interval. However, this spike can be avoided by sensing the directions of the instantaneous currents drawn from both switch pairs and delaying the gating of the switches whose output changes instantaneously upon gate transition, as shown in Fig. 7. Note that this technique compensates for dead-time delays to eliminate commutation spikes through the coordination of gating signals to **two** multilevel phase-legs based on currents flowing through **both** phase-legs. This is unlike previously reported dead-time compensation strategies [7], [8], usually associated with a variable hysteresis band algorithm, where gating signals to only a **single** phase-leg are adjusted to compensate for volt-second error caused by dead-time delays.

V. Control Variable Selection

The control variables of either the three-phase line currents or delta currents (defined as the differences between any two of the three line currents [8], [9]) are commonly used with two-level current regulators. Both sets of control variables are equally applicable to the proposed reduced common mode hysteresis regulation strategy. However, the use of delta currents achieves significantly lower low-order harmonic distortion. The reasons for this can be explained by considering the general representation of a power electronic system as shown in Fig. 8.

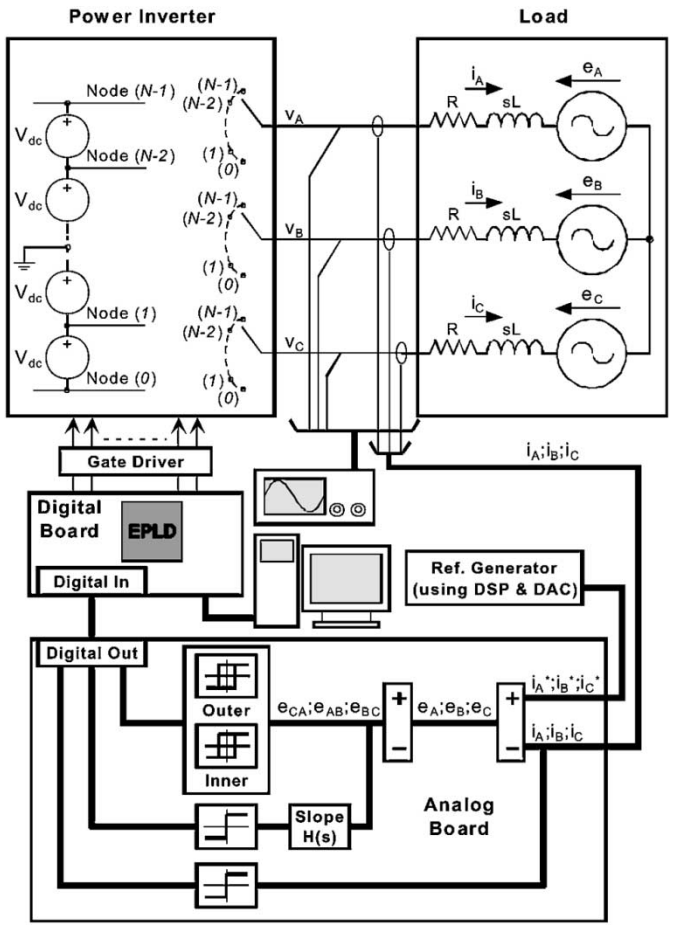

Fig. 8. General representation of experimental test system.

The state equations for the system can be written as (ignoring filter resistance since $R \ll L$)

$$v_A = v_U - v_V = e_A + L\frac{di_A}{dt}; \tag{1}$$

$$v_B = v_V - v_W = e_B + L\frac{di_B}{dt}; \tag{2}$$

$$v_C = v_W - v_U = e_C + L\frac{di_C}{dt} \tag{3}$$

where v_U, v_V, and v_W are outputs implicitly generated by regulators U, V, and W, respectively. Rearranging (1)–(3) gives

$$\begin{aligned} v_A - v_B &= v_U + v_W - 2v_V \\ &= e_A - e_B + L\left\{\frac{di_A}{dt} - \frac{di_B}{dt}\right\} \end{aligned} \tag{4}$$

$$\begin{aligned} v_B - v_C &= v_U + v_V - 2v_W \\ &= e_B - e_C + L\left\{\frac{di_B}{dt} - \frac{di_C}{dt}\right\} \end{aligned} \tag{5}$$

$$\begin{aligned} v_C - v_A &= v_V + v_W - 2v_U \\ &= e_C - e_A + L\left\{\frac{di_C}{dt} - \frac{di_A}{dt}\right\}. \end{aligned} \tag{6}$$

Since $v_U + v_V + v_W = 0$, (4), (5), and (6) can be expressed in term of the line currents as

$$[v_V, v_W, v_U]^T = \frac{1}{3}\{M \cdot [i_A, i_B, i_C]^T - [e_{AB}, e_{BC}, e_{CA}]^T\} \quad (7)$$

where

$$M = \begin{bmatrix} -Lp & Lp & 0 \\ 0 & -Lp & Lp \\ Lp & 0 & -Lp \end{bmatrix} \quad \text{and} \quad p = d/dt.$$

From (7), if the line currents are used as control variables, each regulator output is dependent on two control variables (because of the nonzero off-diagonal elements in M). Hence there will be cross-coupling interactions between any two current regulators.

On the other hand, if the delta currents are used as the control variables, (4), (5), and (6) become

$$[v_V, v_W, v_U]^T = \frac{1}{3}\{M' \cdot [i_{AB}, i_{BC}, i_{CA}]^T - [e_{AB}, e_{BC}, e_{CA}]^T\} \quad (8)$$

where

$$M' = \begin{bmatrix} -Lp & 0 & 0 \\ 0 & -Lp & 0 \\ 0 & 0 & -Lp \end{bmatrix}.$$

The presence of diagonal terms only in M' clearly implies the removal of cross-coupling effects, and the output of each regulator is now solely determined by a single delta current variable. Note that since the analysis is based on manipulating general state equations of a power electronic system, it is equally applicable for a linear current regulator and is similar in concept to the removal of phase coupling effects within a synchronous PI compensator used for uninterruptible power supplies [10], [11].

VI. Physical Implementation of Current Regulation Strategy

To validate the presented hysteresis current regulation strategy, an experimental prototype was implemented, as shown in Fig. 8. The hysteresis current regulators can be conveniently implemented using low cost analog op-amps (LF347), comparators (LM311) and a *Lattice Semiconductor* in-system complex programmable logic device (ispLSI2128E CPLD). On the analog controller board, the measured line currents are subtracted from the reference currents (generated using a DSP for convenience) to give the line current errors $\{e_A, e_B, e_C\}$, which are subtracted again to give the delta current errors $\{e_{CA} = e_C - e_A, e_{AB} = e_A - e_B, e_{BC} = e_B - e_C\}$. The delta current errors and their derivatives are then passed through comparators to generate intermediate logic signals. These intermediate signals are further processed by the CPLD on the digital board to generate signals suitable for switching the power inverter (a three-phase three-level inverter was implemented for this work). Note that the same controller structure can be used for controlling higher level inverters (limited only by the capacity of the CPLD) by simply re-programming the CPLD.

TABLE I
Parameters of Experimental Three-Level Inverter

DC link voltage	260V
Fundamental frequency	50Hz
First harmonic sideband	≈ 3.5kHz
Modulation depth	90%
Dead-time	2μs

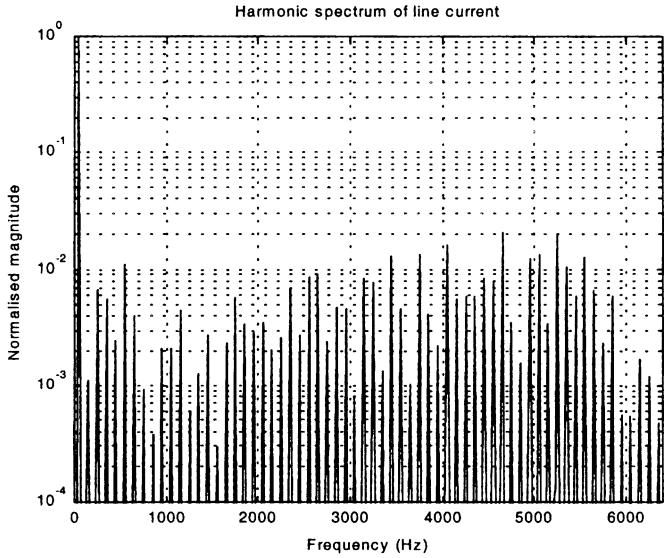

Fig. 9. Simulated current spectrum using HLCR regulation of a three-level inverter: THD (120th harmonic)= 5.6402.

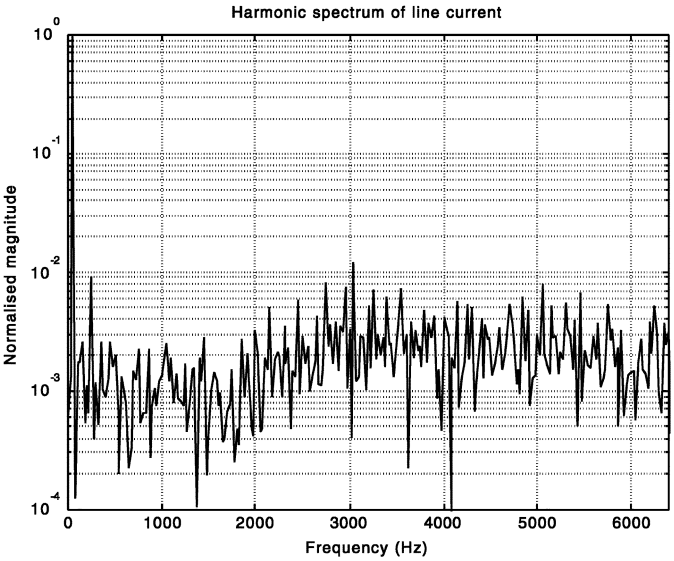

Fig. 10. Simulated current spectrum using HDCR regulation of a three-level inverter: THD (120th harmonic) = 3.8937.

The main complication associated with implementing the current regulators is their susceptibility to noise amplification while taking the derivatives of the delta current errors. Derivative inputs are essentially high pass filters, and noise injected through these filters can cause the digital state machine to oscillate rapidly between possible states. This can cause high frequency limit cycles at the inverter output. To filter off the high frequency noise, a differentiator with a second order roll

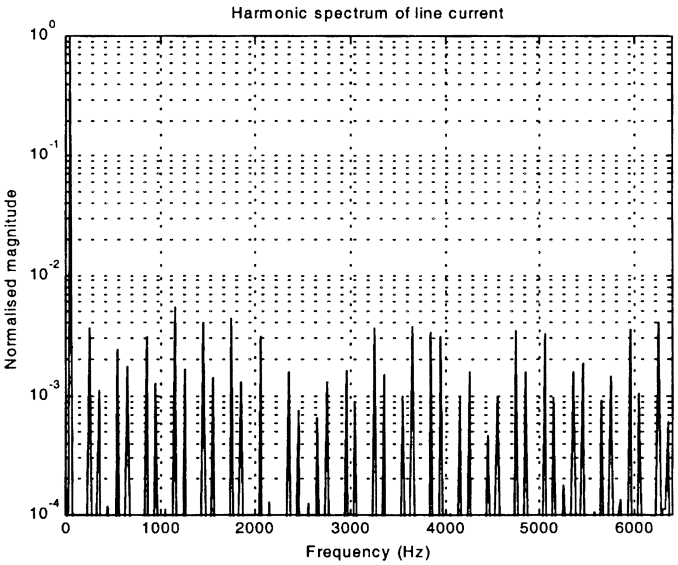

Fig. 11. Simulated current spectrum using HLCR regulation of a five-level inverter: THD (120th harmonic) = 1.5054.

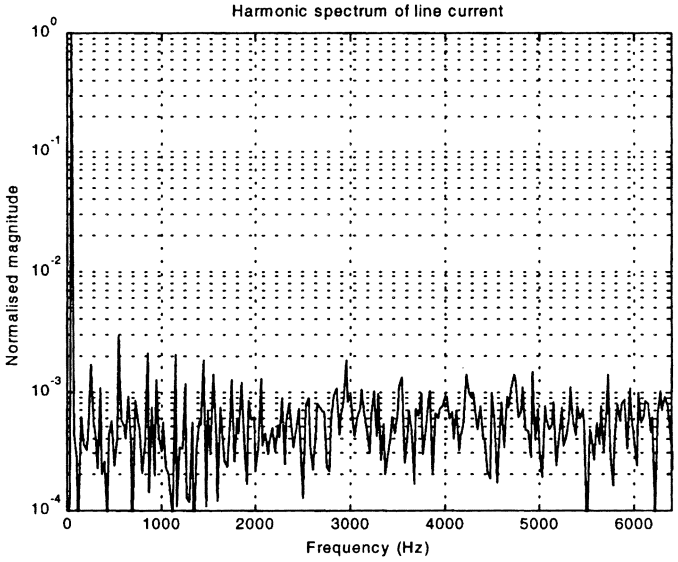

Fig. 12. Simulated current spectrum using HDCR regulation of a five-level inverter: THD (120th harmonic) = 0.8845.

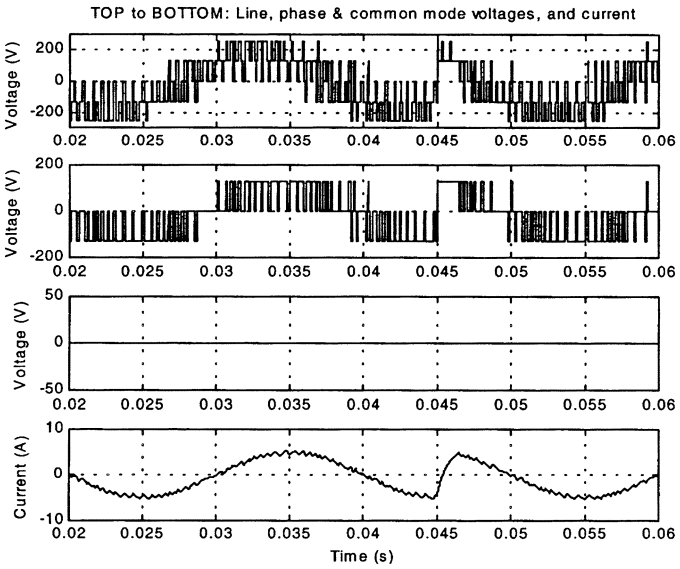

Fig. 13. Simulated switched waveforms using HDCR regulation of a three-level inverter with dead-time compensation.

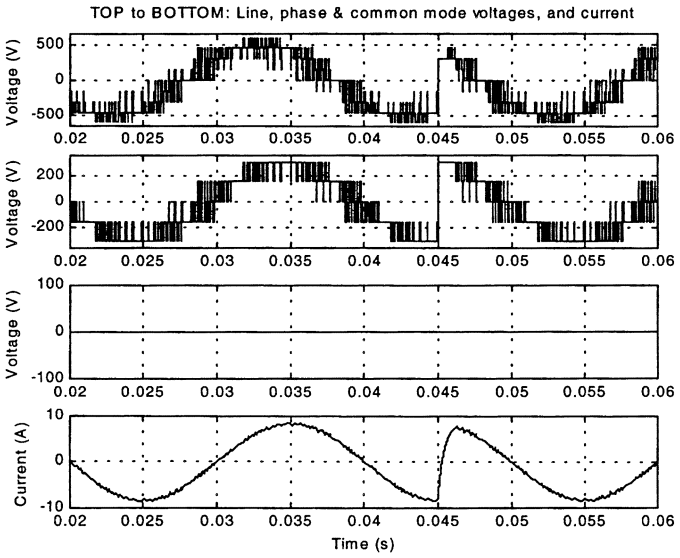

Fig. 14. Simulated switched waveforms using HDCR regulation of a five-level inverter with dead-time compensation.

off is adopted. The mathematical formulation of the selected differentiator can be written as

$$\frac{Y(s)}{X(s)} = \frac{Ks}{(s+\omega_1)(s+\omega_2)} \tag{9}$$

where $Y(s)$ = output of the differentiator, $X(s)$ = input to the differentiator, K = gain constant, $\omega_1; \omega_2$ = selected 3 dB cut−off frequencies.

Unfortunately, the two additional poles of the differentiator cause a phase lag in the detection of change of error direction. This lag can however be compensated within the digital logic by introducing a short lockout time interval to prevent further state change immediately after a switching event. This allows enough time for any changes to the current error slopes caused by a switching event to propagate through the controller board before the next switching decision is made.

VII. Simulation and Experimental Results

The performance of the current regulation strategy presented above has been verified in simulation for a three-level and a five-level inverter, and experimentally for a three-level inverter (parameters of the experimental inverter are given in Table I). The simulation investigations were performed with MATLAB Simulink and with practical effects such as sampled three-phase references and dead-time delays taken into consideration so as to match the experimental system closely. Note also that for the results presented, the term HLCR (Hysteresis Line Current Regulator) refers to the proposed current regulator using the line currents as the control variables while HDCR (Hysteresis Delta Current Regulator) refers to the regulator using the delta currents as the control variables.

To verify the performance improvement that can be achieved through the use of the delta currents as the control variables,

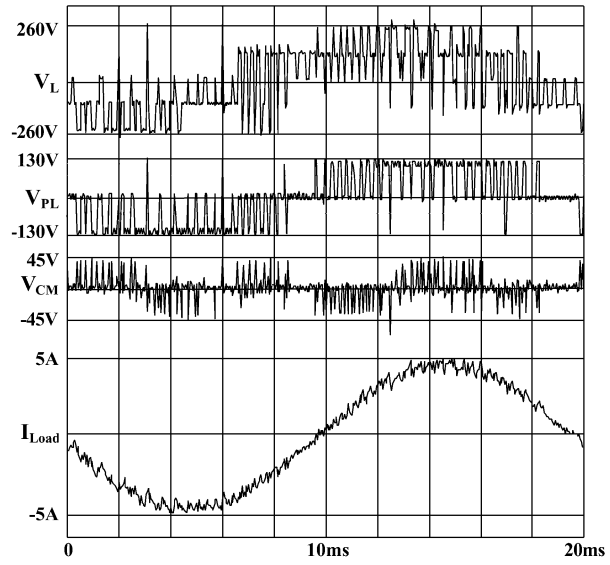

Fig. 15. Experimental switched waveforms using HDCR regulation of a three-level inverter without dead-time compensation: $\mathrm{V_L, V_{PL}, V_{CM}}$ = line, phase-leg, and common mode voltages; $\mathrm{I_{LOAD}}$ = current.

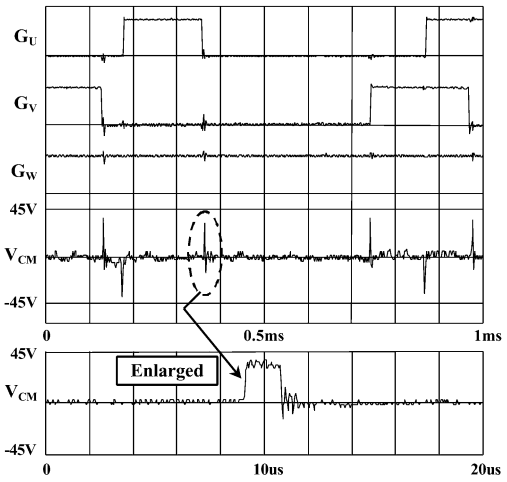

Fig. 16. Zoomed IN view of common mode spikes: G_U, G_V, G_W = current regulator outputs; V_{CM} = common mode voltage.

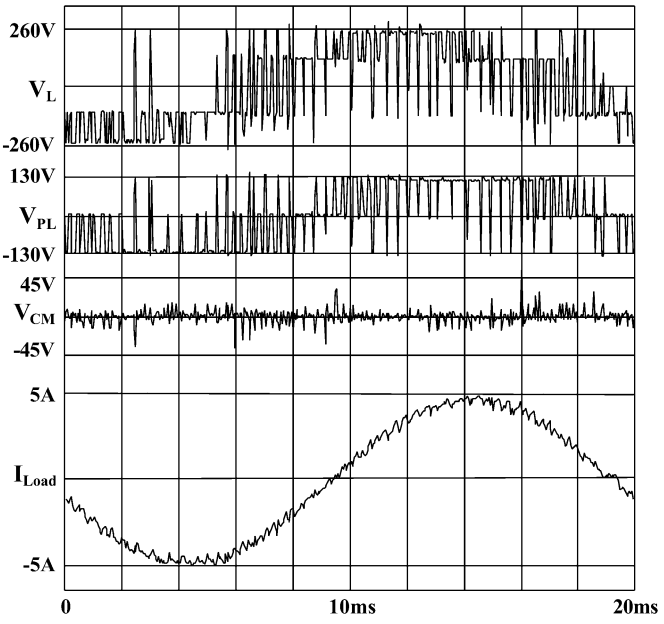

Fig. 17. Experimental switched waveforms using HDCR regulation of a three-level inverter with dead-time compensation: $V_L, V_{\mathrm{PL}}, V_{\mathrm{CM}}$ = line, phase-leg and common mode voltages; I_{LOAD} = current.

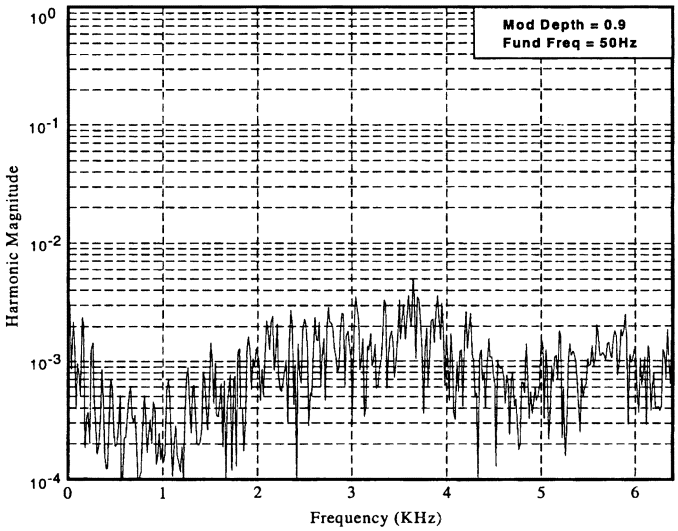

Fig. 18. Experimental spectrum of common mode voltage using HDCR regulation of a three-level inverter with dead-time compensation.

Figs. 9 and 10 show the simulated output current harmonic spectra when using the HLCR and HDCR current regulators respectively to control a three-level inverter. Figs. 11 and 12 show the obtained spectra with the regulators controlling a five-level inverter. Note the significantly improved harmonic performance (both low order and switching performances) of the HDCR regulator with much lower output current THD values. Due to this performance improvement, the experimental prototype was implemented with the HDCR regulator and subsequent results presented in this section are for the HDCR regulator only.

Fig. 13 shows the simulated switched waveforms of a three-level inverter controlled with the HDCR current regulator with dead-time compensation, while Fig. 14 shows the simulated waveforms for the case of a five-level inverter. These figures clearly show the effectiveness of the presented strategy in eliminating common mode voltage and its easy application to higher level inverters with the same level of effectiveness.

Fig. 15 shows the experimental switched waveforms of a three-level inverter controlled with the HDCR regulator without dead-time compensation, while Fig. 16 shows an enlarged view of the common mode voltage. As anticipated, in addition to achieving excellent reference tracking performance, the regulator reduces the common mode voltage to only transitional spikes of 2 μs duration (i.e., the dead-time interval) and has a magnitude of $V_{\mathrm{DC}}/3 \approx 45$ V. Fig. 17 shows the experimental switched waveforms with the proposed dead-time compensation technique incorporated to the HDCR regulator. Note the further reduction of common mode spikes as compared to Fig. 15. Fig. 18 shows the experimental harmonic spectrum

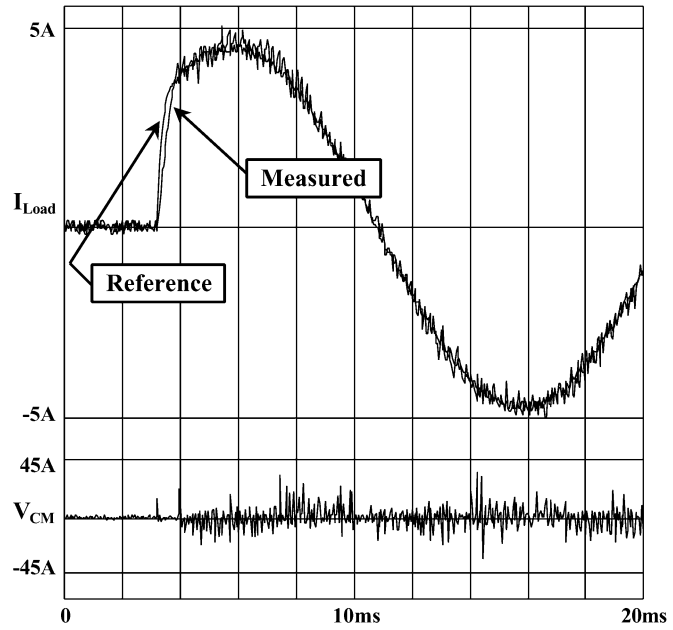

Fig. 19. Experimental transient performance using HDCR regulation of a three-level inverter: I_{LOAD} = current; V_{CM} = common mode voltage.

of the common mode voltage under these conditions, with no significant harmonics at all. Fig. 19 shows the experimental transient performance of the HDCR current regulator under a no-load to full-load step change, which confirms the excellent dynamic performance of the proposed regulator.

Lastly, it is commented that a reasonably high switching frequency was used for the above investigations to better illustrate the effectiveness of the presented regulation strategy in eliminating switching common mode voltage. The strategy can equally be used for (high power) low switching frequency applications with similar advantages.

VIII. Conclusion

This paper presents a new reduced common mode hysteresis current regulation technique for the control of multilevel inverters. The proposed technique is based on restricting the inverter phase-leg switching states to achieve reduced common mode voltages. By further compensating for dead-time delays across two phase-legs, common mode transitional spikes can also be eliminated. In addition, by selecting the delta current errors as the control variables, cross-couplings between independent control loops are removed and an improved low order harmonic performance is achieved.

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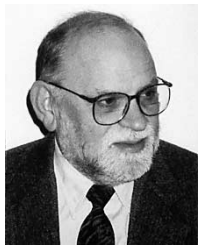

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