Investigation of 9-switch Dual-bridge Matrix Converter Operating under Low Output Power Factor

Lixiang Wei and Thomas A.Lipo

Department of Electrical and Computer Engineering The University of Wisconsin-Madison,
Madison, WI, 53705, USA

Abstract- The dual-bridge matrix converter (DBMC) concept has been gaining recognition as a promising circuit alternative in recent years. Among all the DBMC topologies with reduced number of switches, the 9-switch topology shows the least number of switches and high quality waveforms. However, it has been proven that this converter can not operate safely when the output power factor is less than 0.866. This paper proposes a novel method to operate the 9-switch DBMC with low output power factor loads. In order to accomplish this task, one additional clamp circuit switch is introduced to exchange power when the output power factor is lower than 0.866. With this switch, the 9- switch DBMC can continue to provide high quality input/output waveforms when the output power factor is not too low. Theoretical analysis, simulation and experimental results are presented in the paper to verify its effectiveness.

I. INTRODUCTION

The dual-bridge matrix converter (DBMC) is a relatively new developed concept [11[21[31[41. Compared to the conventional matrix converter[51, it possesses the same high quality performance, such as near sinusoidal inputloutput waveforms, adjustable input power factor, and compact system design due to absence of large energy storage components. Moreover, it has several other advantages over the conventional matrix converter, including easier and safer commutation, reduced number of switches, and a simple clamp circuit among others.

Among those topologies with reduced number of switches,
the 9-switch DBMC has the least number of switches that can provide high quality input/output waveforms (see figure. 1). However, one disadvantage of this converter is that its DC link current must remain non-negative to guarantee safe operation. If the DC link current becomes negative, high voltage spikes can be generated because there are no paths in the line side converter. Consequently, the converter will bedamaged by these spikes. It is mentioned in papers [21[31[41 that the output power factor should always be higher than 0.866 to guarantee safe operation of the converter.

In order to solve this problem, a simple clamp circuit was added to the converter I2IL4]. The clamp allows negative DC link current flow into the clamp capacitor for short periodsf time. However, the DC link current cannot be continuously negative because the voltage of the clamp capacitor cannot be charged for extended periods. Thus, the operation of this converter

under very low output power factor isstill not completely reliable.

This paper investigates the possibility of operating the 9- switch DBMC under low output power factor area. By introducing one additional switch in the clamp circuit, the power can be exchanged between the clamp capacitor and the converter and the converter can operate safely without any consideration of load side power factor. Moreover, both the simulation and experimental results show that the converter can still produce high quality inputloutput waveforms when the output factor is not too low.

Figure. 1: Configuration of the 9-switch DBMC

The paper is organized through the following steps. After a brief presentation of its space vector PWM control scheme, the reasons why 9-switch DBMC cannot operate under low output power factor is analyzed. Then, the proposed clamp circuit is illustrated and the operation of this circuit under low output power factor is discussed. Finally, simulation and experimental results are presented to verify the effectiveness of this method.

11. THE SPACE VECTOR PWM SCHEME AND ITS LIMITATION
ON THE 9-SWITCH DBMC

One limitation of the 9-switch DBMC is that the DC link

current id, 2 0 must be guaranteed. Thus, the space vector PWM scheme [11[21[41 is only applicable to the 9-switch DBMC when the DC link current is nonnegative.

In order to simplify the analysis, it is assumed that there is
no input filter on the line side. Hence, from Fig. 1 :

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Lf =O; Cf =O; V, =Vx; i, =ix; x=a,b,c

It is assumed that the input source voltages are described by

v,, = v, case, = v, cos(ait)

vsb = v, cos eb = v, COS(a,t - -)

v,, = v, cos 8, = V, COS(a,t + -)

(1)

2.n
3
2n
3

and the output currents are

is, = I, cos 8,i = I, cos(8, - cp,)

2rt is, = I, cos(8, - cp, --) 3

237 is, = I, cos(8, - cp, + -) I 3

where a, and a,are the input and output angular

frequencies, 8, is the angle of the expected output voltage

vector and cp, is the output power factor angle. V, and I, are the amplitudes of input voltage and output current respectively.

A. Six intervals and two portions

To enhance safe commutation, the space vector PWM control method mentioned in paper [2] identified six intervals based on detection of the input voltage synchronization angle (see figure. 2). During each interval, only one of the three-phase input voltages has the largest absolute value. For example, V,, has the largest absolute voltage in interval 1, and Vsc has the largest absolute voltage in interval 2 and so forth.

1 2 3 4 5 6 1

Fig. 2. Six intervals of a switching cycle

Two portions are also identified ineach switching cycle. In each portion, some appropriate switching behavior can be analyzed on different switches according to the number of intervals to replace the DBMC topology as a DC/AC inverter.

For example, V,, in interval 2 has the largest absolute voltage, the two largest positive line voltages are V,, -V,, and Vsb -Vsc respectively. The line side switching states in each portion can be determined by the following stages:

In portion 1, sbm, and S,, remains turned on; Sum remains

turned off. The DC side voltage Vdc is then equal to Vsb - V,,, the DC side current id, equals i,b and -is,, and is,
equals zero. The duty ratio of this portion is defined as dbr.

0 In portion 2, Sum and S,, remains turned on; sb, remains turned off. The DC side voltage Vdc equals Vab -Vs,, the DC side current id, equals is, and -is,, and isb equals zero. The duty ratio of this portion is defined by d,,

i L L L l

(a) Portion 1 (b) Portion 2
Figure. 3: Equivalent circuit in interval 2

Figure 3 shows the equivalent circuits of the converter during these two portions of interval 2. With these equivalent circuits, the converter can be considered as an equivalent DC/AC inverter with different DC voltages during each of the two portions. The commutation of the various switches has been discussed in [2] in detail and will not be addressed further in this paper.

B. Space vector P WM control

Initially, it is useful to consider the conventional VSI with three-phase output voltage V,, , V,, , and Vsw supplied by a

DC voltage source V,, = 3 V,, /2 .

In complex form, the space vector of the desired output voltages is

Where 0 < k < &/2 is a constant.

Supposing 0 < 8, < zf3 and that the system operates in

interval 2, this vector can be approximated by its two

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adjacent voltage vectors (V, and V2) and the zero voltage
vector Vo as shown in Fig. 9. The duty ratios of these vectors
are

When the system operates during the other intervals or
when 0, > .n/3 , the Same results can be obtained.

2k x 2k . d1 =-sin(- - 8,) ; d2 = -sin(e,) ; do = 1 - dl - d2 (4) C. DC link current and the load sidepower factor 453 &
Since the DC side current equals to is, while the output The DC current of the inverter at voltage vectors Vo, Vl and
V2 can be expressed as 0, is,, and -is," respectively. The
average DC current of the inverter with the above duty ratios

voltage is V1, then from equation (2)

is determined as (9) id, = I, cos(e, - cpo) 2 o

(5) Thus one has

(10) Because there are two portions during each switching

cycle, the duty ratios V,, V2, and Vo are also distributed to

x -cp <- x
2

Because 0<0, <x/3, the following equations can be

O-2

each portion. During the first portion, they are:

dlbc = dl . lCOS 8b I ; d2bc = d2 . ICOS 8b I derived from (1 0)
dObc =do 12; dbc = dlbc + d2bc + dObc (6)
-

During the second portion,

x 7T -29 <-
6 '-2

dlac = dl .Icos~,I ; dzac = d2 . ~COS 8, I On the other hand, the DC side current equals to -is,,, while
the output voltage is V2, then from equation (2) doac =do /2 ; dac = dlac + d2ac + doac (7)

011

A v22,t2

/\

idc = -I, cos(0, - cpo + -1 2.n 2 0
3

Thus one obtains

x 2.n 3x

2 3 2 -I0, -To +-I-

Because 0 < 0, < x/3, the following equation can be derived from (1 3)

(14)

x x --Icp, I-

2 6 v, , f1
001

Thus, to apply the space vector PWM control method to the 9-switch DBMC topology, the output power factor angle can be derived from equation (1 1) and (14) as

3v,
2

000
111

Figure 4 Space vector PWM for inverter while 0 < 8, < X/3

(15)

x 72: Combining from Equations (3) to (7), the actual average
output voltage vector and the input current can finally be
obtained as

- - I 'p, I- or cos cp, I 0.866
6 6

- v, =k.-L8,; 3vm is, =Iim 'cos0,

i,b = I, ' cos 8b ; is, = I, . cos 8,

2

(8)

This result demonstrates that the space vector PWM control method generates the same actual output voltage as the reference voltage and that the line side power factor can inherently remain at unity.

This is a strict limitation for the 9-switch DBMC topology
if there are no additional circuits in the DC link to provide paths for the negative current. Consequently, the application of this topology is somewhat limited, for instance, it can not reliably operate an induction motor drive.

111. THE PROPOSED CLAMP CIRCUIT

A simple clamp circuit with only one capacitor and one diode has been proposed in ~aper[~][~]; however, one

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limitation of this clamp circuit is that it only allows the power flow from the DC link to the clamp circuit. When the output power factor is lower than 0.866, the current flows into this clamp capacitor continuously to increase its voltage. If this voltage is too high, some of the components will be damaged.

Figure.5 shows a novel clamp circuit. Comparing to the clamp circuit in paper['], this circuit has one additional switch to exchange the power between the clamp capacitor and the converter. The operation of this circuit is shown below:

When the converter is started, all the switches inthe line
side turn on initially and the clamp capacitor voltage is charged up to the maximum peak line voltage.
"P
I T T T T

Figure. 5: Configuration ofthe 9-switch DBMC with new clamp circuit

-

Under a fault state, all switches in the converter are turned off immediately. The energy stored in the inductive load flows into the clamp capacitor to avoid high voltage spikes.

During normal operation, if the clamp voltage V,, is higher than the threshold voltage V,h, the clamp switch Sc turns on. Then the line side converter is anti-biased because the threshold voltage is higher than the maximum amplitude of the input line voltage. In this condition, the voltage of clamp capacitor begins to reduce because it provides power for the load. Figure. 6 shows the equivalent circuit of the 9-switch DBMC when Sc is turned on.

During normal operation, if the clamp voltage VC1 is lower than the threshold voltage, the clamp switch Sc is turned off. The line side switches startso operate again. Figure 7 shows the equivalent circuit of the 9-switch DBMC when Sc is turned off.

From the analysis, it can be determined that the 9-switch DBMC can operate safely when the output power factor is lower than 0.866. However, since the space vector PWM is not applicable in this condition, some low order harmonics will be generated when the output power factor is lower than 0.866.

Iv. SIMULATION RESULTS

The operation of the 9-switch DBMC with an inductive load has been extensively investigated through simulation. The parameters of this converter using MATLAB are:

Input Line voltage: 230V; Input frequency: 60Hz
Filter inductor: 200uH; Threshold voltage: 320V
Filter capacitor: 30uF; Clamp capacitor: 30uF

The output load is adjusted to create the expected output power factor. Figures 8, 9, and 10 show the waveforms of the 9-switch DBMC when the output power factor equals to
0.707, 0.5, and 0.2 respectively. The waveforms presented in these figures are DC link voltage, input/output current.

Figure.6: Equivalent circuit of the circuit when Sc turns on

vP
I T T T T T I

.

I I I

Figure.7: Equivalent circuit of the 9-switch DBMC when Sc turns off

From figures 8 and 9, it can be found that the 9-switch
DBMC can still provide high quality inputioutput waveform when the output power factor is not too low. Figure 10 shows
that the input current waveform is obvious distorted when output power factor is low.

Figure 11 shows experimental results for the 9-switch DBMC while output power is higher than 0.866. Figures 12 and 13 show the waveforms of the 9-switch DBMC when the output power factor equals to 0.7 and 0.2 respectively operating with the same parameters. From these three figures, one can note that the waveforms of the nine switch DBMC under low output power factor has the same high quality inputioutput waveforms as the high output power factor area. Safe operation of the converter under low output power factor loads have clearly been verified.

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c --- I I

8 100' I
0145 015 0155 016 0165 017 0175 018

2 -201 I

9 1

0145 015 0155 016 0165 017 0175 018

- 50

-

Q

- 501
0145 015 0155 016 0165 017 0175 018
tbl

Figure. 8: Simulation result of the inpuuoutput waveforms while output power factor is 0.707

400 I I

8 1001 I
0.145 0.15 0.155 0.16 0.165 0.17 0.175 0.18

- 20 51 1

- -
: -201
0145 015 0155 016 0165 017 0175 018

I.

c -I-
m

$ 200
1 c
-

' .?8b6 -0 045 -0 b4
P 201

4.62 -0 d15 -0 bl -0 OR5

'

Figure. 11: Experimental result of input'output waveforms while output power factor is higher than 0.866

4001 I

8 01 22 221 222 223 224 225 226 227 228 229 23
5. 10,

m

s -

5 0

5, -

"'!?2 221 222 223 224 225 226 227 228 229 23

Q

-501
0145 015 0155 016 0165 017 0175 018
tb)

Figure.9: Simulation result of the inpub'output waveforms during operation at a power factor of 0.50

- 400 I I

m

300

0 >* 200 - -
8 1001 I
0145 015 0155 016 0165 017 0175 018

I

.- -20 I I
0.145 0.15 0.155 0.16 0.165 0.17 0.175 0.18
I

I
0.145 0.15 0.155 0.16 0.165 0.17 0175 0.18
t(s)

Figure. 10: Simulation result of the inpuuoutput waveforms while output power factor is 0.20

.-

-'?I2 2.>1 2.12 2 23 2.>4 2.25 2.>6 2.>7 2.k 2.29 213

t ($1

Figure. 12: Experimental result of input/output waveforms while the output power factor is 0.7

8 01 I 2.2 2.21 2.22 2.23 2.24 2.25 2.26 2.27 2.28 2.29 2.3
- 10 51

a -101 I

- 5 9

50

c -5

22 221 222 223 224 225 226 227 228 229 23

-

c m

u
+

22 221 222 223 224 225 226 227 228 229 23

t ($1

Figure. 13: Experimental results for inpuuoutput waveforms while the output power factor is 0.20

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V. CONCLUSION [5] M. Venturini , "A new sine wave in, sine wave out, conversion

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The 9-switch DBMC can generate high quality input/output
waveforms with the least number of switches. However. it 1980, pp. E3-1-E3-15.
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when the output power factor is always higher than 0.866. [6] P.D.Ziogas, Y. Kang, V.R. Stefanovic and et al, " Rectifier-
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circuit with one switch, one diode, and one capacitors
proposed in the paper to protect the converter under low

simulation and experimental results verify that the 9-switch

circuit

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The DBMC can still provide high quality inputioutput
waveform when the output power factor is not too low.

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0

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As a result, this converter can be used to drive different motors with high quality waveforms, such as induction machines, permanent magnet synchronous machines etc.; However, one disadvantage of this converter is that when
the output power factor is very low, some low order harmonics are generated in the line side current.

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VII. REFERENCES

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