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Investigation of 9-switch Dual-bridge Matrix Converter Operating under Low Output Power Factor

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Abstract- **The dual-bridge matrix converter (DBMC) concept has been gaining recognition as a promising circuit alternative in recent years. Among all the DBMC topologies with reduced number of switches, the 9-switch topology shows the least number of switches and high quality waveforms. However, it has been proven that this converter can not operate safely when the output power factor is less than 0.866. This paper proposes a novel method to operate the 9-switch DBMC with low output power factor loads. In order to accomplish this task, one additional clamp circuit switch is introduced to exchange power when the output power factor is lower than 0.866. With this switch, the 9-switch DBMC can continue to provide high quality input/output waveforms when the output power factor is not too low. Theoretical analysis, simulation and experimental results are presented in the paper to verify its effectiveness.**

I. INTRODUCTION

The dual-bridge matrix converter (DBMC) is a relatively new developed concept [1][2][3][4]. Compared to the conventional matrix converter[5], it possesses the same high quality performance, such as near sinusoidal input/output waveforms, adjustable input power factor, and compact system design due to absence of large energy storage components. Moreover, it has several other advantages over the conventional matrix converter, including easier and safer commutation, reduced number of switches, and a simple clamp circuit among others.

Among those topologies with reduced number of switches, the 9-switch DBMC has the least number of switches that can provide high quality input/output waveforms (see figure.1). However, one disadvantage of this converter is that its DC link current must remain non-negative to guarantee safe operation. If the DC link current becomes negative, high voltage spikes can be generated because there are no paths in the line side converter. Consequently, the converter will be damaged by these spikes. It is mentioned in papers [2][3][4] that the output power factor should always be higher than 0.866 to guarantee safe operation of the converter.

In order to solve this problem, a simple clamp circuit was added to the converter [2][4]. The clamp allows negative DC link current flow into the clamp capacitor for short periods of time. However, the DC link current cannot be continuously negative because the voltage of the clamp capacitor cannot be charged for extended periods. Thus, the operation of this converter under very low output power factor is still not completely reliable.

This paper investigates the possibility of operating the 9-switch DBMC under low output power factor area. By introducing one additional switch in the clamp circuit, the power can be exchanged between the clamp capacitor and the converter and the converter can operate safely without any consideration of load side power factor. Moreover, both the simulation and experimental results show that the converter can still produce high quality input/output waveforms when the output factor is not too low.

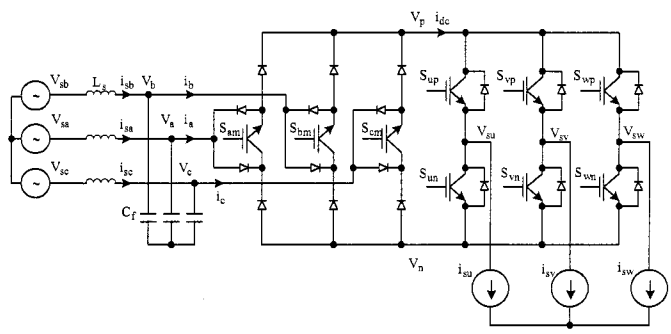

Figure.1: Configuration of the 9-switch DBMC

The paper is organized through the following steps. After a brief presentation of its space vector PWM control scheme, the reasons why 9-switch DBMC cannot operate under low output power factor is analyzed. Then, the proposed clamp circuit is illustrated and the operation of this circuit under low output power factor is discussed. Finally, simulation and experimental results are presented to verify the effectiveness of this method.

II. THE SPACE VECTOR PWM SCHEME AND ITS LIMITATION ON THE 9-SWITCH DBMC

One limitation of the 9-switch DBMC is that the DC link current $i_{dc} \geq 0$ must be guaranteed. Thus, the space vector PWM scheme [1][2][4] is only applicable to the 9-switch DBMC when the DC link current is nonnegative.

In order to simplify the analysis, it is assumed that there is no input filter on the line side. Hence, from Fig.1:

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$$L_f = 0\,;\; C_f = 0\,;\; V_{sx} = V_x\,;\; i_{sx} = i_x\,;\; x = a,b,c$$

It is assumed that the input source voltages are described by

$$\begin{cases} V_{sa} = V_m \cos\theta_a = V_m \cos(\omega_i t) \\ V_{sb} = V_m \cos\theta_b = V_m \cos(\omega_i t - \frac{2\pi}{3}) \\ V_{sc} = V_m \cos\theta_c = V_m \cos(\omega_i t + \frac{2\pi}{3}) \end{cases} \quad (1)$$

and the output currents are

$$\begin{cases} i_{su} = I_o \cos\theta_{oi} = I_o \cos(\theta_o - \varphi_o) \\ i_{sv} = I_o \cos(\theta_o - \varphi_o - \frac{2\pi}{3}) \\ i_{sw} = I_o \cos(\theta_o - \varphi_o + \frac{2\pi}{3}) \end{cases} \quad (2)$$

where ω_i and ω_o are the input and output angular frequencies, θ_o is the angle of the expected output voltage vector and φ_o is the output power factor angle. V_m and I_o are the amplitudes of input voltage and output current respectively.

A. *Six intervals and two portions*

To enhance safe commutation, the space vector PWM control method mentioned in paper [2] identified six intervals based on detection of the input voltage synchronization angle (see figure. 2). During each interval, only one of the three-phase input voltages has the largest absolute value. For example, V_{sa} has the largest absolute voltage in interval 1, and V_{sc} has the largest absolute voltage in interval 2 and so forth.

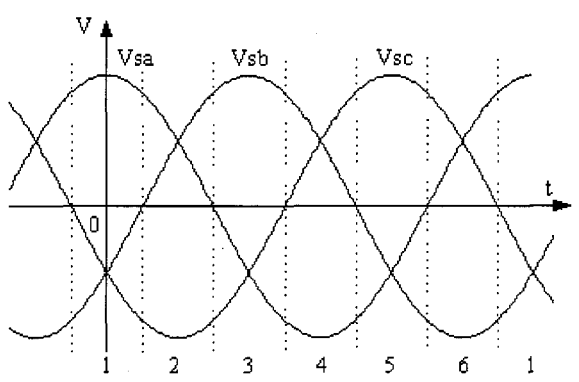
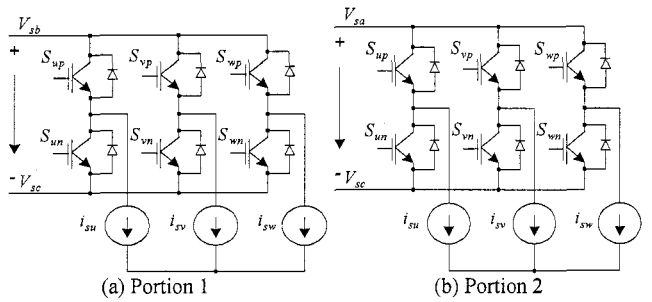


Fig. 2. Six intervals of a switching cycle

Two portions are also identified in each switching cycle. In each portion, some appropriate switching behavior can be analyzed on different switches according to the number of intervals to replace the DBMC topology as a DC/AC inverter.

For example, V_{sc} in interval 2 has the largest absolute voltage, the two largest positive line voltages are V_{sa} -V_{sc} and V_{sb} -V_{sc} respectively. The line side switching states in each portion can be determined by the following stages:

- In portion 1, S_{bm}, and S_{cm} remains turned on; S_{am} remains turned off. The DC side voltage V_{dc} is then equal to V_{sb} - V_{sc}, the DC side current i_{dc} equals i_{sb} and $-i_{sc}$, and i_{sa} equals zero. The duty ratio of this portion is defined as d_{bc}.
- In portion 2, S_{am} and S_{cm} remains turned on; S_{bm} remains turned off. The DC side voltage V_{dc} equals V_{ab} -V_{sc}, the DC side current i_{dc} equals i_{sa} and $-i_{sc}$, and i_{sb} equals zero. The duty ratio of this portion is defined by d_{ac}.



(a) Portion 1 (b) Portion 2

Figure. 3: Equivalent circuit in interval 2

Figure 3 shows the equivalent circuits of the converter during these two portions of interval 2. With these equivalent circuits, the converter can be considered as an equivalent DC/AC inverter with different DC voltages during each of the two portions. The commutation of the various switches has been discussed in [2] in detail and will not be addressed further in this paper.

B. Space vector PWM control

Initially, it is useful to consider the conventional VSI with three-phase output voltage V_{su}, V_{sv}, and V_{sw} supplied by a DC voltage source $V_{dc} = 3 \cdot V_m / 2$.

In complex form, the space vector of the desired output voltages is

$$\vec{V}_{o_ref} = V_{su} + V_{sv} \cdot e^{j\frac{2\pi}{3}} + V_{sw} \cdot e^{-j\frac{2\pi}{3}} = k \cdot \frac{3V_m}{2} \angle\theta_o \quad (3)$$

Where $0 < k < \sqrt{3}/2$ is a constant.

Supposing $0 < \theta_o < \pi/3$ and that the system operates in interval 2, this vector can be approximated by its two

adjacent voltage vectors (V_1 and V_2) and the zero voltage vector V_0 as shown in Fig. 9. The duty ratios of these vectors are

$$d_1 = \frac{2k}{\sqrt{3}}\sin(\frac{\pi}{3} - \theta_o)\,;\, d_2 = \frac{2k}{\sqrt{3}}\sin(\theta_o)\,;\, d_0 = 1 - d_1 - d_2 \quad (4)$$

The DC current of the inverter at voltage vectors V_0, V_1 and V_2 can be expressed as 0, i_{su}, and $-i_{sw}$ respectively. The average DC current of the inverter with the above duty ratios is determined as

$$i_{dc} = k \cdot I_o \cdot \cos(\theta_o - \theta_{oi}) = I_{im} \quad (5)$$

Because there are two portions during each switching cycle, the duty ratios V_1, V_2, and V_0 are also distributed to each portion. During the first portion, they are:

$$d_{1bc} = d_1 \cdot |\cos\theta_b|\,; \qquad d_{2bc} = d_2 \cdot |\cos\theta_b|$$
$$d_{0bc} = d_0/2\,; \qquad d_{bc} = d_{1bc} + d_{2bc} + d_{0bc} \quad (6)$$

During the second portion,

$$d_{1ac} = d_1 \cdot |\cos\theta_a|\,; \qquad d_{2ac} = d_2 \cdot |\cos\theta_a|$$
$$d_{0ac} = d_0/2\,; \qquad d_{ac} = d_{1ac} + d_{2ac} + d_{0ac} \quad (7)$$

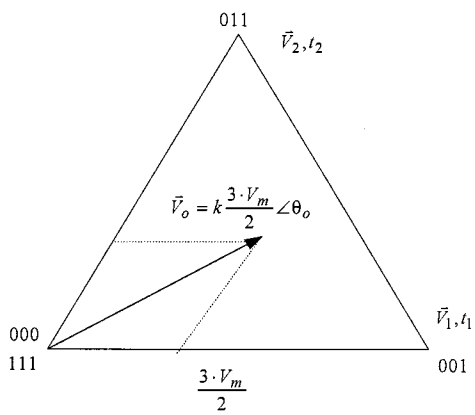


Figure. 4: Space vector PWM for inverter while $0 < \theta_o < \pi/3$

Combining from Equations (3) to (7), the actual average output voltage vector and the input current can finally be obtained as

$$\vec{V}_o = k \cdot \frac{3V_m}{2}\angle\theta_o\,;\; i_{sa} = I_{im} \cdot \cos\theta_a$$
$$i_{sb} = I_{im} \cdot \cos\theta_b\,;\; i_{sc} = I_{im} \cdot \cos\theta_c \quad (8)$$

This result demonstrates that the space vector PWM control method generates the same actual output voltage as the reference voltage and that the line side power factor can inherently remain at unity.

When the system operates during the other intervals or when $\theta_o > \pi/3$, the same results can be obtained.

C. DC link current and the load side power factor

Since the DC side current equals to i_{su} while the output voltage is V_1, then from equation (2)

$$i_{dc} = I_o \cos(\theta_o - \varphi_o) \geq 0 \quad (9)$$

Thus one has

$$-\frac{\pi}{2} \leq \theta_o - \varphi_o \leq \frac{\pi}{2} \quad (10)$$

Because $0 < \theta_o < \pi/3$, the following equations can be derived from (10)

$$-\frac{\pi}{6} \leq \varphi_o \leq \frac{\pi}{2} \quad (11)$$

On the other hand, the DC side current equals to $-i_{sw}$ while the output voltage is V_2, then from equation (2)

$$i_{dc} = -I_o \cos(\theta_o - \varphi_o + \frac{2\pi}{3}) \geq 0 \quad (12)$$

Thus one obtains

$$\frac{\pi}{2} \leq \theta_o - \varphi_o + \frac{2\pi}{3} \leq \frac{3\pi}{2} \quad (13)$$

Because $0 < \theta_o < \pi/3$, the following equation can be derived from (13)

$$-\frac{\pi}{2} \leq \varphi_o \leq \frac{\pi}{6} \quad (14)$$

Thus, to apply the space vector PWM control method to the 9-switch DBMC topology, the output power factor angle can be derived from equation (11) and (14) as

$$-\frac{\pi}{6} \leq \varphi_o \leq \frac{\pi}{6} \text{ or } \cos\varphi_o \leq 0.866 \quad (15)$$

This is a strict limitation for the 9-switch DBMC topology if there are no additional circuits in the DC link to provide paths for the negative current. Consequently, the application of this topology is somewhat limited, for instance, it can not reliably operate an induction motor drive.

III. THE PROPOSED CLAMP CIRCUIT

A simple clamp circuit with only one capacitor and one diode has been proposed in paper[2][4]; however, one

limitation of this clamp circuit is that it only allows the power flow from the DC link to the clamp circuit. When the output power factor is lower than 0.866, the current flows into this clamp capacitor continuously to increase its voltage. If this voltage is too high, some of the components will be damaged.

Figure.5 shows a novel clamp circuit. Comparing to the clamp circuit in paper[2], this circuit has one additional switch to exchange the power between the clamp capacitor and the converter. The operation of this circuit is shown below:

- When the converter is started, all the switches in the line side turn on initially and the clamp capacitor voltage is charged up to the maximum peak line voltage.

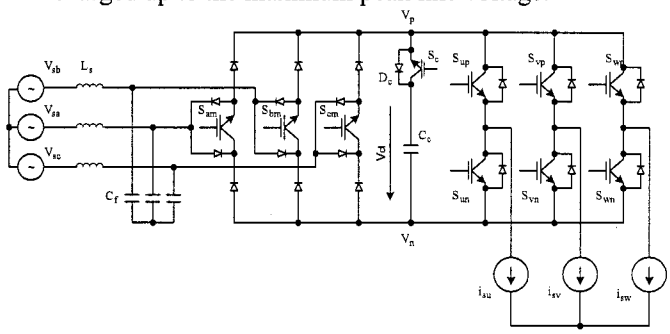


Figure. 5: Configuration of the 9-switch DBMC with new clamp circuit

- Under a fault state, all switches in the converter are turned off immediately. The energy stored in the inductive load flows into the clamp capacitor to avoid high voltage spikes.

- During normal operation, if the clamp voltage V_{cl} is higher than the threshold voltage V_{th}, the clamp switch Sc turns on. Then the line side converter is anti-biased because the threshold voltage is higher than the maximum amplitude of the input line voltage. In this condition, the voltage of clamp capacitor begins to reduce because it provides power for the load. Figure. 6 shows the equivalent circuit of the 9-switch DBMC when Sc is turned on.

- During normal operation, if the clamp voltage V_{cl} is lower than the threshold voltage, the clamp switch Sc is turned off. The line side switches starts to operate again. Figure 7 shows the equivalent circuit of the 9-switch DBMC when Sc is turned off.

From the analysis, it can be determined that the 9-switch DBMC can operate safely when the output power factor is lower than 0.866. However, since the space vector PWM is not applicable in this condition, some low order harmonics will be generated when the output power factor is lower than 0.866.

IV. SIMULATION RESULTS

The operation of the 9-switch DBMC with an inductive load has been extensively investigated through simulation. The parameters of this converter using MATLAB are:

Input Line voltage:	230V;	Input frequency:	60Hz
Filter inductor:	200uH;	Threshold voltage:	320V
Filter capacitor:	30uF;	Clamp capacitor:	30uF

The output load is adjusted to create the expected output power factor. Figures 8, 9, and 10 show the waveforms of the 9-switch DBMC when the output power factor equals to 0.707, 0.5, and 0.2 respectively. The waveforms presented in these figures are DC link voltage, input/output current.

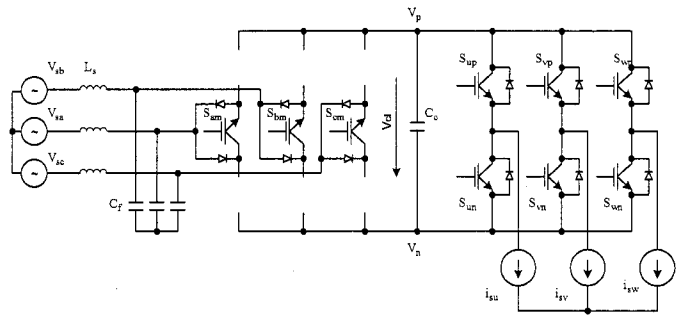


Figure.6: Equivalent circuit of the circuit when Sc turns on

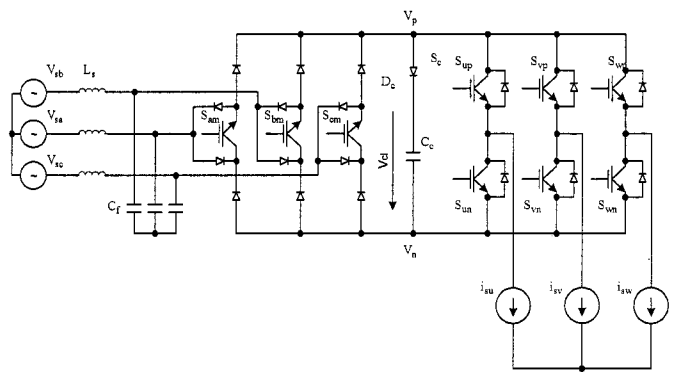


Figure.7: Equivalent circuit of the 9-switch DBMC when Sc turns off

From figures 8 and 9, it can be found that the 9-switch DBMC can still provide high quality input/output waveform when the output power factor is not too low. Figure 10 shows that the input current waveform is obvious distorted when output power factor is low.

Figure 11 shows experimental results for the 9-switch DBMC while output power is higher than 0.866. Figures 12 and 13 show the waveforms of the 9-switch DBMC when the output power factor equals to 0.7 and 0.2 respectively operating with the same parameters. From these three figures, one can note that the waveforms of the nine switch DBMC under low output power factor has the same high quality input/output waveforms as the high output power factor area. Safe operation of the converter under low output power factor loads have clearly been verified.

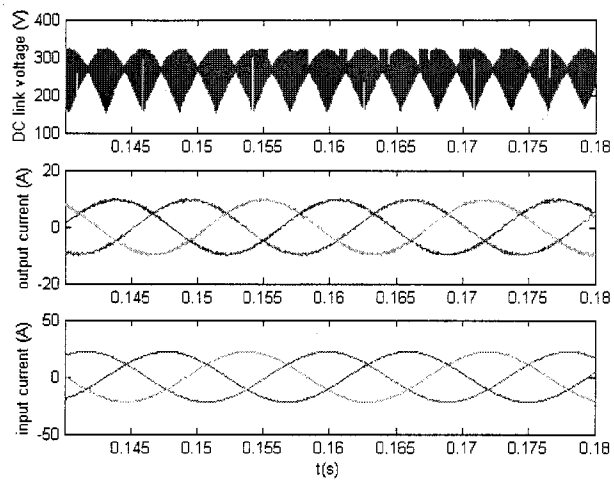


Figure.8: Simulation result of the input/output waveforms while output power factor is 0.707

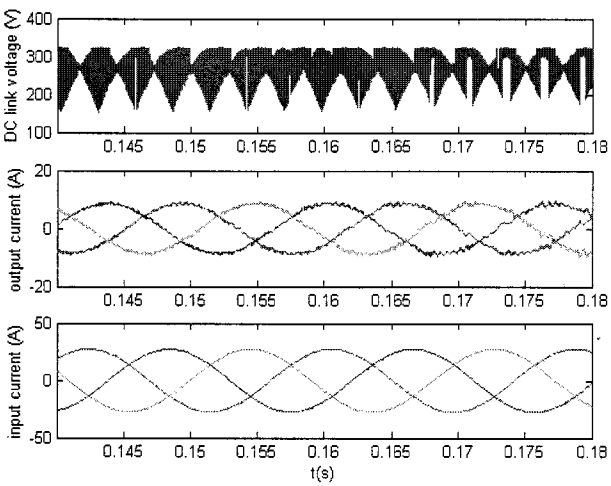


Figure.9: Simulation result of the input/output waveforms during operation at a power factor of 0.50

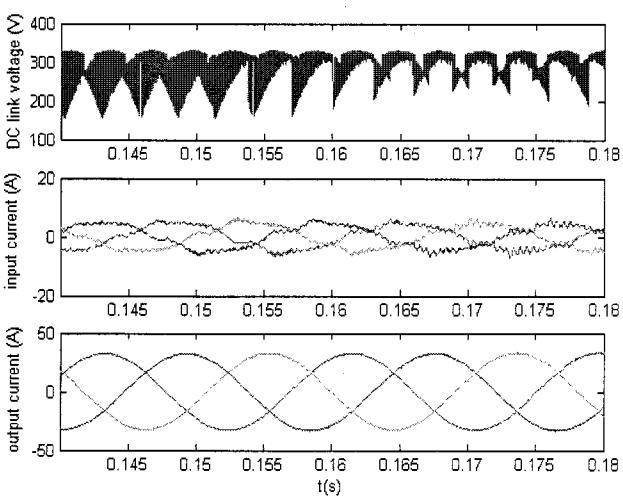


Figure.10: Simulation result of the input/output waveforms while output power factor is 0.20

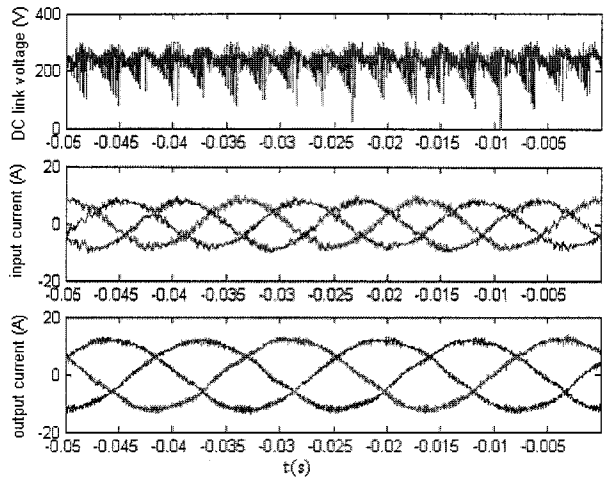


Figure.11: Experimental result of input/output waveforms while output power factor is higher than 0.866

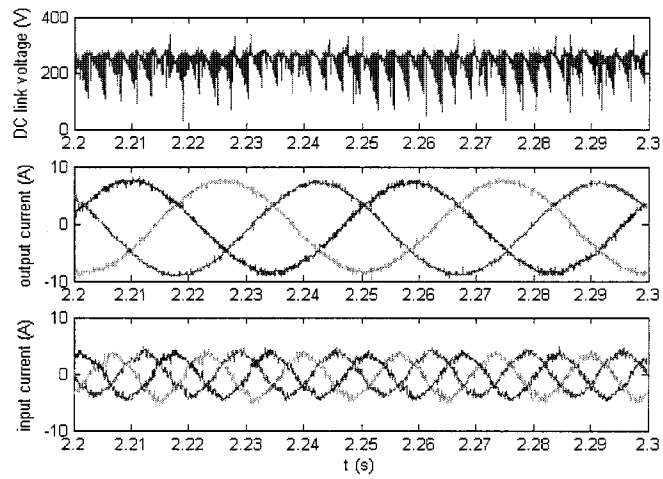


Figure.12: Experimental result of input/output waveforms while the output power factor is 0.7

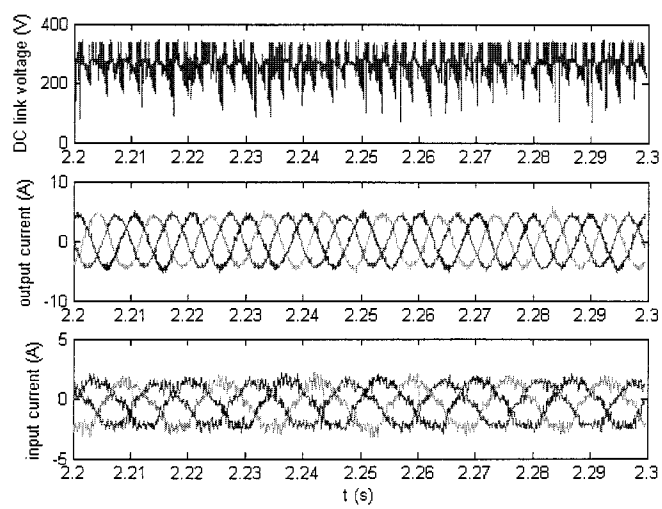


Figure.13: Experimental results for input/output waveforms while the output power factor is 0.20

V. CONCLUSION

The 9-switch DBMC can generate high quality input/output waveforms with the least number of switches. However, it has been shown that this converter can only operate safely when the output power factor is always higher than 0.866. This paper investigates the possibility of running this converter under a low output power factor. A novel clamp circuit with one switch, one diode, and one capacitor is proposed in the paper to protect the converter under low output power factor conditions. Theoretical analysis, simulation and experimental results verify that the 9-switch DBMC has the following characteristics with this clamp circuit

- The DBMC can operate safely without regard to the output power factor;
- The DBMC can still provide high quality input/output waveform when the output power factor is not too low. As a result, this converter can be used to drive different motors with high quality waveforms, such as induction machines, permanent magnet synchronous machines etc.;
- However, one disadvantage of this converter is that when the output power factor is very low, some low order harmonics are generated in the line side current.

VI. ACKNOWLEDGEMENT

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