

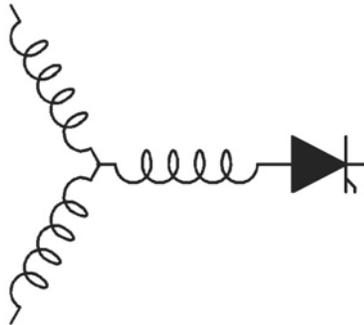
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Fault Interrupting Methods and Topologies for Interior PM Machine Drives

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Fault Interrupting Methods and Topologies for Interior PM Machine Drives

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Abstract—This letter investigates methods to interrupt the phase currents induced when interior permanent magnet (IPM) machine drives suffer short-circuit or uncontrolled generator mode faults. A fault-tolerant silicon switch is proposed in which the antiparallel diode in a reverse-blocking inverter switch is replaced by a thyristor. A reduced-parts-count fault-interrupting topology is also proposed which consists of delta-connected thyristors inserted at the center star point of wye-connected IPM machine stator windings. Control of the proposed reduced-parts-count fault-tolerant drive is discussed and simulation results are presented to verify operation of the proposed topology.

Index Terms—Inverter shutdown, protection, short-circuit fault, uncontrolled generator, variable speed drive.

I. INTRODUCTION

INTERIOR permanent magnet (IPM) synchronous machines are attractive for a variety of applications because of their high power density, wide constant-power speed range, and excellent efficiency. However, their adoption is often hindered by concerns about faults, since the magnets mounted in the spinning rotor produce a source of flux which cannot be turned off at will in the event of a fault.

The IPM motor in a typical six-switch drive system configuration would be subjected to a symmetrical short-circuit type fault if either the upper switches or lower switches are all gated on, or as a result of a dc link short-circuit. During the symmetrical short-circuit, the IPM machine responds as a special type of inside-out induction motor with the permanent magnets providing a balanced excitation while the shorted stator plays the part of a squirrel cage. The result is sustained and possibly damaging phase currents [1]. In the opposite case, where gating signals are removed from all of the switches, an uncontrolled generator (UCG) fault occurs. The spinning motor will then induce currents back to the dc link through the anti-parallel diodes of the inverter if the rotor speed is sufficiently high [2], [3]. In both of these faults, the resulting current asymptotes to the characteristic current of the machine given by Ψ_{mag}/L_d as the speed increases. As a result, machines with large values of Ψ_{mag} can induce fault currents in excess of the rated inverter current.

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This letter investigates fault-interrupting methods for IPM machine drives. It proposes employing a reduced parts count topology in conjunction with a form of phase control to eliminate fault-induced currents. A novel fault-tolerant silicon switch structure is also presented as a potential solution. Simulation results are presented to verify the proposed reduced-parts-count fault-interrupting drive topology.

II. FAULT-INTERRUPTING CIRCUITS

The fundamental difficulty with interrupting and extinguishing the currents and torque due to either short-circuit or UCG type faults lies in the basic inverter structure; there is no capacity to interrupt the motor phase connections, or alternatively, to remove the source of the rotor PM magnetic flux. It is recognized that ordinary wound field synchronous machines or variations of claw pole types of machines can be employed in place of machines with a PM flux. Since their flux can be electrically controlled, their fault protection is strait forward. However, machines without permanent magnets do not meet the efficiency and power density requirements in many applications, including automotive traction and high-power 42-V alternator applications. As a result, necessary fault handling methods to accommodate the presence of the magnets needs to be developed.

One potential solution to changing the source of flux was presented in [4]. The IPM machine in this reference employed movable iron plates sandwiched on both ends of the rotor. Moving the plates closer to the rotor ends diverts some of the flux through the plates so it is not linked to the stator. It is also possible to add a field winding to the stator to adjust the air gap flux [5]. However, both of these solutions require mechanical components and/or additional separate power electronic converters in order to control the flux. As an alternative to these methods of achieving flux control, several integrated electronic methods can be employed as discussed in the following sections.

A. Series Switch Topologies

In [6], a comprehensive survey of fault-tolerant inverter topologies was presented. From these results, it can be concluded that if both a short-circuit fault and a UCG fault are to be interrupted, fuses or back-to-back thyristors must be inserted in series with each of the motor phases. Series thyristors can be considered preferable for the task of interrupting and extinguishing the fault since their operation is controllable.

A recent topology [7] proposed to provide fault tolerance is shown in Fig. 1. In series with each motor phase are back-to-

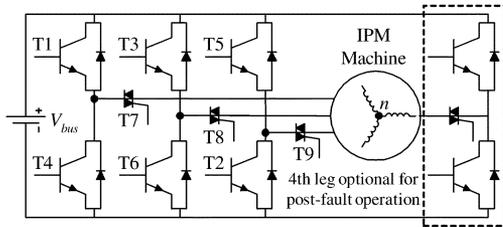


Fig. 1. Fault-tolerant IPM machine-drive configuration.

back connected thyristors. As proposed, the topology provides some capacity for post-fault operation and torque production. If the objective is to interrupt the fault, as in this letter, the addition of the fourth leg to the inverter is not required.

To interrupt either a short-circuit or UCG fault, the circuit works by commanding the back-to-back silicon controlled rectifiers (SCRs) to open upon detection of the fault. As a result, the currents in the three motor phases will be extinguished at the next current-zero crossing. In the case of a UCG fault, which is likely to occur as a result of a control power failure at elevated rotor speeds, the gate pulses would also automatically be removed from the three back-to-back SCRs if they are operated from the same power supply.

B. Fault-Tolerant Switch Topology

For the purpose of fault interruption, the topology of Fig. 1 offers opportunities for simplification. One interesting option is the creation of a fault-tolerant silicon switch. Each inverter switch consists of an IGBT power device in parallel with a discrete diode as shown in Fig. 2(a). As a result, it is possible to take advantage of the physical separation between the two components that make up the switch to develop a silicon switch with improved fault tolerance. This can be achieved by replacing the discrete diode in the combined switch with a thyristor. The proposed fault-tolerant inverter switch is shown in Fig. 2(b). Each of the switches in a conventional voltage-source bridge inverter can be replaced with one of these fault-tolerant switches, eliminating the need for the series back-to-back SCRs in the Fig. 1 topology.

In the fault-tolerant Fig. 2(b) switch, it is a requirement that the insulated gate bipolar transistor (IGBT) must be capable of blocking both forward and reverse voltages. As a result, a diode is required in series with the IGBT if the fault-tolerant switch uses standard IGBT devices that have poor reverse-voltage blocking capabilities. It should be noted that the presence of the series diode does not change the forward conduction losses from the levels achieved by the Fig. 1 topology. However, the adoption of the fault-tolerant inverter switches approximately halves the reverse conduction losses compared to Fig. 1 since the phase current flows through one series device instead of two. Reverse-blocking IGBTs would further reduce the forward conduction losses by eliminating the series diode in Fig. 2(b), but their present characteristics make them best suited for applications with lower switching frequencies (below 1500 Hz) [8].

The proposed fault-tolerant inverter switch has the advantage of being a better candidate for inverter power module packaging than a fault-tolerant inverter topology such as the one in Fig. 1

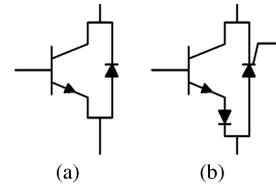


Fig. 2. (a) Standard IGBT-based inverter switch. (b) Proposed fault-tolerant switch topology.

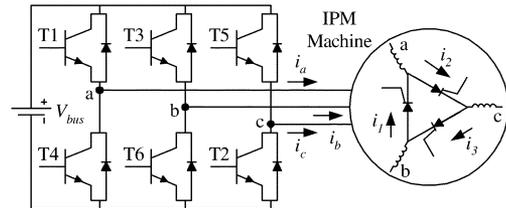


Fig. 3. Proposed reduced parts count fault-tolerant drive configuration.

because of the shared features of the standard and fault-tolerant switch configurations in Fig. 2(a) and (b). However, there are several disadvantages associated with the fault-tolerant switch configuration. First, the thyristors are gated continuously during unfaulded operation. Hence, they must serve as anti-parallel diodes and need to have the appropriate switching characteristics including low reverse-recovery current. Second, the IGBT device (and series diode) is now required to block the maximum reflected voltage of the load which may exceed the standard bus voltage because of high PM machine back-emf voltages fed back to the bus during faulted UCG operation at high rotor speeds. In the topology of Fig. 1, only the back-to-back SCRs are required to have this increased blocking voltage rating, while the IGBT switches are only required to block the normal dc bus voltage. Nevertheless, the fault-tolerant IGBT inverter switch configuration offers lower conduction losses when reverse-blocking IGBT devices can be employed.

C. Reduced-Parts-Count Topology

A fault-tolerant drive configuration with reduced-parts count is shown in Fig. 3 in which thyristors connected in delta are inserted at the star point of the wye-connected stator windings. During normal operation, the thyristors are gated on continuously in order to provide the normal wye-connection of the motor. In the event of a fault, the thyristors are gated off so that the currents will extinguish at the next zero crossing of the delta circuit currents. This circuit has been used in the past for phase control of induction motors [9], [10]. The reduced-parts-count circuit requires only three thyristors, while the circuits of Figs. 1 and 2(b) each require six thyristors.

Fig. 4 shows the relationship between the phase currents and the currents flowing through the delta-connected thyristors using the current polarities defined in Fig. 3. From a ratings standpoint, the delta-connected thyristors must be able to block the peak line-to-line back-emf of the IPM motor, but they actually have a smaller required rms current rating than the main inverter switches, as indicated in Table I. Since the stator currents will flow through either one or two series thyristors in addition to the main inverter switches, the reduced-parts-count

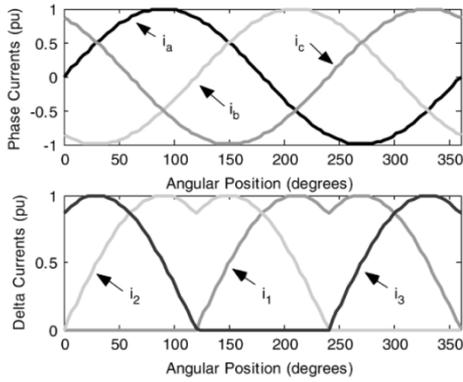


Fig. 4. Relationship between phase currents and delta currents in the Fig. 3 drive configuration.

TABLE I
PROPOSED FAULT TOLERANT DRIVE COMPONENT RATINGS

Component	Component Count	Voltage Rating	Current Rating (A_{peak})	Current Rating (A_{rms})
Main inverter switches	6	V_{bus}	1 pu	0.707 pu
Delta thyristors	3	Peak line-to-line back-emf	1 pu	0.631 pu

topology will have higher conduction losses than either the series-switch topology or fault-tolerant switch topology.

It should be noted that the series switch topology (Fig. 1), fault-tolerant switch topology [Fig. 2(b)], and reduced-parts-count fault-tolerant topology (Fig. 3) only offer methods to interrupt the fault currents. They do not offer a means of limiting the amplitude of the initial fault current surge that accompanies the onset of a serious fault such as a shorted inverter switch.

III. SIMULATION RESULTS

The operation of the proposed reduced-parts-count fault-tolerant drive configuration of Fig. 3 has been investigated via simulation using Simulink with data post-processing in MATLAB.¹ The simulations employed the IPM motor parameters provided in Appendix [11]. The simulation employs ideal inverter switch devices and diodes since the macroscopic behavior of the proposed circuit was the main focus of the investigation. For the simulations, it has been assumed that the system is initially operating in a steady-state faulted condition associated with either a three-phase symmetrical short-circuit or a three-phase UCG condition. As a result, it should be noted that PWM switching behavior of the inverter does not take place during the simulation time duration. The only switches that are being actively gated during the simulation time are the thyristors, whose behavior is being investigated.

Fig. 5 shows simulation results for operation of the Fig. 3 circuit interrupting a symmetrical short-circuit fault at a rotor speed of 1000 r/min. During the initial steady-state short-circuit condition, the motor phase currents have amplitudes given by the machine's characteristic current value of $\Psi_{mag}/L_d = 91 A_{peak}$, and the machine braking torque is small, with a value of approximately 1 Nm.

¹ Simulink and MATLAB are registered trademarks of The MathWorks, Natick, MA.

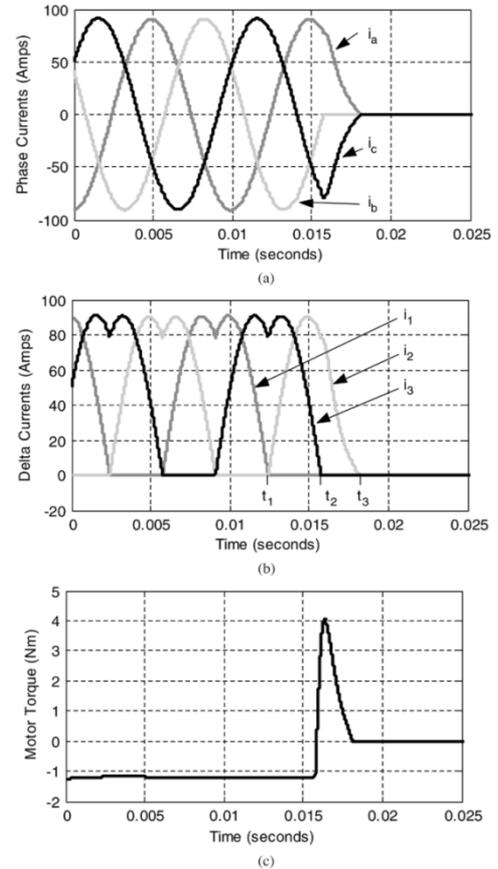


Fig. 5. Simulated results during a three-phase short-circuit interrupting response at $\omega_r = 1000$ r/min. (a) Phase currents. (b) Delta thyristor currents. (c) Machine torque.

Under this three-phase short-circuit condition, the usual dq model of the IPM machine applies. When the system detects that a fault condition is present and gives the command to open the delta-connected thyristors, a delay will occur since each thyristor cannot open and stop conducting until its current has decayed to zero. Due to the inability of the thyristors to open immediately upon command, the command to open the thyristors may occur at any point during the time interval between t_1 and t_2 in Fig. 5(b). At t_2 , a natural zero crossing of a thyristor current occurs so that thyristor will open. At this point, two of the thyristors are open-circuited, while one is still closed, even though it is gated off. With two of the thyristors in an open-circuit state, the IPM motor has current flowing in two of its phases. Since this condition essentially makes one of the motor phases open-circuited (phase b in this case), the usual three-phase model of the IPM motor is no longer applicable, and a model of the system with one-phase open-circuited [12] must be employed. Applying the one-phase open-circuit model after t_2 , the remaining two phase currents decay to zero at t_3 . At t_3 , the current in the remaining two conducting thyristors reach zero and the thyristors revert to their blocking states. With all three of the thyristor switches in open conditions, the wye star connection point of the motor is opened, and the fault currents have been extinguished.

It should be noted that during the time when only two thyristors are conducting, the system experiences a torque pulsation

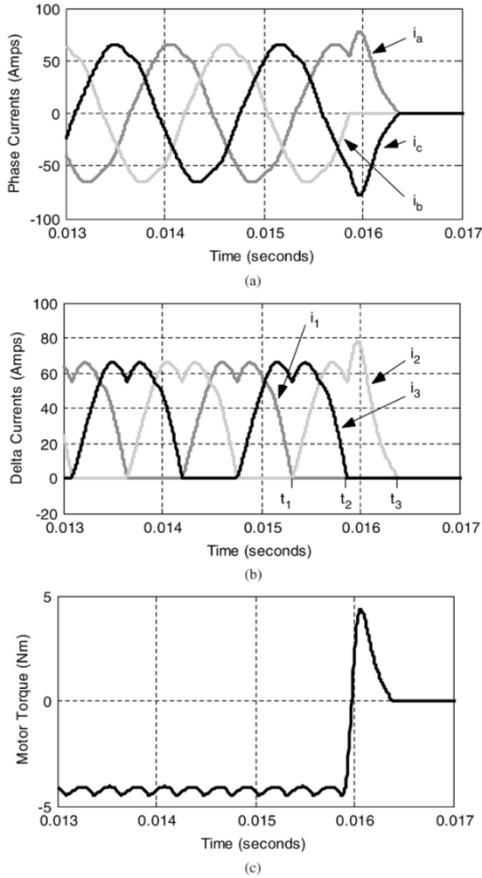


Fig. 6. Simulated results during a three-phase UCG mode interrupting response at $\omega_r = 6000$ r/min. (a) Phase currents. (b) Delta thyristor currents. (c) Machine torque.

of modest amplitude before the torque drops to zero when the thyristors have all opened. This is shown in Fig. 5(c).

Fig. 6 shows the operation of the fault-interrupting drive topology following a three-phase UCG mode fault at 6000 r/min. During the steady-state UCG fault, the braking torque produced is larger than the braking torque for a three-phase symmetrical short-circuit condition. Unlike the symmetrical three-phase short circuit, energy is returned to the dc link through the antiparallel diodes during a UCG mode fault.

From the simulated waveforms, it can be seen that the braking torque produced during the initial steady-state fault is pulsating in nature. This is also apparent in Fig. 6(a) by the appearance of harmonic components in the phase currents. The steady-state currents have a value of approximately $60 A_{\text{peak}}$ at 6000 r/min. At higher speeds, the current amplitudes will asymptote to the characteristic current value of $91 A_{\text{peak}}$. As was the case when interrupting the symmetrical short-circuit fault, the command to interrupt the fault by opening the thyristors can occur as early as t_1 shown in Fig. 6(b), although it will not have an impact until the next thyristor current zero crossing (i_3) that occurs at t_2 . At the t_2 zero current crossing, the corresponding thyristor opens up, creating the transient condition of single-phase open-circuit operation. During this condition between t_2 and t_3 , the currents actually increase in value since they would asymptote to the characteristic current amplitude at a lower speed than for a three-

phase UCG fault. At the next zero-current crossing indicated by t_3 , the remaining two thyristors open and the fault currents are extinguished. During the transition when only two thyristors are conducting, the system experiences a transient torque pulsation as shown in Fig. 6(c).

IV. CONCLUSION

This letter has proposed two methods to interrupt the faulted-phase currents and torque that are produced following both short-circuit and uncontrolled generator-mode faults in an IPM machine drive. A fault-tolerant silicon switch topology has been proposed in which the antiparallel diode of an inverter switch is replaced by a thyristor. By removing the gating for the thyristor, it is possible to extinguish the phase currents in the event of a fault.

A reduced-parts-count fault-interrupting topology that consists of three delta-connected thyristors inserted at the center star-point of a set of three-phase wye-connected stator windings has also been proposed. This topology requires only three thyristors with peak current ratings equal to those of the inverter switches. By opening the thyristors in the event of a fault, it is possible to extinguish the fault currents and torque within 240° of an electrical cycle. Simulation results have been presented verifying operation of the reduced-parts-count interrupting topology.

As a final note, it is important to point out that by employing methods such as those highlighted in this paper to interrupt faults and halt their operation; a key concern about adopting strong permanent magnet synchronous machines in many applications can be eased.

APPENDIX

INTERIOR PM MACHINE PARAMETERS

We have a three-phase, 6-kW-peak at 6000 r/min, 12 pole machine [11] with

$$r_s \approx 0.0103 \Omega \quad \Psi_{\text{mag}} \approx 5.91 \text{ mW}_{\text{rms}} \quad L_d \approx 91.5 \mu\text{H}$$

$$L_{q\text{max}} \approx 305 \mu\text{H} \quad C_1 \approx 0.0058 \frac{\text{H}}{\text{Amp}} \quad C_2 \approx -0.605$$

where the q -axis inductance is approximated as

$$L_q \approx L_{q\text{max}} \text{ or } L_q \approx C_1 |i_q^e|^{C_2}$$

whichever is smaller.

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