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Real-Time Simulation of Matrix Converter Drives

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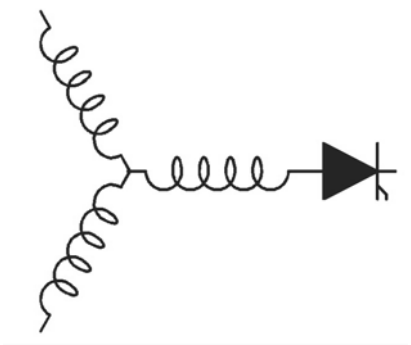

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Keywords

Matrix converters, Real-Time Simulation, Hardware-In-the-Loop Simulation, Interpolation

Abstract

This paper describes a real-time simulator of matrix converter system. The simulated plant is a classical matrix converter with source, input filter and load. The simulator is based on RT-LAB real-time simulation platform that allows for easy model-to-target design from Simulink models. The simulator is designed to accept real IGBT/GTO/MOSFET firing pulses from high performance I/O thus permitting matrix converter controller testing in hardware-in-the-loop (HIL) simulation. The matrix converter model use interpolation methods to have variable-step-solver equivalent precision in the fixed time step scheme required by HIL applications. The paper shows the speed and accuracy of the simulator and highlights the special techniques necessary to simulate kHz-range inverters.

Introduction

Recent years have seen renewed interest on matrix converter based drives. Fig. 1 depicts such a drive configuration. It is composed of 18 IGBTs , MCTs[2] or even Reverse Blocking IGBTs (RB-IGBTs)[3], grouped in pairs in series- parallel configuration with diodes (except in the case of RB-IGBT). An input filter and voltage clamp circuit complete the circuit. This drive topology has some interesting characteristics of it own. It has intrinsic power regeneration capability. It can have smaller mounting place than conventional AC-AC converters because braking resistor nor large electrolytic capacitor are not necessary. It has low total harmonics of input current with high efficiency and power factor. Because the matrix converter drive also has no large DC-bus capacitor (usually electrolytic) so it has longer lifetime and is more reliable.

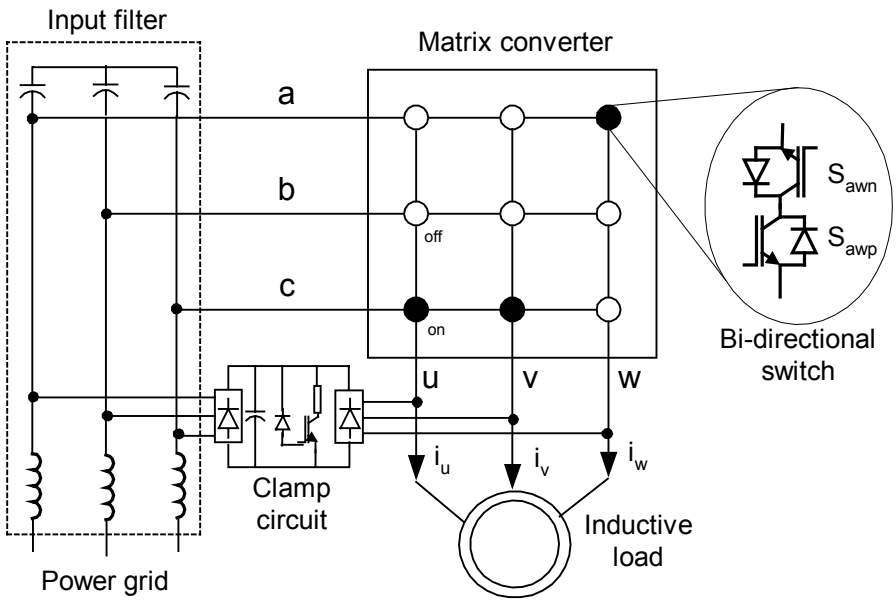

Fig. 1. Matrix converter with its input filter, load and clamp circuit.

Real matrix converter implementations present some problems though. One of these problems is the complex firing scheme of the topology. This scheme must avoid at the same time short-circuiting IGBTs pair while avoiding any load open-circuit conditions. At the same time, this firing must be synchronized in some way to the AC input voltage. The required Phase-Lock Loops are more complex then simple AC diode rectification for example.

The complex control schemes of the matrix converter demands, in return, higher tests requirements on the candidate controllers. One of modern way of testing controllers before final integration on actual apparatus is to make Hardware-In-the-Loop (HIL) real-time simulation tests. This testing methodology basically consists on running the actual controller connected to a real-time simulation of the device or plant it is supposed to control. Model-based simulation software like Simulink or SystemBuild is used in conjunction with automatic code-generation software to produce the plant executable. The connection between the controller and the real-time simulation is made through I/O. Using HIL simulation permits easier integration of the plant and controller part of the matrix converter by allowing extensive test capability of the controller without any risk of damages to the high power part of the devices or scientific personnel.

While HIL simulation is a well-established testing technique in the classic automotive industry for example, it is somewhat an emerging technology in the field of electrical drives and power systems. Indeed, the HIL plant simulation technique is more difficult to realize for electrical systems for several reasons. For example, electrical systems usually have a lot of working modes caused by switches. Electrical systems also tend to be “stiff” by nature, requiring very small time steps or variable-step solvers to achieve convergence and/or accuracy. An important difficulty in simulating a matrix converter or other modern drives comes from its high commutation frequency. Basic HIL sampling of the matrix converter gate signals can then result in poor accuracy at current simulator technology of 10 microseconds time step.

Interpolation and HIL simulation of Electric Drives

A real-time simulator runs at constant sampling rate and therefore, *a priori*, samples any signals from the I/O at this rate and time resolution. This has important impacts when sampling IGBT gate signals with switching frequency high relative to the sampling rate.

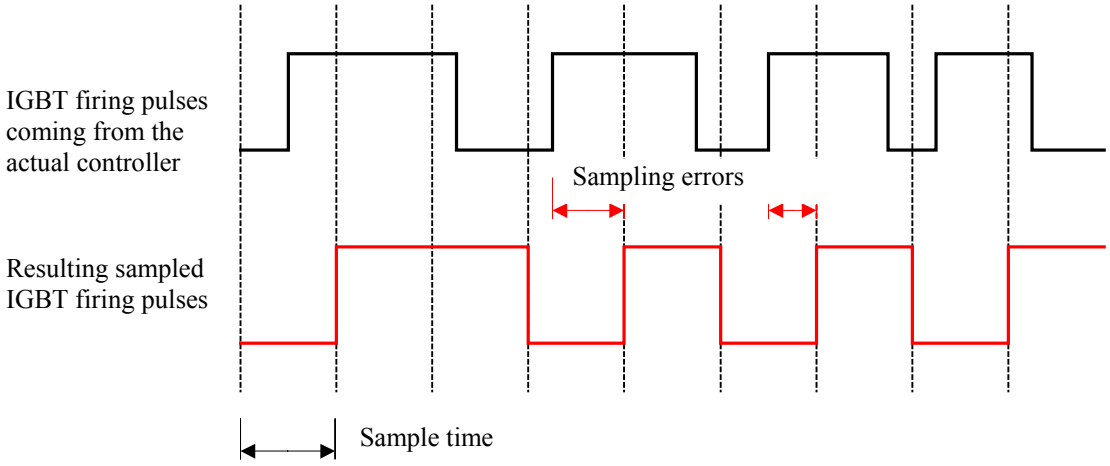

Fig. 2. Sampling errors made with standard I/O

These IGBT pulses are somewhat very similar in shape to the actual voltage fed to the load. If the load is a machine for example, integration of the voltage is made to compute machine fluxes and accuracy can become very bad. These errors occur at each transition and one can deduct that they get worse when the ratio of sample time (Ts) to carrier period (Tpwm) becomes higher. Typical ratios necessary to have good accuracy on motor drive (without special techniques like interpolation) are lower than 1/100. For a 100 kW converters switched at 10 kHz and typical real-time simulator of 10 microseconds, this ratio is 1/10 and lead to inaccurate results.

The solution to this problem is to use interpolation techniques. In HIL simulation, this technique is two-fold.

- First of all, the IGBT gate signals must be sampled by high frequency counter cards (like Opal-RT FPGA card) so their transition timings are captured with higher definition than the simulator sampling frequency (typically 10 ns).
- Secondly, this accurate timing information must be use to feed the IGBT inverter load with compensated voltage-sample time products so the integration by the load of this voltage results in accurate flux or current. Opal-RT Time Stamped Bridges has these features and where demonstrated to be very effective for a variety of drives[5][6][7][8].

A similar problematic exist in fully numerical real-time simulation where controllers and plant are simulated. In this case, the IGBT gate signals generation must be made with equivalent sub-microseconds resolution despites the fixed-time simulation. This requires the use of RT-Events, a Simulink blockset designed for interpolation of in-step events like the sinus-triangular comparisons occurring in PWM generation.

The RT-LAB real-time simulator

The RT-LAB simulator is designed to make the real-time simulation of Simulink or SystemBuild models on clusters of standard Pentium-based multi-CPU PC.

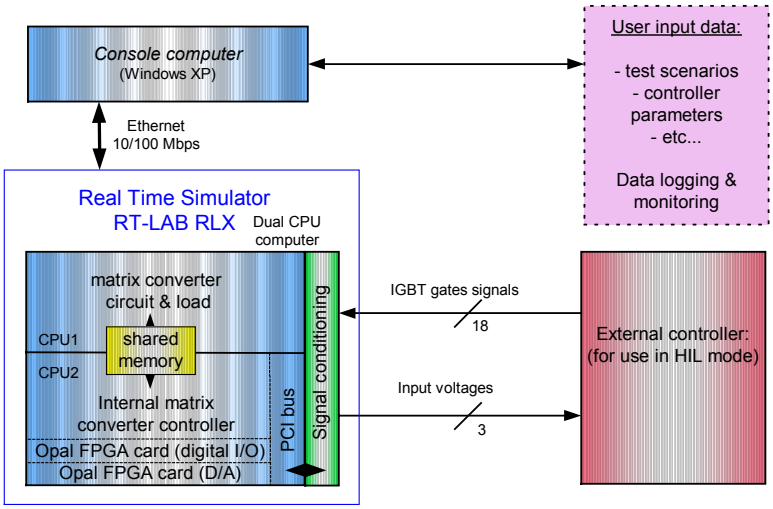

Fig. 3. Structure of the RT-LAB real-time simulator

PC-based systems with Dual or Quad-Pentium processors are commercially available for this purpose. RT-LAB build parallel tasks from the original Simulink model and run them on each CPU of the multi-CPU computer. Data are exchanged though shared-memory that has ultra-low latency in the same order of the CPU system memory and thus permits the parallel simulation of electrical systems at time step below 10 microseconds. This is shown in Fig. 3for the matrix converter application. The figure shows a typical task separation on a dual-CPU computer: one CPU holds the plant model and I/O interface while the other CPU holds numerical version of the controllers.

Larger HIL simulation requirement can be fulfill by using RT-LAB on PC cluster connected through external communication links. To achieve this, RT-LAB uses an FPGA-based proprietary communication link called SignalWire™ capable to deliver up to 1.25 Gbit/s transfer rates, with a latency of 200 ns or InfiniBand.

The same FPGA board implements the I/O functionalities of the RT-LAB simulator for Hardware-In-the-Loop testing of electrical systems. The RT-LAB platform is configured to be used with a supplied library of Simulink blocks that allow the user to implement the DIO, event capture, event generation, and PWM I/O capabilities, all with 10 ns resolution, in the real-time model without coding.

A real-time matrix converter model

The proposed matrix converter model was designed with the following requirements:

1- Accurate at typical time simulator time step (10 μs) and typical matrix converter switching frequency (10 kHz)

2- Able to take into account multiple dead time effects occurring in matrix converters

3- Detect individual IGBT firing faults like load open-circuit and source short-circuits

4- Be independent of the commutation technique (ex: dependency on current direction)

5- Be able to take into account IGBT voltage offset and resistive voltage drops.

6- Be able to take into account IGBT rise-fall times with a dependency on IGBT currents.

The requirements 1 and 2 are somewhat linked. Take for example the switching actions necessary to change voltage of leg *u* from *Va* to *Vb* in a current commutation scheme proposed in [2].

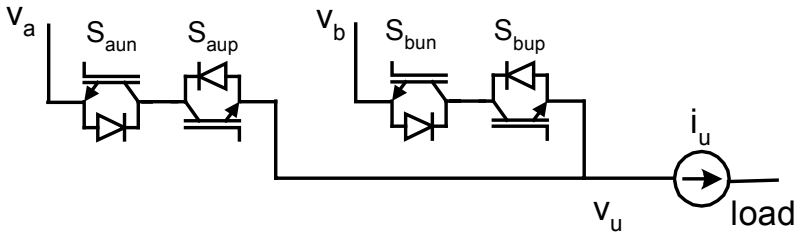

Fig. 4. Two pairs of switches of the matrix converter

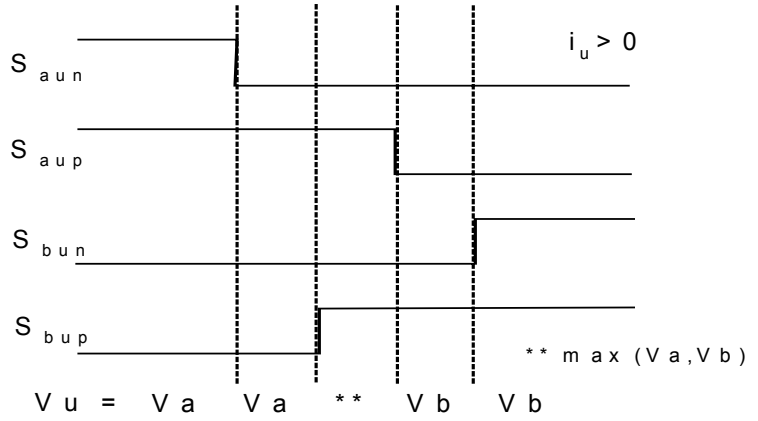

Fig. 5. Switching sequence to change the voltage of one phase of the load

The sequence of Fig. 5 has 5 intervals of a typical duration between 0 and 5 μs (some intervals can be null). The fact is that all these intervals can occurs during a single time step of the simulator! The problems can grow if a gate is allowed to turn ON and OFF in the same time step (which is often the case).

The technique use to accurately simulate such a high number of switching actions per time step consists on the following steps:

1- Sampling all the gate signals with high resolution (ex: FPGA counting card)

2- Apply internally any transportation delay (with current dependence if any). This is equivalent to shifting the pulse edges in time (Requirement 6)

3- Check for any source short-circuit or load open circuit conditions (Requirement 3). For example, the sequence of Fig. 5 would generate a load open-circuit error if the load current were reversed.

4- Compute the load voltage (with IGBT losses, Requirement 5) of all intervals during a simulator time step.

5- Send the load the average of all voltage intervals during the simulator sample time and send the load current to the input stage of the matrix converter (for input filter capacitor integral equation).

The model was programmed in a MATLAB S-function and compiled for usage in Real-Time Workshop and RT-LAB. For each trio of switch pairs connected to one phase of the load, extensive *case{}* "C" statements are used to determine the voltage of all intervals depending on the gate levels and transition timings, the voltage amplitude of the 3 input voltage sources and the load current.

The proposed matrix converter model cannot be used to simulate load shutdown because it assumes constant conduction of the load

Validation of the proposed model

Extensive tests were conducted to validate the matrix converter model. Validation is first made on one trio of IGBT pairs connected to one phase of a grounded RL-load. Final tests are made on the complete matrix converter attached to a source and input filter. All tests were made in open-loop conditions where the user fixes the modulation index and output frequency.

Matrix converter modulation scheme

The matrix converter tests were made using the space vector pulse width modulation (SVPWM) with voltage commutation. The modulation technique is described in details in [1]. The technique models the matrix converter as an AC/DC/AC converter with virtual DC-link. The virtual AC rectifier is controlled so that the input phase with the highest absolute voltage is connected to the virtual DC-link (6 different sectors) at all time while the opposite input leg alternates between the other input phases (2 portions). During each portion, SVPWM is applied to the virtual inverter part of the matrix.

Matrix converter IGBT gate signal generation

Simulating at 10 μs a matrix converter is somewhat a challenge but generating the IGBT pulse at the same rate in Simulink is even more difficult because it involves a lot of signal comparison, similar to carrier-modulation index in normal PWM, that have more than 1 zero crossing during a single time step for the modulation method used in this paper. Therefore, the following methodology was used to generate the IGBT pulses:

1- A variable step simulation of the firing scheme is first made with dead time added only to the modulating switches in each sector. See [1] for details

2- The IGBT pulse recording from the variable step simulation is then translated to a format compatible with fixed step simulation (OPHSDIO format)

3- The real-time simulation of the Time Stamped Matrix Converter model with the recorded OPSHDIO format of switch gating is then made.

The OPHSDIO fixed step event format is format developed by Opal-RT to send or receive discrete event by a high frequency I/O card. It is basically a record of events occurring at each time step. As seen in Fig. 6, the input digital signal is transformed in two series of size-2 vectors. The first of these vectors records the digital value just after each transition. The second vector records the elapse time of each event since the beginning of the time step. Default values of –1 and Ts are used if there is less than 2 transitions during the time step.

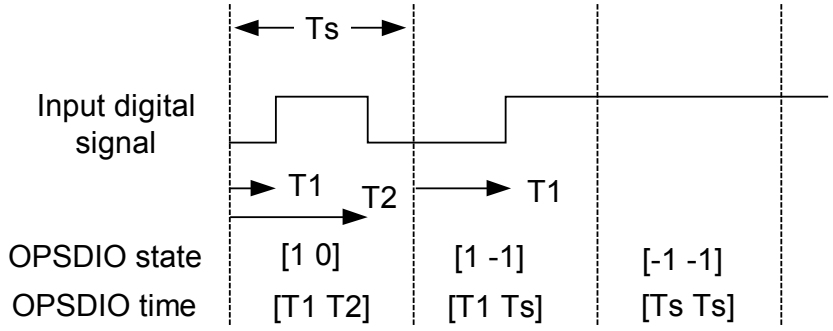

Fig. 6. OPHSDIO event format used in the matrix converter model

The proposed matrix converter model use this format to input the IGBT gate signals and is therefore ready fed from gate signals coming from I/O in HIL applications.

Test1: Ideal (no dead time) IGBT pair switching and effect of interpolation

Test #1 highlights the effect of interpolation in the matrix converter running with high sample time to carrier period ratio. To simplify the overall analysis, the test is conducted on one trio of IGBT pairs as depicted in Fig. 7. An R-L load connects the *u* output phase to ground. The resulting load currents therefore have a source 3rd harmonic component (180 Hz for the source frequency used in all the tests) that is not present in normal usage of the model on ungrounded loads.

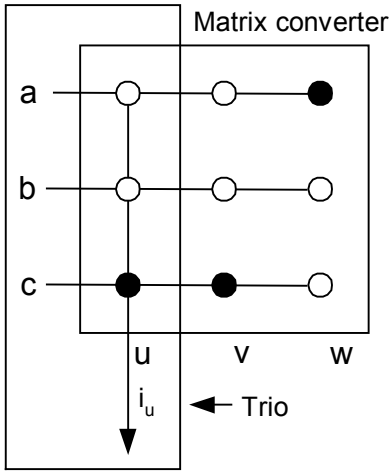

Fig. 7. The trio of IGBT pairs used for tests 1 & 2

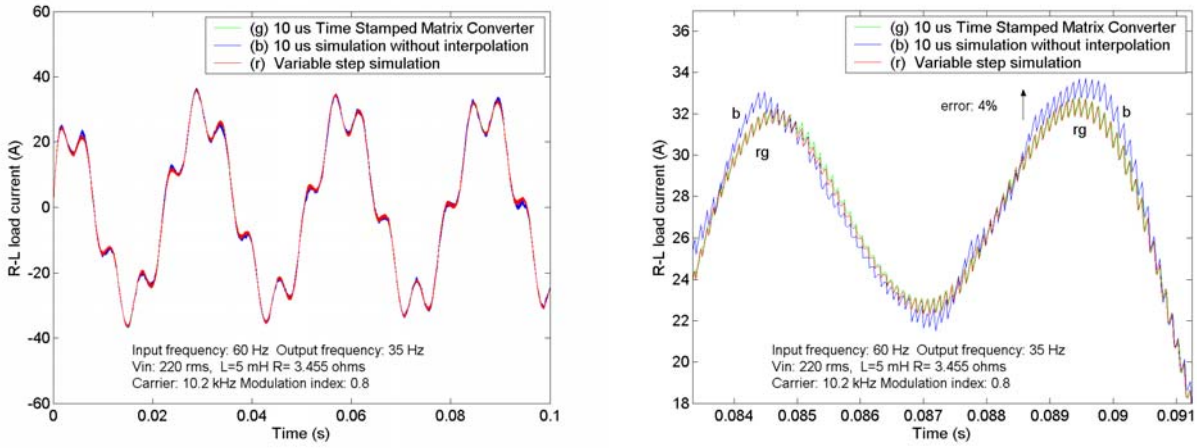

Fig. 8. Load current with details (right plot). No dead time

Fig. 8 reveals that the 10 µs Time Stamped Matrix Converter (model with interpolation, curve *g*) is very accurate when compared to a simulation made with a variable step solver (curve *r*). When interpolation is disabled this results in 4 % errors in this case.

Test 2: Simulation with dead time

In test #2, the proposed real-time matrix converter model is tested with dead time applied to its gating signals and the results are shown in Fig. 9. For this test, reference curves where obtained using SimPowerSystems blockset from Simulink with discretisation at a very small time step of 0.2 µs. The results shows that the Time Stamped Matrix Converter (TMSM) and SimPowerSystems models match very closely with dead times of 0 (curves *r* and *g*) and 2 µs (curves *m* and *o*). The TMSM was also run with a dead time of 1 µs (curve *b*) to highlight the gradual load current drop when dead time is increased.

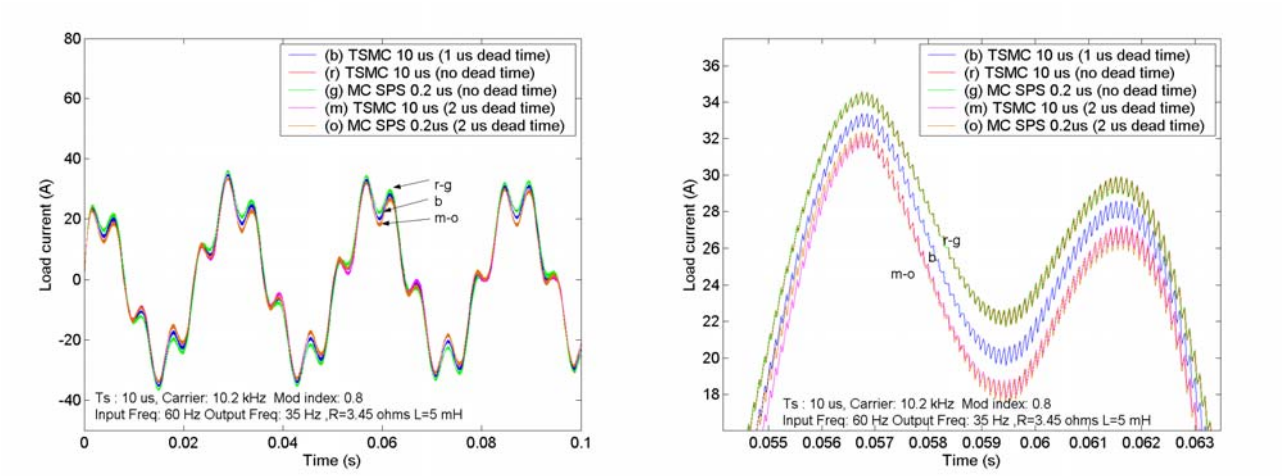

Fig. 9. Load current with deadtime

Test 3: Real time simulation of the complete matrix converter

The complete Time Stamped Matrix Converter model is tested in this section connected to a 3-phase load and input filter. Test parameters are put forward in Table 1. The input filter has a resonant frequency around 2 kHz.

Table I: Time Stamped Matrix Converter test parameters

Sample Time	10 µs	Load resistance Load inductance	3.45 Ω 5 mH
Carrier Frequency	8 kHz	Input filter inductance Input filter capacitance	0.2 mH 30 µF
Modulation index	0.8	Dead time	0 - 2 µs
Input Frequency	60 Hz	Output Frequency	20 Hz

Fig. 10 shows the real time simulation results of the Time Stamped Matrix Converter with load and input filter. Left figure shows the load current with a 2 µs dead time and no dead time. Right figure shows the filter input current (going through the filter inductance) for the same dead times. The results shows a load current drop caused by the dead time. It is interesting to note that the load current has no distortion caused by the dead time as it can normally be observed for standard AC inverters (short stall at zero current crossing)[5][8].

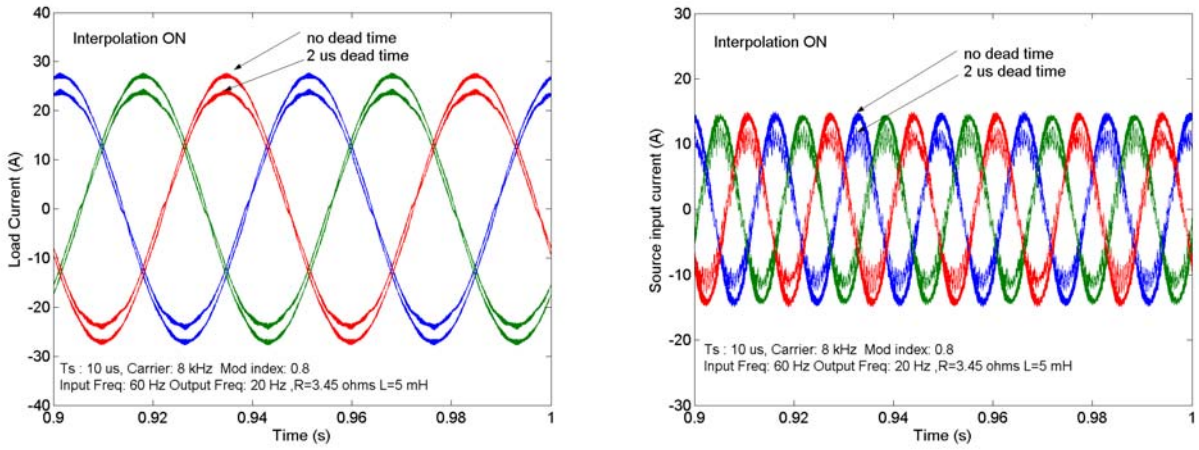

Fig. 10. Load current and filter input current with TSMC simulation at 10 μs time step

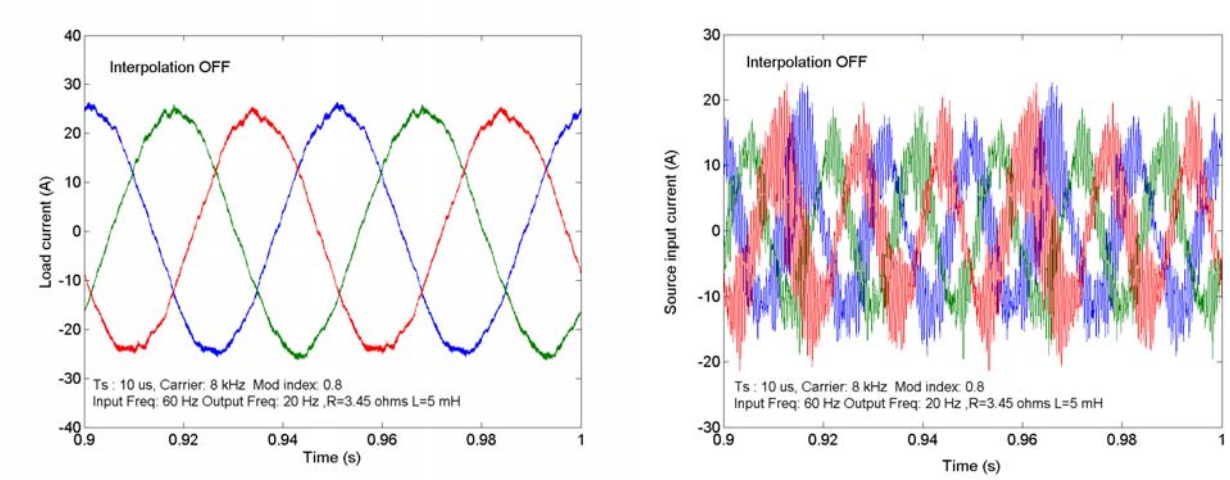

Fig. 11. Load and input filter current simulation at 10 μs time step with interpolation disabled

The same simulation made without interpolation was carried out and the results are shown in Fig. 11. It shows increased noise level, especially for the input filter current. This last curves implies that interpolation techniques are very important if the matrix converter where to be connected to a weak network.

Test #4: Computational Speed

The complete matrix converter model with voltage sources, input filter, R-L load as a calculation time of 6 μs on a Xeon 2.4 GHz PC running RT-LAB 7.1.4. The model did not include protection clamp circuits.

Conclusion

This paper has presented a matrix converter model for usage in real time applications like HIL validation of matrix converter controllers. The model was compared against commercial simulation software for its accuracy and was demonstrated to be computational fast enough to run in real time. The matrix converter model can help make controller integration with the matrix converter plant safer and more progressive. It also permits testing the controller for parameters that could be dangerous for the real plant.

The matrix converter model was demonstrated to be very accurate in fixed step simulation even with dead time effect much smaller than the sample time. It was also demonstrated that interpolation methods were critical to obtain good accuracy, especially at the source side.

An interesting finding of the paper is that the matrix converter modulation scheme used in the paper did not seem to cause distortion due to dead times. This finding shall be investigated further.

Finally, although the proposed matrix converter is already programmed to include IGBT turn-on and turn-off delay with current dependency, thorough validation of this characteristic remains to be done and presented.

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