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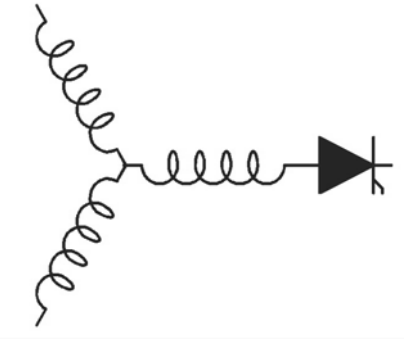
K. Lee, T. M. Jahns, T. A. Lipo,
G. Venkataramanan, W. E Berkopek*

University of Wisconsin – Madison
1415 Engineering Dr.
Madison, WI 53706 USA

*Eaton
4201 North 27th St.
Milwaukee, WI 53216 USA



Wisconsin
Electric
Machines &
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Electronics
Consortium

University of Wisconsin-Madison
College of Engineering
Wisconsin Power Electronics Research Center
2559D Engineering Hall
1415 Engineering Drive
Madison WI 53706-1691

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Impact of Input Voltage Sag and Unbalance on DC Link Inductor and Capacitor Stress in Adjustable Speed Drives

Kevin Lee†
KevinLee@eaton.com

Thomas M. Jahns*
jahns@engr.wisc.edu

Thomas A. Lipo*
lipo@engr.wisc.edu

Giri Venkataramanan*
giri@engr.wisc.edu

William E. Berkopec†
WilliamEBerkopec@eaton.com

† Eaton
4201 North 27th St.
Milwaukee, WI 53216 USA

*University of Wisconsin – Madison
1415 Engineering Dr.
Madison, WI 53706 USA

***Abstract* – This paper investigates the impact of input voltage unbalance and sags on stresses in the dc bus choke inductor and dc bus electrolytic capacitors of adjustable-speed drives (ASDs). These stresses are primarily attributable to the rectifier's transition into single-phase operation, giving rise to low-order harmonic voltages (120 Hz, 240 Hz, etc.) that are applied to the dc link filter components. These harmonics elevate the ac flux densities in the dc choke core material significantly above values experienced during normal balanced excitation conditions, causing additional core losses and potential magnetic saturation of the core. It is shown that the effects of voltage unbalances and sags on the dc link capacitor lifetime will be the same when either line inductors or a dc link choke inductor are used if the dc choke inductance value is twice the value of the line inductance. Simulations and experimental tests are used to verify the accuracy of predictions provided by closed-form analysis and simulation for a 5 hp ASD system.**

I. INTRODUCTION

A variety of power quality problems exist today that include harmonic distortion, frequency variation, noise, transient voltage spikes, outages, voltage surges and sags. Power quality problems induced in adjustable-speed drives (ASDs) have been reported in several papers and surveys [1-5]. These studies have shown that voltage sags and longer-term voltage unbalances account for a major fraction of today's power quality problems.

There are three major negative effects that unbalanced input voltages can have on ASDs that are highlighted in Fig. 1. First, unbalanced voltages can create significant input current unbalances that stress the diode bridge rectifiers and input protective devices such as fuses, contactors and circuit breakers [6,7,8]. Second, unbalanced voltages typically inject a second harmonic voltage component onto the dc bus voltage (120 Hz for 60 Hz system) that increases the electrical stresses on the dc bus choke inductor (if used) and the dc link electrolytic capacitors, potentially shortening the capacitor lifetime [9]. Third, voltage unbalances can give rise to significant amounts of 120 Hz ripple torque in the ASD induction machine, increasing the mechanical and thermal stresses [10,11].

Attention in this paper is focused on general-purpose ASDs that consist of a three-phase rectifier input stage, a PWM inverter stage that delivers constant Volts-per-Hertz excitation,

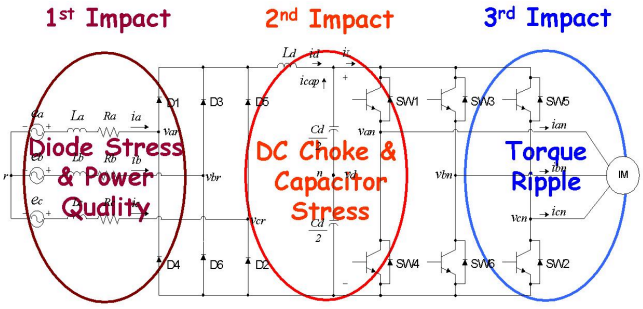

Figure 1. Major negative effects of input voltage sags and unbalances on ASD operation.

and a dc link that includes an inductor. Many modern ASDs use a dc bus inductor (choke) for a combination of reasons that include reduction of input line current harmonics in order to meet IEEE 519 limits, improvement of the input power factor, reduction of ac ripple on the dc bus, and elimination of dc bus nuisance overvoltage tripping [12,13]. Electrolytic capacitors are used to filter the rectifier voltage ripple and act as a low impedance path for ripple currents generated by the rectifier and PWM inverter stages. In addition, the capacitors provide ride-through energy storage capacity on the dc bus.

In most cases, the dc choke is designed to absorb 360 Hz harmonic voltage components when the input voltages are balanced. Under realistic operating scenarios that include a moderate input voltage unbalance as described in this paper, a significant amount of ac flux is added that stresses the magnetic core material due to the low-frequency harmonic voltage components at 120 Hz, 240 Hz, etc. This condition will generate additional core losses, as well as potentially causing the iron core to magnetically saturate, resulting in significant drops in the effective inductance value. The consequences include high peak input currents that can overstress the front-end bridge rectifiers to cause premature failures, as well as inducing elevated ripple current in the dc bus capacitors.

The lifetime of the dc bus capacitors is principally determined by their core temperatures. Both rectifier and inverter ripple currents contribute to the capacitor temperature rise. The capacitor heating effects due to the rectifier ripple currents associated with balanced input voltage conditions has been reported in [14,15]. Similarly, ripple current effects

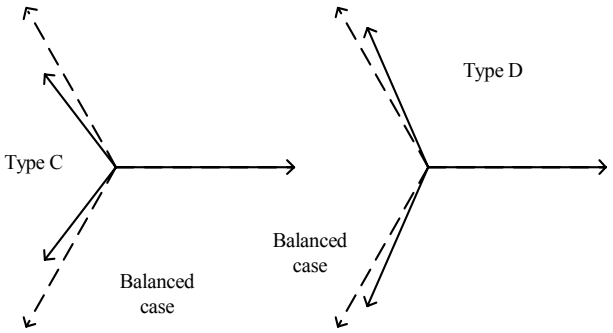

Figure 2. Phasor diagrams of Types C and D three-phase input voltage unbalances.

caused by normal pulse-width modulation (PWM) operation of inverters are discussed in [16,17]. However, a comprehensive analysis of the stresses induced in the dc bus electrolytic capacitors caused by input voltage unbalance and sag conditions in ASD systems with a dc bus choke inductor does not exist in the literature. Results presented in this paper complement and extend work presented previously for ASD systems with ac line inductors [9].

The purpose of this paper is to investigate the impact of input voltage unbalance and sag conditions on stresses in the dc bus choke inductor and electrolytic capacitors in ASDs. Closed-form equations are developed to evaluate the dc bus dynamics under these unbalanced input conditions with a finite dc bus inductance and capacitance. The harmonic spectrum of the dc bus choke inductor current and the resulting inductor flux density characteristics are evaluated. Ripple current caused by both the rectifier and the inverter space vector pulse-width modulation (SVPWM) are also included in the capacitor lifetime analysis. Capacitor heating is calculated incorporating the frequency dependence of the capacitor equivalent series resistance (ESR).

The analytical tools presented in this paper can be used to select an appropriate dc bus choke inductor and capacitors for applications subjected to input voltage unbalance and sag conditions. A 5 hp ASD system is used to verify the accuracy and effectiveness of the analysis by comparing performance predictions to simulation and experimental results. In addition, a systematic methodology for evaluating the capacitor lifetime in practical ASD systems is presented.

II. Summary of ASD Analytical Model for Sags

Fig. 2 illustrates the three-phase voltage phasors under unbalanced conditions that have been defined as Type C and Type D sags [2]. Both of these sag conditions are distinguished by two phase voltage phasors that deviate symmetrically in both amplitude and phase from their balanced conditions. Attention in this paper is focused on investigating the effects of Type C unbalance on ASD operation, although the presented analytical method can be extended to study the effect of Type D sags as well.

The amount of voltage unbalance can be quantified using percentages. For reference, the standard IEEE definition of

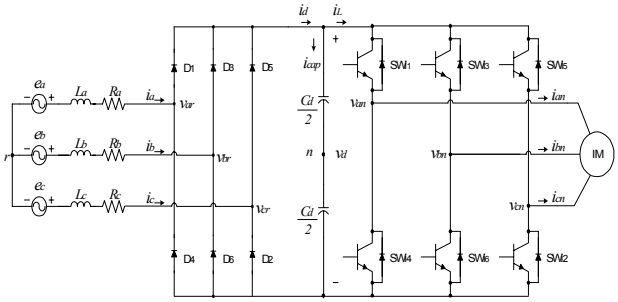

Figure 3: Induction machine ASD power circuit diagram including three identical input line inductors L_a, L_b, and L_c.

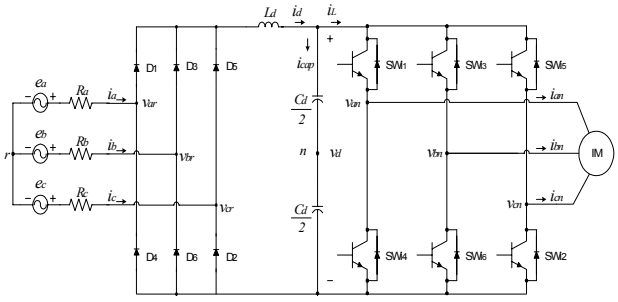

Figure 4: Induction machine ASD power circuit diagram including a dc link choke inductor L_d.

phase-voltage unbalance in three-phase systems [18] is expressed as:

$$unbalance\% = \frac{|V_{avg} - V_{\Phi}|}{V_{avg}} \quad (1)$$

$$V_{avg} = \frac{V_a + V_b + V_c}{3} \quad (2)$$

where V_{Φ} is the amplitude of one of the three input phase rms voltages (V_a ,V_b ,V_c) that produces the largest deviation from the average voltage.

Figs. 3 and 4 illustrate two widely used ASD configurations. Three-phase ac line voltages are fed to a three-phase rectifier (D_1-D_6) bridge. The input line impedance values are assumed to be balanced, each consisting of a series resistance R_a ($=R_b=R_c$) and line inductance L_a($=L_b=L_c$) in Fig. 3. The line inductors are eliminated in Fig. 4 in favor of a single dc link inductor L_d. The dc bus voltage is buffered by dc bus capacitance C_d.

The PWM inverter consists of six IGBT switches (SW_1 - SW_6) and anti-parallel diodes. PWM control of these switches is used to synthesize variable-frequency, variable-amplitude ac voltage waveforms that are delivered to the induction machine following a constant Volts-per-Hertz algorithm.

It has been shown previously [9,10] that the input rectifier stage of the ASD configuration using ac line inductors (Fig. 3) can easily slip into single-phase operation during input voltage sag or unbalance conditions. Analysis of the ASD configuration using a dc link choke inductor (Fig. 4) reveals that this topology behaves almost identically to the line inductor configuration during Type C unbalance conditions.

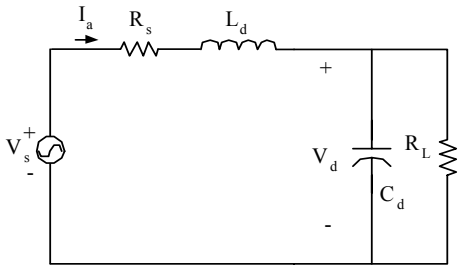

Figure 5. Equivalent circuit during single-phase operation.

The equivalent circuit of the ASD input stage with the dc link inductor under such single-phase excitation conditions is shown in Fig. 5 [11]. This circuit is almost identical to the corresponding circuit for the ASD with line inductors [10], except that the dc bus choke inductor L_d that appears in Fig. 5 is replaced by two line inductors L_a in series. The resistance R_L that appears in this circuit is the simplified representation of the inverter and motor load.

The closed-form solution of the second-order *RLC* circuit in Fig. 5 leads to the following time-domain expression for the dc bus voltage $V_d(t)$:

$$V_d(t) = \begin{cases} V_{pk}\left[A\cos[\Omega\,(t - t_x)] + N\cos(\omega t)\right] & t_{in} < t < t_{ex} \\ V_d(t_{ex}) \cdot e^{-\frac{t-t_{ex}}{C_{dc} R_L}} & t_{ex} < t < t_{in} + \frac{T}{2} \end{cases} \quad (3)$$

where t_{in} is the inception time of the discontinuous bus current i_d, t_{ex} is the current extinction time, and T is the period of the ac excitation frequency (e.g., 1/60 = 16.7 ms for 60 Hz excitation). The other coefficient definitions are provided in the Appendix, with the inductance L_s in these definitions taking on the following values for the two ASD configurations:

$$L_s = 2\,L_a \quad \text{for ASD with line inductors (Fig. 3)} \quad (4)$$

$$L_s = L_d \quad \text{for ASD with dc link inductor (Fig. 4)} \quad (5)$$

The effects of finite values of input line inductance or dc link inductance on inductor stress and dc bus capacitor lifetime can be evaluated using this closed-form bus voltage expression.

III. DC Bus Inductor Stress Evaluation and Experimental Results

Several of the benefits of a dc bus choke under balanced input voltage conditions were summarized in the Section I introduction. However, the presence of line voltage sag and unbalance conditions causes the dc choke inductor to be exposed to 120 Hz and its harmonics in addition to the 360 Hz components it experiences under normal balanced operating conditions. The dc choke inductor offers protection against input current surges, but it cannot protect the rectifier bridge converter in Fig. 4 from line voltage spikes because of its location. As a result, the diode converter bridge is directly

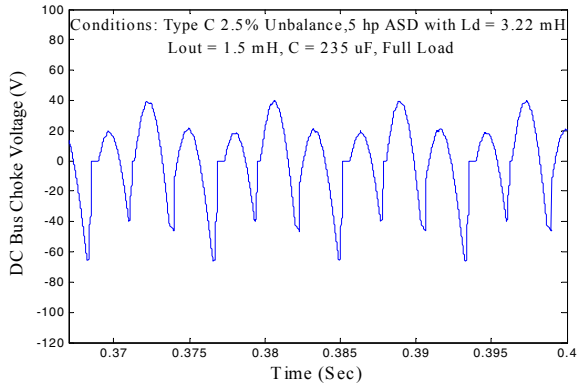

Figure 6. Simulated voltage waveform across the dc bus choke inductor during Type C sag with 2.5% voltage unbalance.

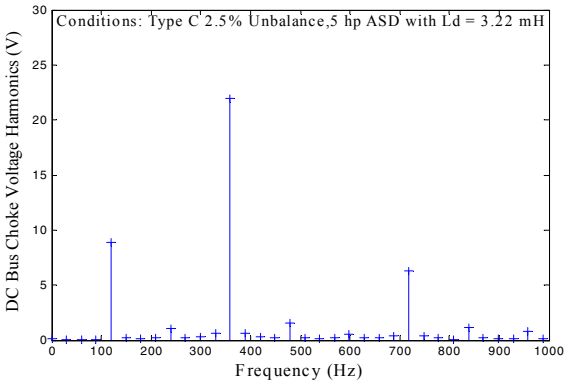

Figure 7. Harmonic spectrum of the simulated dc bus choke voltage waveform during Type C sag with 2.5% voltage unbalance.

exposed to the prevailing line conditions in the absence of additional external line reactor components.

For a 5 hp ASD system operating with a 2.5% Type C input voltage unbalance, the dc bus choke inductor develops a high ac voltage across it as shown in the simulated voltage waveform in Fig. 6. The harmonic spectrum of this voltage waveform is shown in Fig. 7, highlighting the significant component at 120 Hz in addition to the expected 360 Hz component. (Key parameters for this analysis are: R_a = 10 mΩ, L_d = 3.22 mH, C_d = 235 μF, full load).

The magnetic flux density in the dc bus choke inductor consists of a dc component contributed by the dc current and ac components produced by the ac voltage components illustrated above in Fig. 6. The governing equations are [20]:

$$B_{dc} = \frac{3.19 \cdot N \cdot I_{dc}}{0.85 \cdot L_g} \quad (6)$$

$$B_h = \frac{E_h \times 10^8}{4.44 \cdot f_h \cdot A_c \cdot N \cdot SF} \quad (7)$$

$$B_{total} = B_{dc} + \sum_n B_h \quad (8)$$

where B_{dc} is the dc flux density [T], B_h is the peak ac flux density contributed by one of the voltage harmonics [T],

TABLE I. SIMULATED AND MEASURED VOLTAGE ACROSS THE DC BUS CHOKE

Conditions: 5 hp ASD at Full Load with Type C Sag at 2.5% Unbalance

DC Choke Inductor 3.22 mH, 9 A	*120 Hz Component*	*360 Hz Component*
Voltage -Simulation	8.9 Vrms	21.9 Vrms
Voltage -Measurement	9.3 Vrms	21.3 Vrms
Magnetic Flux Linkage, λ - Simulation	11.8 mWb-rms	9.7 mWb-rms

TABLE II. 120 HZ AND 360 HZ CORE LOSS COMPARISONS BASED ON FIGURE 8 DATA.

Flux Density (Gauss)	*120 Hz Core Loss (mW/cm^3)*	*360 Hz Core Loss (mW/cm^3)*	*Ratio of 120Hz/360Hz*
1000	1	~ 3.5	28.6%
2000	~ 4.2	~ 14	30.0%
3000	~ 9	~ 28	32.1%

B_{total} is the peak core flux density [T], N is the number of series winding turns, I_{dc} is the dc current [A], L_g is the air gap length [mm], E_h is the amplitude of one of the ac harmonic voltage components [Vrms], f_h is the harmonic frequency [Hz], A_c is the core sectional area [mm2], and SF is the core stacking factor.

Because of the cost pressures in industry, the dc choke inductor is typically designed to handle only the 360 Hz ripple component expected under balanced input voltage excitation conditions. This analysis shows that the dc bus voltage components at 120 Hz and its harmonics in Figs. 6 and 7 combine to increase the peak ac flux density significantly compared to operation with balanced excitation.

Table I captures the largest measured voltage harmonics that appear across the dc bus choke inductor used in this study. It should be noted that the 120 Hz component does not exist in the balanced excitation case, while the 360 Hz component remains approximately the same in both the balanced and unbalanced cases (i.e., the 360 Hz voltage component is 21.3 Vrms for balanced excitation). The calculated values of the low-frequency voltage components (via simulation) agree very well with the measured values from the experimental equipment (see Sec. V) tested under the same conditions.

The last row in Table I provides the calculated values of the resulting magnetic flux linkage contributed by the 120 and 360 Hz components, having an amplitude V/ω. It is notable that, after including the effects of the difference in frequency, the amplitude of the 120 Hz flux linkage that appears under voltage sag or unbalance conditions exceeds the amplitude of the 360 Hz component under balanced excitation conditions.

It is impossible to state whether the presence of the additional harmonic components in the magnetic flux linkage will cause the choke inductor to enter magnetic saturation without specifying the details of the inductor design. However, it can be generally stated that inductors that are designed more aggressively to minimize their cost by targeting only balanced excitation conditions will be the most vulnerable to saturation under unbalanced voltage conditions.

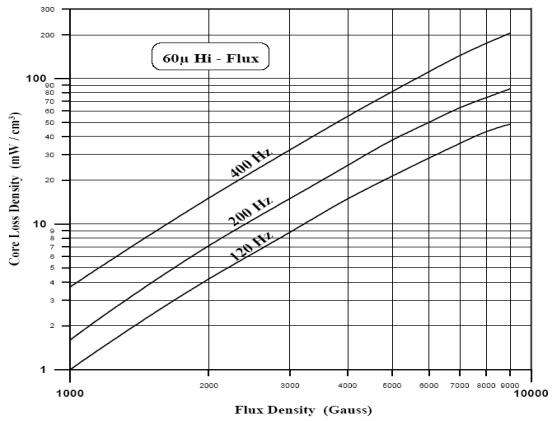

Figure 8. Arnold powder 60µ core loss vs. ac flux density [19].

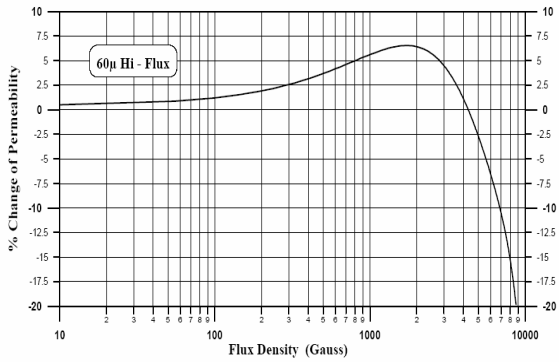

Figure 9. Arnold powder 60µ permeability change vs. ac flux density [19].

The additional harmonic components present in the ac magnetic flux density under unbalanced conditions increase the core losses, even if the total flux density is still below the core saturation level. The extent of this effect is influenced by the choice of core material for the dc choke design.

For example, Fig. 8 shows the ac loss characteristics of one commercial powder that is a candidate for this choke inductor application. Although a specific inductor design is not reported here, Table II provides a parametric comparison of the core loss characteristics of this material at 120 Hz and 360 Hz for three different values of harmonic flux density amplitude. For the unbalance conditions considered in Table I, the amplitudes of the 120 Hz and 360 Hz harmonic flux density components will be roughly equal, with the 120 Hz component being slightly larger. Entries in Table II suggest that the voltage unbalance conditions will increase the core losses by at least 30% because of the presence of the 120 Hz component.

If the unbalance condition persists for a long time, the additional losses could significantly increase the inductor temperature to damaging levels unless these harmonics are appropriately considered during the inductor design process. Incremental copper losses contributed by the resulting ac current components will further aggravate this situation.

As noted above, the elevated harmonic flux density components developed under unbalanced voltage conditions can combine to push the core material into magnetic saturation if the inductor does not have a sufficient safety margin in its cross-sectional area to account for these components. Using the same candidate core powder material as an example, Fig. 9 provides a plot of the core permeability as a function of the flux density, highlighting the sharp drop above 0.2 T (=2 kG). The effect of the core material on the choke inductor value is summarized by the following equation [20]:

$$L = \frac{3.19 \cdot A_c \cdot N^2 \times 10^{-8}}{L_g + L_c / \mu_c} \tag{9}$$

where L is the inductance, A_c is the core sectional area, N is the winding turns, L_g is the air gap length, L_c is the core magnetic path length, and μ_c is the core permeability. The impact of a significant drop in core permeability is readily apparent from this equation.

IV. Lifetime Estimation of Electrolytic Capacitors in ASD Systems

Several factors affect the lifetime of the electrolytic capacitors in ASD systems including applied voltage, ripple current, frequency, ambient temperature, as well as airflow. For example, the dielectric stress is increased if the applied dc voltage is raised. When the operating temperature is near the capacitor's rated value, the additional leakage current that results from operating near the maximum voltage rating can cause electrochemical degradation and hydrogen gas evolution that reduce the capacitor lifetime. As a result, a reduction in the applied dc voltage will extend the capacitor lifetime, especially at elevated temperatures in capacitors that are tightly sealed.

As the ambient temperature, ripple current, air speed, and frequency change, the lifetime changes in response. Ripple current multipliers have been developed [21] to reflect how the capacitor lifetime varies as a function of these factors. Equations (10), (11), and (12) summarize the ripple current multipliers as functions of ambient temperature, frequency and air speed, respectively:

$$m_t = \sqrt{\frac{T_A}{T_R}} \tag{10}$$

$$m_f = \sqrt{\frac{R_S + \frac{D}{2\pi f C}}{R_S + \frac{D}{2\pi f_R C}}} \tag{11}$$

$$m_{as} = \sqrt{\frac{\theta_{CC} + 500\, A^{-7/8} (v+1)^{-2/3}}{\theta_{CC} + 500\, A^{-7/8} (v_R+1)^{-2/3}}} \tag{12}$$

where T_A is the ambient temperature [°C]; T_R is the rated ambient temperature (85°C); R_S is the resistance of electrolyte, tabs, and foils[Ω]; D is the dissipation constant (≈ 0.013); f is the frequency [Hz]; C is the capacitance (F); θ_{CC} is the core-to-case thermal resistance [˚C/W]; A is the surface area of the capacitor (cm^2); v is the airflow velocity (m/s); and v_R is the rated air velocity (≈ 0-1 m/s). Since each multiplier is independently calculated [21], the three factors from (10) to (12) are multiplicative.

Closed-form analysis and computer simulations of the ASD system with ac line inductors (Fig. 3) were presented [9] for evaluating the dc bus capacitor ripple current under voltage unbalance and sag conditions. Subsequent investigation [11] revealed that the same equivalent circuit in Fig. 5 can be used to calculate the ripple current when either ac line inductors or a dc choke inductor is used (Figs. 3 and 4). As discussed earlier, both circuits yield identical results for the same unbalance conditions if the value of the dc choke inductance is twice the value of the ac line inductor. As a result of this equivalency, the design equations previously developed to estimate the capacitor lifetime with ac line inductors [9] can be used for ASD configurations using a dc bus choke inductor by appropriately using the relations (3) and (4).

A systematic methodology for evaluating the impact of voltage unbalance and sag conditions on the lifetime of dc link electrolytic capacitors has been developed to assist engineers who are faced with the task of performing this task. Each of the four steps is discussed as follows:

A. Step 1: Determine Capacitor Current Frequency Spectrum

First, the low-frequency rectifier ripple currents at 120Hz (I_{r120}), 240 Hz (I_{r240}), 360Hz (I_{r360}), and higher (if desired) are calculated using the Fig. 5 equivalent circuit. The switching-frequency ripple current (I_{rPWMx}) components contributed by the inverter are calculated as well [9], where x indicates the frequency of the particular component. The lifetime multipliers summarized in the previous section are then applied to each of the capacitor ripple current frequency components *individually* to incorporate the effects of dc ambient temperature, frequency, and air speed, as follows:

$$I_{rx}^m = m_t \cdot m_{fx} \cdot m_{as} \cdot I_{rx} \tag{13}$$

$$I_{PWMx}^m = m_t \cdot m_{fx} \cdot m_{as} \cdot I_{PWMx} \tag{14}$$

where I_{rx}^m is the modified value of the rectifier-induced ripple current component at frequency x, I_{PWMx}^m is the modified value of the inverter-induced ripple current component at frequency x, m_{fx} is the ripple current multiplier (11) evaluated at frequency x, and I_{rx} is the amplitude of one of the harmonic ripple current components calculated from the Fig. 5 equivalent circuit.

It is important to emphasize that this is the step in the process where the effects of temperature, frequency, and air speed are incorporated into the lifetime calculations by means of (13) and (14).

TABLE III: CAPACITOR CURRENT, LOSS, AND LIFETIME PREDICTIONS

Test Conditions: R_d = 10 mΩ, L_d = 4 mH, C_d = 330 uF, 50% Load, and 2.5% Type C Input Voltage Unbalance

Conditions		Ripple Current (Arms)	Capac. Loss (W)	Hot Spot Temp (°C)	Estimated Cap. Lifetime (hours)
Bal.	Simulation	1.06	0.13	67.2	18,169
Unbal. with DC L_D	Analysis	1.98	0.85	79.3	9,018
	Simulation	2.00	0.88	79.7	8,806

B. Step 2: Calculate Total Capacitor Power Loss

The capacitor's ESR can then be applied to the individual modified ripple current harmonic components I_{rx}^{m} and I_{PWMx}^{m} to calculate the individual adjusted harmonic losses that are then summed as described in [9]. It is important to recognize that the capacitor's ESR rises significantly at low frequencies so that the capacitor losses are particularly sensitive to the low-order rectifier ripple current frequency components (e.g., 120 Hz, 240 Hz).

C. Step 3: Calculate Capacitor Hot Spot Temperature

The capacitor hot spot temperature is calculated using data provided by the manufacturer [9] for the particular capacitor type. This hot-spot temperature is the key determining factor for estimating the capacitor lifetime.

D. Step 4: Calculate Capacitor Lifespan

Finally, the predicted capacitor lifetime is calculated using the relationship between the calculated hot-spot temperature and lifetime provided by the manufacturer [9,22].

An Evox Rifa electrolytic capacitor (Model PEH532VAG3220M2) [22] is used to perform the capacitor loss and lifetime evaluations presented in this paper. The values of the capacitor rms ripple current, loss, hot-spot temperature, and predicted lifetime derived from the closed-form analysis, and simulation results are tabulated in Table III.

For the ASD with a dc bus choke studied in this paper, the predicted capacitor lifetime is approximately cut in half compared to the predicted lifetime with balanced input voltage conditions. The closed-form analytical solution agrees quite well with the simulation results.

V. EXPERIMENTAL TESTS

A 5 hp, 460 V, 60 Hz ASD test bed is used to evaluate the drive characteristics with a dc bus choke inductor under Type C 2.5% unbalanced input voltage conditions. A view of the test configuration is provided in Fig. 10, consisting of a programmable power source, the ASD under test, an external dc choke inductor, and a four-quadrant induction machine load. The measured results are presenting in Table I, confirming very good agreement with the simulation results.

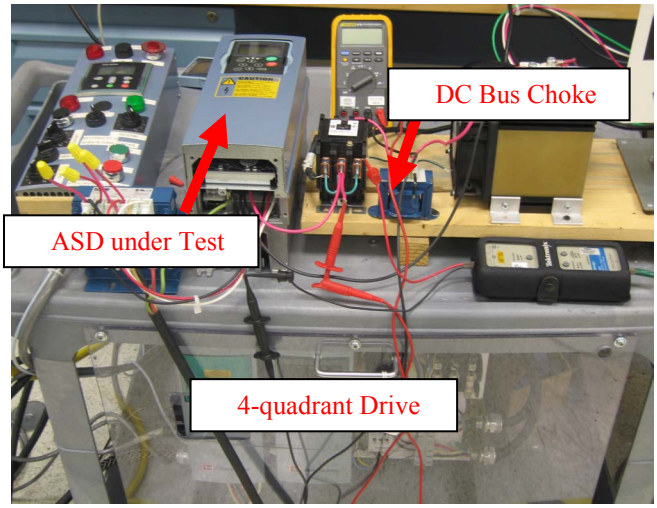

Figure 10. Experimental 5hp ASD test equipment.

It was previously demonstrated [9] that the closed-form analysis and simulation models for estimating the capacitor lifespan do a very good job of matching the experimental results for the same unbalanced operating condition. Since the dc bus capacitors are not accessible for the commercial ASD used for these tests, the experimental capacitor results have not been collected for the dc choke inductor case. Based on the previous results [9], there is reason for confidence that the results in Table III provide useful estimates for predicting the capacitor lifetime as they did with ac line inductors.

These results emphasize the fact that relatively low levels of unbalance in the input voltages can have a very significant impact on the peak temperature and lifetime of the dc bus electrolytic capacitors. The combination of single-phase rectifier operation and capacitor ESR values that increase at low frequencies serve to amplify the detrimental impact of voltage unbalance and sag conditions on the capacitors.

VI. CONCLUSIONS

The impact of input voltage sag and unbalance conditions on the dc bus choke inductor and dc link electrolytic capacitors in adjustable-speed drives has been investigated. Key system tradeoffs associated with choosing an ASD configuration that uses a dc bus choke inductor instead of three line inductors have been identified. Regardless of the inductor location, the ASD is quite vulnerable to transitions into single-phase operation caused by the appearance of even modest levels of input voltage unbalance.

The impact of single-phase operation on the dc bus choke inductor includes elevated core losses and increased risks of magnetic saturation in the inductor core. It has been shown that typical unbalanced voltage conditions can cause the inductor core losses to increase by at least 30% in a powder-core inductor compared to balanced excitation. Extra thermal margin must be designed into the inductor in order to account for the possibility of operation with persistent unbalanced voltages, and a safety margin may also be necessary for the core cross-sectional area in order to avoid magnetic saturation.

The 120 Hz voltage component contributed by single-phase operation causes significant increases in the bus ripple current that raise the temperature of the electrolytic bus capacitors. Calculations using manufacturer data show that the predicted capacitor lifetime under typical voltage unbalance conditions (Type C 2.5% unbalance) can be reduced by approximately 50% compared to its predicted lifetime with balanced excitation.

A 5 hp ASD experimental setup has been used to confirm the predicted operating conditions of the dc bus choke inductor with unbalanced input voltages. These results are intended to assist engineers with the task of designing robust ASD systems despite the presence of unbalanced input voltage or sag conditions.

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APPENDIX

CLOSED-FORM DC BUS EQUATION COEFFICIENTS

The coefficients used in (3) are summarized below. Interested readers are referred to [6] for detailed derivations.

$\tau =$ equivalent damping time constant of the 2nd-order system

$\omega =$ ac excitation frequency

$\Omega =$ equivalent damped resonant frequency of the 2nd-order system.

$$\tau = \frac{2}{R_s \big/ L_s + 1 \big/ R_L C_d} \qquad \text{(A1)}$$

$$N = \left| \frac{R_L \parallel 1 \big/ j\omega C_d}{R_s + j\omega L_s + R_L \parallel 1 \big/ j\omega C_d} \right| \qquad \text{(A3)}$$

$$\Omega = \sqrt{\frac{1 + R_s \big/ R_L}{L_s C_d} - \frac{1}{\tau^2}} \qquad \text{(A2)}$$

$$\Omega' = \frac{1}{\sqrt{L_s C_d}} \qquad \text{(A4)}$$

$$\phi = \angle \left[\frac{R_L \parallel 1 \big/ j\omega C_d}{R_s + j\omega L_s + R_L \parallel 1 \big/ j\omega C_d} \right] \qquad \text{(A5)}$$

$$A = \left| (1 - N)\cos\omega t_{in} + \frac{j}{\Omega'} \left\{ \frac{1}{R_L C_d} \cos\omega t_{in} - N\omega \sin\omega t_{in} \right\} \right| \qquad \text{(A6)}$$

$$t_x = \frac{1}{\Omega} \left[t_{in} - \angle \left(\begin{array}{l} (1 - N)\cos\omega t_{in} + \\ \frac{j}{\Omega'} \left\{ \frac{1}{R_L C_d} \cos\omega t_{in} - N\omega \sin\omega t_{in} \right\} \end{array} \right) \right] \qquad \text{(A7)}$$