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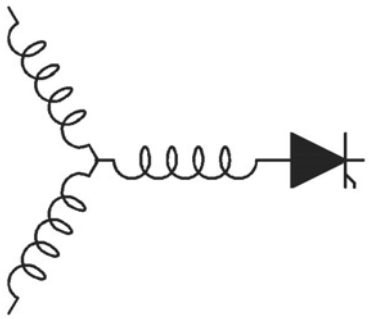

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Low Voltage Ride-Through Capability for Wind Turbines based on Current Source Inverter Topologies

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***Abstract*—This paper proposes a circuital solution, aimed at a class of current-source inverter topologies, that provides the ability to ride-through temporary low voltage, as well as open circuit conditions at the mains without opening the mains circuit breakers. Although the proposed solution has broader applications, it is described in the framework of a previously published current-source inverter topology for modern wind turbines. For such systems, the low voltage ride-through capability is becoming a necessary feature. The current source topology considered exploits the cable length between the nacelle and the ground to provide a significant portion of the dc-link inductance. Prior work discussed the control strategy, flexibility, design rules, protection and experimental results of this topology and acknowledged the need for low-voltage ride through capability. One possible solution, derived from an already proposed protection scheme, is presented together with selected simulation and experimental results.**

***Index Terms*—Current-Source Topology, Low Voltage Ride-Through, Open circuit fault, Wind Turbines.**

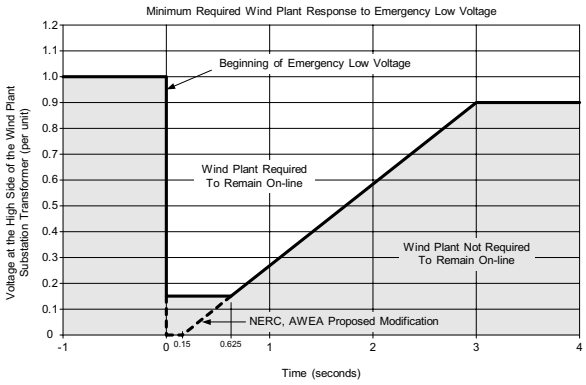

Fig. 1. Low Voltage Ride-Through (LVRT) requirement per Appendix G of FERC's Large Generator Interconnection Agreement (LGIA).

I. Introduction

Historically, wind turbine power generation was only a minute percentage of the total installed generating capacity, a situation commonly referred to as *low wind power penetration*. The somewhat sporadic nature of wind power generation is similar to the relatively sporadic nature of loads and, in the case of low wind power penetration, could be handled in a similar manner. Hence, wind turbines were allowed to disconnect from the grid whenever the situation suited the wind turbine.

However, with increasing wind power penetration, the simultaneous disconnection of a significant percentage of generating capacity can have a profound effect on the stability of the grid, especially when such an event is triggered by another grid fault, such as low-voltage due to a short-circuit or an over-load condition. In the United States, this led the Federal Energy Regulatory Commission (FERC) to propose a low voltage ride-through (LVRT) requirement in Appendix G of its Order No. 661, Large Generator Interconnection Agreement (LGIA) which was issued June 2, 2005 [1]. The new LVRT rule, applying to wind turbine facilities greater than 20 MW, specifies a depth of sag versus time envelope for which a wind turbine is expected to remain on-line and is shown as the solid line in Fig. 1. For example, an applicable wind-turbine generator would be required to remain online during a low-voltage event down to 15% of nominal voltage for up to 0.625 seconds (37.5 cycles at 60 Hz frequency). Similar rules have been proposed or implemented in other countries with high or increasing levels of wind-power penetration as well. However, the North American Electric Reliability Council (NERC) together with the American Wind Energy Association (AWEA) have since proposed a change to the LVRT requirement of Order No. 661 to resolve differences with the existing NERC standard TPL-002-0 which dictates minimum system performance following a single grid fault. The proposed change would require generators to remain on-line for low-voltage conditions down to zero volts for a period not to exceed 9 cycles (0.15 seconds) [2]. This more severe requirement is indicated by the dashed line in Fig. 1. These grid disturbances, as well as other anomalies such as open-circuit conditions, can pose problems for many of today's variable-speed wind turbines.

II. Current Source Topology for Wind Turbines requiring Ride-Through Capability

Fig. 2 shows the schematic of the current source topology for wind turbines previously proposed in [3]–[5]. The inverters (marked 1 and 2 in Fig. 2) employ fully-controllable switches with bidirectional voltage-blocking and unidirectional current-blocking capability. Neither inverter employs PWM modulation, but rather operates under the common phase-control-angle technique, with phase control angles ϕ_1 and ϕ_2 for inverter 1 and 2, respectively. The equations describing a three-phase, phase controlled converter connected to an ideal current

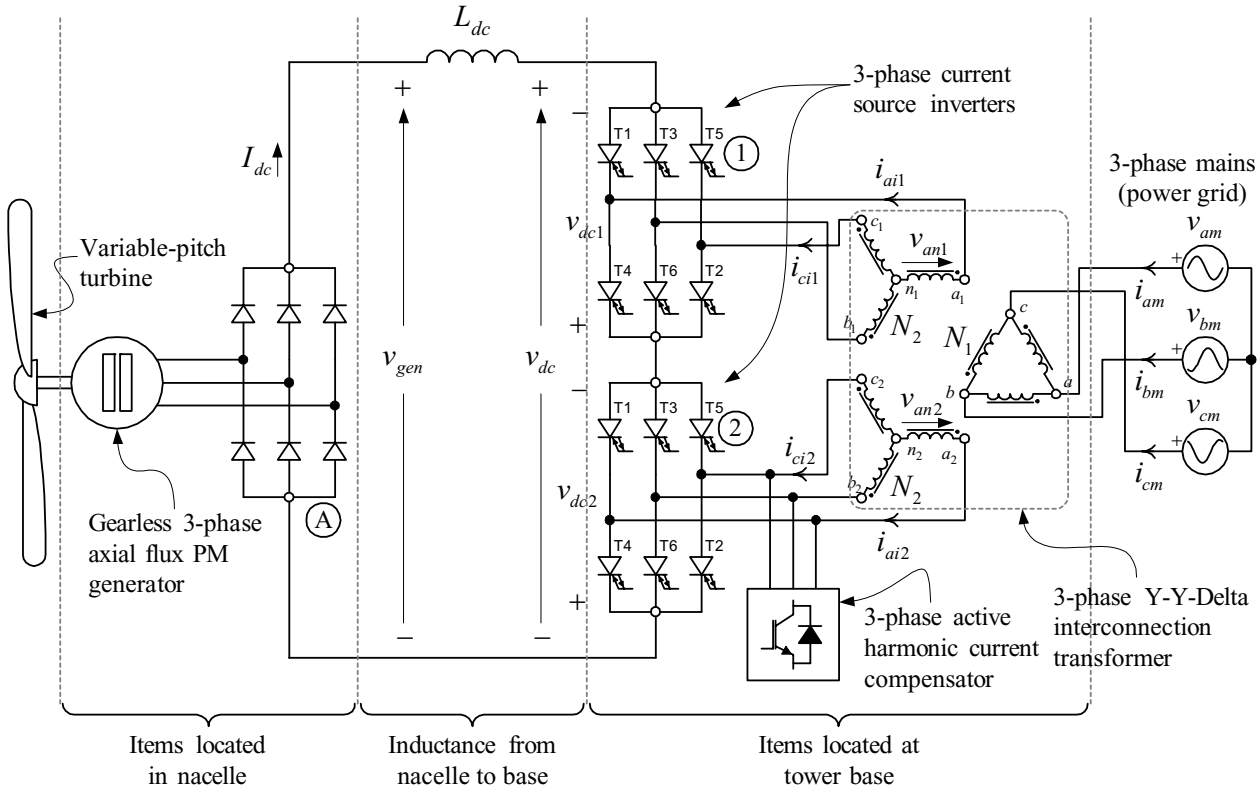

Fig. 2. Proposed Current source topology for gearless variable-speed wind turbines employing a permanent magnet synchronous generator.

source I_{dc} at its two-terminal port and to a symmetrical three-phase system of ideal voltage sources at its three-terminal interconnect, under the action of phase control angle ϕ, are well known [6], [7]. The average voltage $\langle v_{dc}(t)\rangle$ measured across the two terminals of the ideal current source is a function of both the root mean square (RMS) value of the three-phase line-to-line voltage V_{LL} and the phase control angle ϕ. This relationship, in the generator convention, is given in (1). Furthermore, the n-th harmonic mains line current $i_{a(n)}(t)$, as a function of the current I_{dc} and phase control angle ϕ, is given by (2) where ω is the mains frequency expressed in radians per second.

$$\langle v_{dc}(t)\rangle = \frac{3\sqrt{2}}{\pi} V_{LL} \cos\phi \tag{1}$$

$$i_{a(n)}(t) = \frac{2I_{dc}}{\pi n}\left(1-(-1)^n\right)\cos\left(\frac{\pi n}{6}\right)\sin\left[n\left(\phi-\omega t\right)\right] \tag{2}$$

As is evident in (2), one of the main disadvantages of the phase controlled converter is the poor fundamental displacement power factor imposed by large values of ϕ. However, the proposed topology compensates for this short-coming by employing two converters in series whose three-phase line currents are linearly combined by a proper Y-Y-Δ interconnection transformer to the mains, which acts as an algebraic operator over such currents. This circuital structure allows to impose a desired fundamental power factor at the mains via the two independently adjustable phase control angles ϕ_1 and ϕ_2. In [4] it was shown that, through the linear mapping on the converter phase control angles as given in (3), decoupled control of the fundamental amplitude and phase of the mains line current is achievable.

$$\alpha = \frac{\phi_1 - \phi_2}{2} \qquad \beta = \frac{\phi_1 + \phi_2}{2} \tag{3}$$

For the chosen reference polarities indicated in Fig. 2, the average dc-link voltage $\langle v_{dc}(t)\rangle$ and the n-th harmonic mains line current $i_{am(n)}(t)$ are given by (4) and (5), respectively [4].

$$\langle v_{dc}(t)\rangle = -\frac{6\sqrt{6}}{\pi}\frac{N_2}{N_1} V_{LL} \cdot \cos\alpha \cdot \cos\beta \tag{4}$$

$$i_{am(n)}(t) = \frac{8I_{dc}}{\pi n}\frac{N_2}{N_1}\left((-1)^n - 1\right)\cos\left(\frac{\pi n}{6}\right)\sin\left(\frac{\pi n}{3}\right) \cdot \cos\left(n\alpha\right)\sin\left[n\left(\beta-\omega t\right)\right] \tag{5}$$

Hence, the dc-link voltage, and thus the dc-link current, together with the average generator torque, can be controlled via either α or β. However, for a given dc-link current, α determines the amplitude of the fundamental mains line current while β, independently determines its phase. In this way, one can control both the active and reactive power injected to the mains by the wind turbine according to (6) and (7), respectively.

$$P_{mains} = \frac{6\sqrt{6}}{\pi}\frac{N_2}{N_1} V_{LL} \cdot I_{dc} \cos\alpha \cos\beta \tag{6}$$

$$Q_{mains} = P_{mains} \tan\beta \tag{7}$$

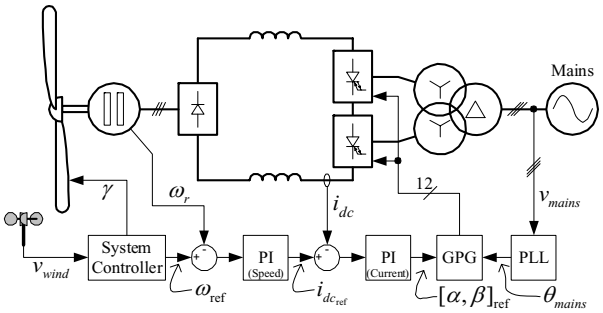

Fig. 3. Overview of the control system principle.

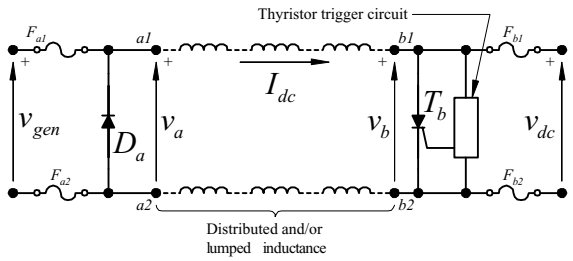

Fig. 4. Decentralized protection scheme.

Fig. 3 shows a simplified control block diagram for the proposed topology. The system controller provides the high-level system commands based on various external parameters such as wind speed, VAr requirements and so on. It is responsible for the maximum power tracking capability of the wind turbine, providing the commands for both the rotor blade pitch and the generator speed. The speed control loop then develops the command for generator torque, which translates into the dc-link reference command $I_{dc_{\text{ref}}}$. The current control loop then develops the inverter voltage command, culminating in the control angles α_{ref} and β_{ref}. The control angles are then acted upon by the gate pulse generator which transforms the control angles α_{ref} and β_{ref} through an inverse mapping of (3) into the individual converter firing angles ϕ_1 and ϕ_2. It develops the inverter gate pulses with respect to the mains phase angle θ_{mains}, which is determined by a phase-lock-loop (PLL).

Selected simulation and experimental results for a 10 kW prototype of this conversion scheme were presented in [3], [4], [8] where it is also shown that specific values of α improve the spectrum of the mains currents. The harmonic content of such currents can be reduced further by providing the three-phase active harmonic compensator shown in Fig. 2. Additional simulation and experimental results (some in transient conditions), additional pictures of the laboratory prototype, as well as a more detailed description of it, are present in the technical report published by the National Renewable Energy Laboratory (NREL) [5]. It is obtainable by searching for the authors' names in the website specified in the reference.

III. Fault Protection Scheme at the basis of the Ride-Through Capability

Although the ride-through requirements might seem uncorrelated with the fault protection needs, some fault scenarios do share common characteristics with a low-voltage or open circuit events at the grid. However, it will be shown that it is possible to ride-through such events only by increasing the flexibility of the circuits originally conceived for fault protection schemes. Hence, it may be useful to revisit the fault protection circuit previously proposed by the authors in [9] in some detail before describing, in the following section, the small modifications necessary to provide the LVRT capability.

Current source topologies require protection schemes aimed at preventing faults having the "dual" character from those particular to voltage source topologies. The protection against open-circuits and the often accompanying over-voltages in current source topologies is just as important as the protection from short-circuits and the often accompanying over-currents in voltage source topologies. Nevertheless, in current source topologies it is also necessary to protect components against over-currents in order to limit electro-dynamic stresses. This is of prominent importance not only for the semiconductors, but for the passive components as well, including the distributed dc-link inductor.

In the current source based conversion circuit shown in Fig. 2 several events can occur that may result in an open circuit condition; a) a failure in the generator and/or rectifier, b) a failure in the dc-link conduction path, c) a failure in one of the inverter circuits, or d) a grid anomaly which manifests itself as an open-circuit at the mains. Without an emergency current conduction path, any one of these events could lead to destructive over-voltages. Furthermore, any possible event capable of rendering $v_{gen} > v_{dc}$ for a sufficiently long interval of time can lead to a potentially dangerous increase of the dc-link current I_{dc}. For example, inverter failures resulting in a short-circuit or a grid anomaly manifesting itself as a low voltage (or zero voltage) at the mains could lead to an uncontrollable increase in the dc-link current.

In [9] the authors introduced a decentralized scheme suitable for protection of the current source inverter topology and in particular, the dc-link inductance, against these "dual" types of dangerous events. The scheme was especially conceived to suit inductors of a distributed nature and to not incorporate any "active" components. The circuit on which the proposed protection scheme is based is shown in Fig. 4. It employs only fuses, a free wheeling diode and a thyristor triggered by a fully passive auxiliary circuit. Additionally, the circuit was conceived to avoid the need of any exchange of information between the two ports $(a1, a2)$ and $(b1, b2)$ (as shown in Fig. 4) which, in the case of a distributed inductance, may be physically located far apart.

Observing Fig. 4, it is possible to analyze briefly how the protection scheme operates in the different fault conditions. As a consequence of an open-circuit, the two following network evolutions are possible:

I) An open circuit event to the left of port $(a1, a2)$, either because of a fault in the generator/bridge or because of the intervention of fuses F_{a1} and/or F_{a2}, forces the dc-link current I_{dc} to flow in the diode D_a. During the interval of the open circuit, the voltage v_a becomes equal to the negative forward voltage drop of the diode while the voltage v_b remains greater than zero. This voltage difference in conjunction with any additional dissipative phenomena forces I_{dc} to decrease, eventually, to zero.

II) An open circuit event to the right of port $(b1, b2)$, due to a grid anomaly, an inverter fault or the intervention of fuses F_{b1} and/or F_{b2}, would cause the voltage v_b to rise indefinitely unless a proper recirculation path for I_{dc} is provided. This is exactly the function of the thyristor T_b.

The thyristor trigger circuit shown in Fig. 4 is designed to switch 'on' the thyristor T_b when v_b reaches a chosen threshold value considered damaging to the converter. After its characteristic turn-on time, the thyristor T_b is in the conduction state, providing the necessary recirculation path for I_{dc}. From this instant onwards, I_{dc} could be controlled by modifying the voltage v_a in such a way that the integral function $\psi_{ab}(t)$ defined in (8) is properly limited.

$$\psi_{ab}(t) = \int_0^t [v_a(\tau) - v_b(\tau)]\, \mathrm{d}\tau \tag{8}$$

Conversely, if this goal is not achievable, I_{dc} will rise until at least one or both of the fuses F_{a1} and F_{a2} intervene, leading to an open circuit event belonging to scenario I described previously. In this case, the final circuit configuration of scenario II is characterized by a dc-link inductor that does not exchange energy with the rest of the network – because at least one fuse among $\{F_{a1}, F_{a2}\}$ and one among $\{F_{b1}, F_{b2}\}$ has intervened – while its current recirculates in the loop created by T_b and D_a, both in the conduction state. The current I_{dc} decreases with a rate defined by the extent the dissipative phenomena present in the loop. Further analysis, the details of the trigger circuit and experimental results are given in [9].

IV. Extension of the Protection Circuit to provide Ride-Through Capability

The analysis of the previous section showed that the evolution of the network in both scenarios I and II involve time intervals in which v_a or v_b are almost zero. This means that the basic structure of the protection network described above is already compatible with low voltage or even short-circuit scenarios at either port, but especially at the inverter port $(b1, b2)$, whose electrical quantities are immediately influenced by anomalies occurring at the point of interconnection with the mains. However, the intervention of fuses, or even the triggering of T_b, is not a suitable response to an event the system is expected to quickly recover from or to ride-through.

It will be shown in the subsequent paragraphs that the addition to the protection circuit of Fig. 4 of only one fully controllable device and associated snubber components along with an extended inverter control strategy will allow the system to cope with low-voltage and open-circuit grid anomalies in a repeatable manner without the intervention of protective devices. Fig. 5 shows the proposed modified system, complete with fault protection, capable of meeting the LVRT requirements, even down to zero-voltage, as well as automatically recovering from a grid-side open circuit.

A low-voltage condition at the mains of the proposed wind turbine topology leads to a reduction of the time-averaged quantity $\langle v_b \rangle$. A complete loss of mains voltage, due to a symmetric short-circuit at the grid, leads to $v_b \simeq 0$, and is akin to thyristor T_b conducting in scenario II, albeit the conduction path now includes the fuses F_{b1} and F_{b2}. Obviously, the intervention of the fuses is a drastic measure, that must be avoided in the LVRT strategy. Hence, as stated previously, a means of limiting I_{dc} via control of v_a is needed.

This is achieved through a sequence of repeated, and controlled, interruptions of the dc-link current exiting the diode bridge (marked A in Fig. 5). The network evolution in this case is the same as that described in scenario I because any interruption of the current in that part of the circuit is equivalent to an open-circuit event to the left of port $(a1, a2)$. When the diode D_a conducts, v_a is equal to the negative forward voltage drop of the diode D_a, providing the modulation of the voltage v_a that reduces the function $\psi_{ab}(t)$. In order to create such a controlled sequence of interruptions, the authors propose the addition of a series connected fully controllable switch T_a (for example a GTO or an IGCT) located in the nacelle, between diode bridge A and the port $(a1, a2)$.

It is necessary to provide a turn-off snubber across the power terminals of T_a as a means to absorb and then dissipate the energy stored in the generator leakage inductance as well as the stray inductance of the diode bridge and associated connections. Just after T_a is turned off, I_{dc} flows through the diode D_{sw} and the capacitor C_{sw}, charging it until the voltage v_{sw} slightly exceeds v_{gen}. When this condition is met, the current I_{dc} commutates to the diode D_a until T_a is turned on again. The capacitor C_{sw} must be selected with the aim of rendering its charging transient considerably shorter than the minimum chosen open-circuit duration, especially at low values of I_{dc}. In Fig. 5, it is straightforward to recognize the basic structure of a dc-dc buck converter whose elements are the switch T_a, the diode D_a and the dc-link inductor. The diode bridge and the dc side of the series connected CSIs constitute the two DC voltage sources between which the energy conversion occurs.

During the time interval that T_a is turned off, the current is diverted from the generator. Hence, the electromagnetic torque is zero. With an accompanying reduction of the applied mechanical torque, the generator will accelerate. Usually the large moment of inertia of the

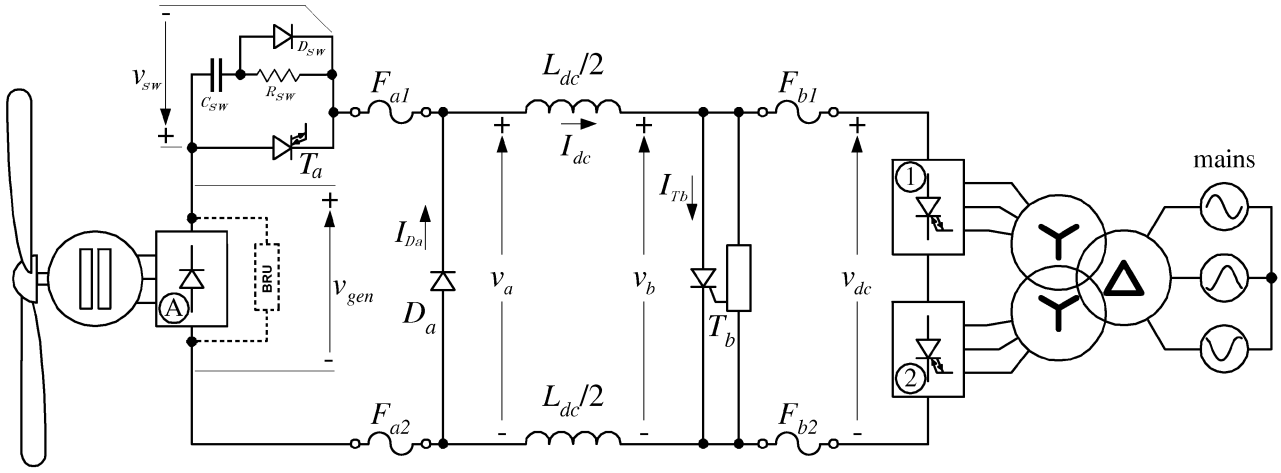

Fig. 5. Modified CSI topology to provide both fault protection and ride-through capability.

turbine and generator prevents over-speed risks in a time interval of some seconds. In the case of an extended event, the mechanical torque applied to the generator can be decreased by means of the rotor-blade pitch controller. In extreme cases, where the previous measure is not sufficient, it would be possible to add also a braking unit (BRU) directly connected at the output of diode bridge A as is shown in Fig. 5.

The dual type of temporary grid anomaly, i.e. the open circuit condition at the mains, is similar to the open circuit scenario II. Nevertheless, riding-through this event requires that v_b does not reach the value at which the thyristor control circuit turns on T_b. This goal can be achieved by creating a recirculation path for I_{dc}, which is alternative to the one that would be provided by T_b. In order to recover from the anomalous event at any instant, it is necessary that such an alternative path can be opened or closed in a fully controllable way. The authors propose to create the alternative recirculation path by simultaneously turning on, in each of the two inverters, the two switches belonging to one, and only one, chosen phase-leg. All other switches, belonging to the other phase-legs, are simultaneously turned off. In the most general case of an inverter which uses fully bidirectional switches, this last turn off command is necessary to prevent short circuits from occurring between any possible combination of phases belonging to the same three-phase inverter.

This alternative path, obtained by voluntarily creating a short-circuit at the dc side of both inverters, satisfies the requirements since it can be created or eliminated at any moment due to the fully controllable nature of the switches employed in the inverters. This solution does not require any additional components. After the circulation path for I_{dc} is provided, as described above, the network evolution and its related requirements are identical to the LVRT case discussed previously. Indeed, for the whole network located to the left of the port $(b1, b2)$, the artificially created short-circuit at the inverter's dc side is indistinguishable from a short-circuit in the grid.

In the extreme case where the control of I_{dc} is lost for any reason, leading to the intervention of the fuses F_{b1} and/or F_{b2} as well as F_{a1} and/or F_{a2}, the protection of the system would be ultimately provided by T_b and D_a in full accordance to the open-circuit scenario II. Further details about the implementation of the LVRT and open-circuit strategies are given in the following subsections.

V. Selected Simulation Results

A simulation model using PLECS, Simulink and Matlab has been constructed of the experimental setup described in [3]–[5], [8]. The parameters of the model are as follows: The nominal RMS value of the line-to-line voltage, both at the primary and the secondaries of the 60 Hz transformer is 230 V. The dc-link inductance is 100 mH and the 48-pole axial-flux permanent magnet generator is characterized by 620 V peak line-to-line voltage at no-load and 570 RPM. The generator has been designed such that, in normal operating conditions and with desired unity fundamental power factor (β^*=0), the angle α can assume the optimum value of 0.914π, leading to a significant reduction of the mains line current harmonic content [3], [4]. The chosen wind turbine average power (7 kW) leads to a dc-link reference current I_{dc_ref} around 11.5 A. It is chosen that the overall system controller maintain I_{dc_ref} practically constant during the LVRT and open-circuit events and that the current hysteresis band be 5 A, a value that leads to switching frequencies, as well as minimum 'on' and 'off' times, suitable for the slowest high-power semiconductor switches currently available.

The simulation results, according to each particular grid event, are described in the following subsections.

A. Ride-Through of a Low Voltage event at the Mains

During normal operation, with the value of the mains line to line voltage V_{LL} inside the accepted tolerances, the series connected switch T_a is continuously gated (or turned on), therefore it produces only conduction losses.

A LVRT event begins when V_{LL} is reduced below such tolerances. Assuming a constant average rectified generator voltage $\langle v_{gen}(t) \rangle$ over the duration of the LVRT event

in question and a desired fundamental power factor at the mains imposed by a specified angle β^* [4], [8], the control angle α is gradually increased, by the controller, towards π as V_{LL} continues to decrease. This occurs because the controller attempts to maintain $\langle v_{gen}(t)\rangle$ equal to $\langle v_{dc}(t)\rangle$ in order to preserve the dc-link current I_{dc} at the reference value. When α assumes the maximum value π and V_{LL} continues to decrease, β must be reduced, ultimately, to zero in order to maximize $\langle v_{dc}(t)\rangle$ according to (4). At this point, if V_{LL} continues to decrease such that $\langle v_{gen}(t)\rangle > \langle v_{dc}(t)\rangle$ for a sufficiently long interval of time, inverter control of the dc-link current is lost and I_{dc} will rise.

When I_{dc} reaches a chosen upper threshold, the switch T_a is turned off and I_{dc} then commutates from the generator to the diode D_a as previously explained. After this instant, I_{dc} begins to decrease, however the inverters will continue to synthesize the mains line current from the remaining dc-link current according to (5) to aid in grid-fault clearing. As I_{dc} decays below a specified lower threshold level T_a is turned on again. If the fault has cleared, the system will resume normal operation. Conversely, if the fault has not cleared, the process will be repeated until the LVRT event is ended. As is the case with a dc-dc buck converter, switching T_a to control I_{dc} renders $\langle v_a(t)\rangle = \langle v_{dc}(t)\rangle$.

It should be noted that special attention must be given to maintaining converter synchronization to the grid, especially during a zero-voltage event which may cause the synchronization mechanism (usually a PLL) to drift. This issue is not specific to the proposed topology, but it is shared by all types of conversion circuits, because it arises from a fundamental lack of information about the phase of the mains voltage. While this is an important practical issue, it is outside the scope of this paper. Nevertheless, assuming this information is available, the proposed LVRT technique is capable of delivering mains current even down to zero mains voltage to assist in fault clearing. In any case, it is never necessary to open the mains breakers, thus satisfying the most crucial LVRT requirement.

Figs. 6 and 7 show one selected simulation result for a LVRT event characterized by the minimum value of V_{LL} (0.15 PU) specified by the present FERC standard. Fig. 6 shows the entire event, whereas Fig. 7 shows the LVRT event on an expanded time scale in order to more closely analyze the details. The electrical quantities listed in the legend are identified by the same names used in the circuit diagrams of Figs. 2, 4 and 5.

The condition chosen to identify the beginning of a LVRT event and to switch to the LVRT control strategy is $(\alpha > 0.98\pi)\mathrm{AND}(I_{dc} > I_{dc\_ref})$. Indeed having α so close to π means that the proportional-integral (PI) dc-link current controller, whose key output is the necessary $\langle v_{dc}\rangle$, cannot increase such voltage any more to maintain the control of I_{dc}. This controller uses the measured V_{LL} and desired β^* to compute α from $\langle v_{dc}\rangle$ via (4), thereby improving the response dynamics of the

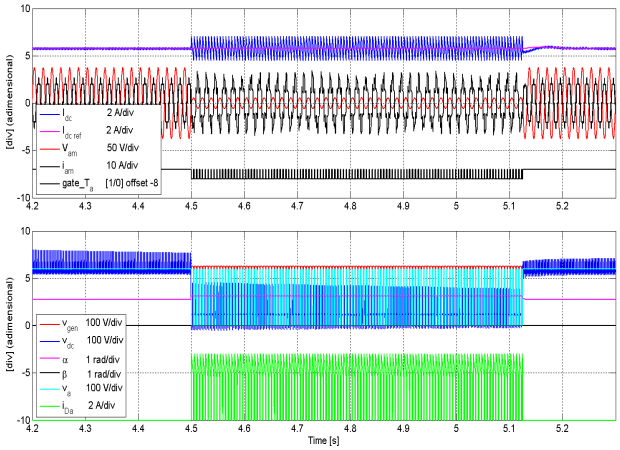

Fig. 6. Most significant quantities during a LVRT event lasting 0.625 seconds with percentage V_{LL}= 0.15 PU

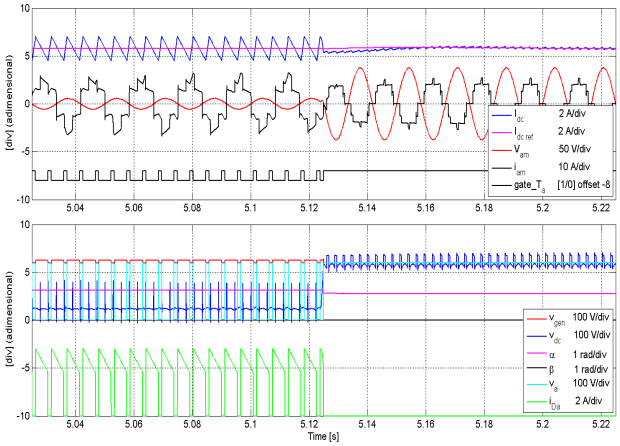

Fig. 7. Most significant quantities during the same LVRT event as Fig. 6 on an expanded time scale highlighting the recovery transient.

converter. Entering the LVRT control mode, immediately activates the hysteretic controller of I_{dc} that commands the commutations of T_a, as is evident from Fig. 6 and 7, to achieve $\langle v_a\rangle = \langle v_{dc}\rangle$. The hysteresis thresholds are symmetrical around $I_{dc_{\mathrm{ref}}}$. The end of the LVRT event is detected by the condition $V_{LL} > 0.9V_{LL_{\mathrm{nom}}}$ (where $V_{LL_{\mathrm{nom}}} = 230$ V).

From Fig. 7, one can notice that the I_{dc} control in normal operation and, consequently, the lower harmonic content in the mains currents are recovered in less than two fundamental cycles. Because of the aforementioned use of (4) to compute α in the dc-link current PI regulator, such an angle recovers its optimum value very quickly at the end of the LVRT event. Additionally, one can observe that, during the LVRT event, the pulsed voltage v_a has an average value that satisfies the necessary condition for current stability $\langle v_a\rangle = \langle v_{dc}\rangle$ and that the switching frequency of T_a is around 200 Hz with 'on' times around 1 ms. The high-frequency voltage spikes observable in v_{dc} during the LVRT event are due to the diode bridge-based snubbers, described in [4], [8], whose dc-link capacitors still possess voltage values close to the secondary line-to-

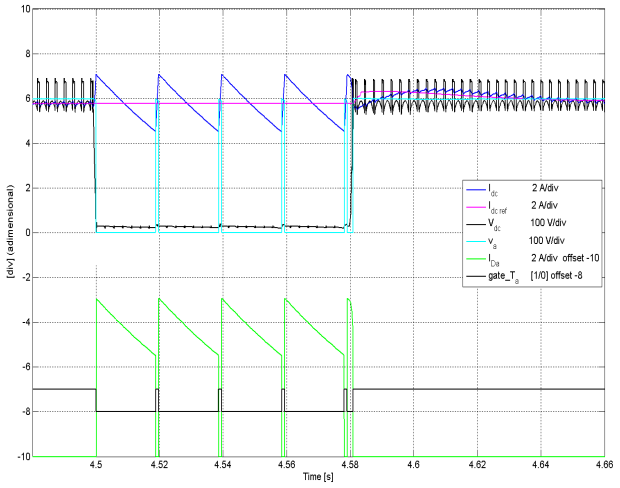

Fig. 8. OCRT event lasting 80 ms with 5A hysteresis band

line peak nominal voltage ($230\sqrt{2}$ V). This is due to the relatively short duration of the LVRT event which does not allow those capacitors to discharge significantly via their parallel connected resistors.

B. Ride-Through of an Open Circuit event at the Mains

It is important to highlight that an open-circuit event, as defined in this paper, is characterized by an open-circuit condition at the point of interconnection with the grid of one single wind turbine. This is a very different case from what is commonly called "islanding", a scenario that usually involves one or more generators and loads connected together to form a smaller grid that has become isolated from the main one. The capability to ride-through an open-circuit at the grid is addressed here because this event is particularly harmful for current source inverters.

An open-circuit event lasting 80 ms has been simulated and the most significant waveforms are shown in Fig. 8. After the detection of the open-circuit event, the two inverters are voluntarily short circuited at their dc side by gating the proper switches. As stated previously, from this instant onwards, the open-circuit event is essentially indistinguishable from a zero voltage LVRT event to the left of port $(b1, b2)$.

Observing Fig. 8, one can notice that the voltage spikes previously present in v_{dc} during the LVRT event are now absent during the open-circuit event because port $(b1, b2)$ is directly short-circuited by the inverters, whose commutations have stopped. The control of $I_{dc_{\text{ref}}}$ by the overall system controller is more difficult during a recovery from an almost zero v_{dc}. Nevertheless, the normal control of I_{dc} is resumed in about 80 ms from the end of the open-circuit event. Here, the switching frequency of T_a is around 50 Hz, lower than the previously shown LVRT case, due to the fact that $v_a \approx v_{dc}$ when D_a conducts. This, in turn, leads to a much slower rate of decay of I_{dc}. As a consequence, I_{dc} requires more time to reach the low hysteresis threshold when compared to the presented LVRT case and this explains the lower switching frequency. Observing the waveforms, one can

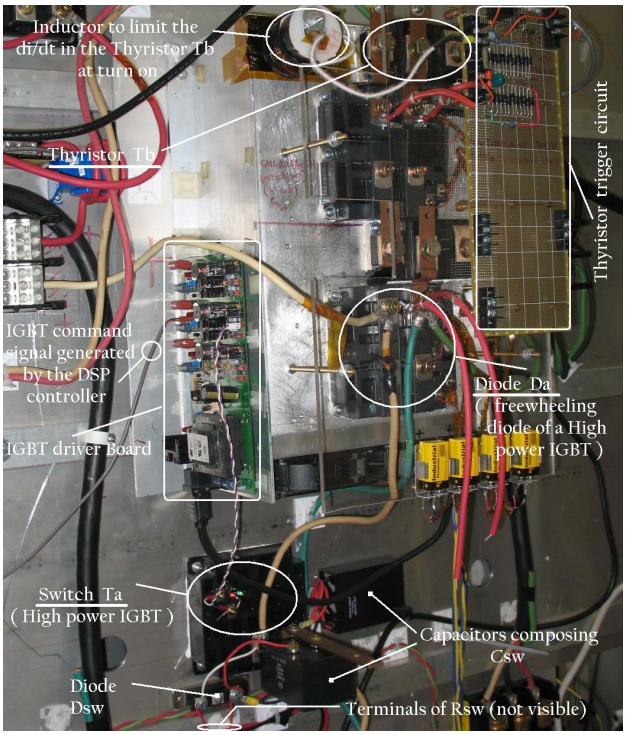

Fig. 9. Photo of the Switch T_a and fuses F_a1 and F_a2

infer that the necessary condition $\langle v_a \rangle = \langle v_{dc} \rangle$ is satisfied. The switching frequency of T_a is almost constant both in the LVRT and open-circuit cases despite the strong hysteretic nature of the LVRT control mode. This occurs because the staircase-shaped voltage $v_a - v_{dc}$ applied across the inductor terminals is characterized by voltage levels having good stability to which relatively high-frequency and regular ripples are superimposed.

VI. Selected Experimental Results

Figure 10 shows a selection of waveforms extracted from the experimental test of the intervention of the thyristor trigger circuit and the subsequent turn on of the thyristor T_b. These are the most important subsystems for the ultimate fault protection of the current source inverter topology, as well as for the detection of an open-circuit event. The recorded waveforms are labeled with the names of the quantities they represent according to the names used in Figs. 2, 4 and 5. Further experimental tests and details, also concerning the internal structure and operation of the thyristor trigger circuit, are reported in [9].

An open circuit event is created to the right of port $(b1, b2)$ through a high-power IGBT connected in series and used as breaker. Immediately after having turned off the IGBT, the voltage v_b begins to rise linearly because the current I_{dc} is initially diverted into a properly designed capacitor present in the thyristor trigger circuit [9]. When v_b reaches the desired intervention threshold, T_b is turned on. It is possible to identify this instant in Fig. 10 by observing the fast rise of the current I_{T_b} (its time derivative is limited by a turn-on snubber inductance

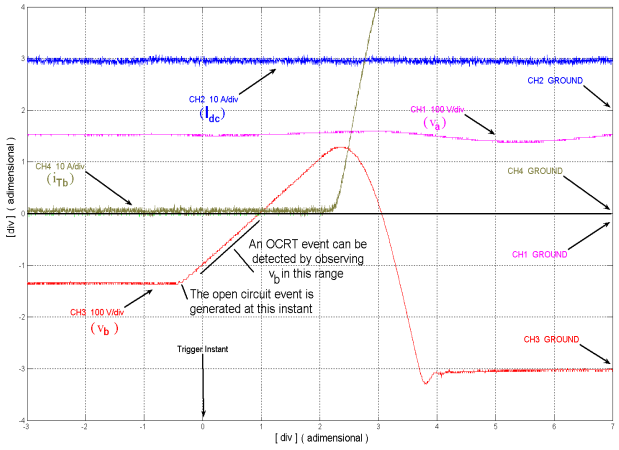

Fig. 10. Turn on of Thyristor T_b after a short circuit event at the left of port $b1 - b2$

connected in series to T_b). From this point onwards I_{dc} is diverted into T_b. The current I_{T_b} temporarily exceeds the value I_{dc} because of the discharge of the aforementioned capacitor through T_b and the turn-on snubber inductance. The similar linear rise of v_b which follows an open-circuit at the grid can be used to detect the open-circuit event. The inverter bridges can be short-circuited when v_b reaches a chosen voltage threshold set well below the one which would trigger T_b.

Fig. 9 shows a picture of a specific area of the experimental setup where all key components of the extended protection scheme are located. The text superimposed on the picture identifies those components according to the names used in Figs. 2, 4 and 5. Additionally, it is possible to observe the turn-on snubber inductance, used to limit the time-derivative of the current flowing in T_b at turn on, together with the IGBT driver board used to commutate T_a which is constituted by a high-power IGBT.

VII. Conclusions

It is a fast-approaching reality that any sizable wind-turbine facility will be expected to perform in a manner similar to their more traditional brethren. As the quest for higher-performance, higher-power wind turbines continues, newly proposed topologies must also be measured with respect to their ability to react to grid anomalies. Regulatory agencies in the United States, Europe and other parts of the world have begun to set minimum standards for wind turbine performance in this regard.

With an eye towards the issues involved in scaling existing wind-turbine technology into the multi-megawatt realm, the authors have proposed a variable-speed wind-turbine employing a gearless axial-flux permanent magnet synchronous generator coupled by a fully-rated, line-frequency switched, current source inverter, the details of which have been reported in previous works.

In this paper, the authors have explored the operation of the proposed topology with respect to both low-voltage (including short-circuit) and open-circuit grid conditions and have demonstrated similarities with fault modes existing within the converter itself.

At the system level, many different possibilities exist with respect to both the mechanical and the electrical control of generator torque during such events. The operation of the modified topology, under one possible control scenario (maintaining constant dc-link current), was successfully demonstrated through simulation. It was shown that the topology could continue to provide fault-clearing current to the mains during a low-voltage or short-circuit event and that, with an expanded inverter algorithm, the topology can repeatedly withstand, and recover from, an open-circuit event.

Experimental results of the action of the fault protection circuitry during an open circuit event were shown to demonstrate the ability of the system to withstand an open-circuit condition.

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