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Input Harmonic Estimation and Control Methods in Active Rectifiers

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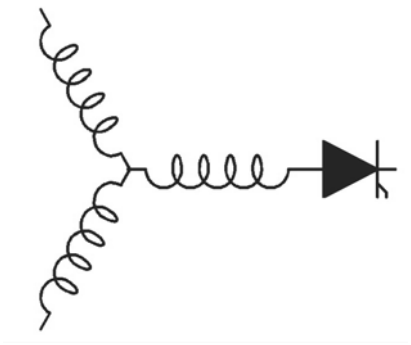

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Input Harmonic Estimation and Control Methods in Active Rectifiers

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***Abstract* - Active rectifiers using PWM voltage-source converters (VSCs) are popular choices for adjustable-speed drives to provide high input power quality. However, input current harmonics are often generated as a result of input voltage source disturbances. Since the frequencies of the 5th-, 7th-, and higher-order harmonics can easily exceed the current controller bandwidth in high-power applications, the elimination of these harmonic disturbances imposes difficult control challenges. Cost-effective observer-based harmonic estimation and mitigation methods are introduced in this paper that compensate delay effects caused by the digital signal processing. Such delays can significantly limit the current controller bandwidth if not compensated. Analytical, simulation, and experimental results are developed to illustrate the effectiveness of the new harmonic estimation and control techniques.**

I. Introduction

Three-phase active rectifiers, also known as PWM voltage-source converters (VSCs), or active front end (AFE) rectifiers, are widely used in industrial and commercial applications [1-3]. They represent a versatile solution for bidirectional power flow that is needed in applications such as cranes, elevators, centrifuges, and wind turbines. With the introduction of recent standards on limiting harmonic pollution of electrical power distribution systems, active rectifiers are being adopted more frequently in high-power electronic equipment to provide the interface to utility power lines. In addition, they are employed to minimize input voltage unbalances [4-6] and reduce dc link capacitance values [7-8]. This same power converter configuration is often chosen for use in active filters [9].

Common nonlinear loads can produce a large amount of harmonic current and cause the source voltages to be distorted [10-11]. The effects of harmonics can be overheating of transformers, cables, motors, generators and capacitors connected to the same power systems with the equipment generating the harmonics.

Passive, active, and hybrid filters are three methods to reduce harmonics in an industrial plant [9, 12]. Selective harmonic voltage compensation methods are described in [13, 14] for a power conditioner and dynamic voltage restorer (DVR). The disadvantage is that these harmonic elimination solutions require additional hardware and sensors at a higher cost. Very little has been published to date [15] regarding the use of active rectifiers to provide this harmonic compensation function.

In this paper, new cost-effective and computationally-efficient observer-based harmonic estimation and mitigation methods are introduced that provide attractive harmonic compensation capabilities for active rectifiers, making it unnecessary to introduce series or shunt passive or active filters to attenuate the harmonics. These new control techniques include compensation for delay effects caused by the digital signal processing that can significantly limit the current controller bandwidth if not compensated.

Since the frequencies of the 5th-, 7th-, and higher-order harmonics can easily exceed the current controller bandwidth, particularly in high power applications, the elimination of these harmonic disturbances imposes difficult control challenges. Analytical, simulation, and experimental results are developed to illustrate the effectiveness of the new harmonic estimation and control techniques. Experimental verification is accomplished using the dSpace controller on a 15hp adjustable-speed drive system.

II. System Description and Analytical Model

A modern four-quadrant adjustable-speed drive or uninterruptible power system equipped with an active rectifier is illustrated in Figure 1. The three-phase ac source is fed to a three-phase IGBT voltage-source converter. The input source and line impedance in phase a is L_{sa}, L_a and R_a, and it is assumed that the line impedances are equal in all three phases. The input EMI and harmonic filter is used to meet IEEE 519 and IEC 61000 standards.

The dc link voltage is smoothed by means of a dc link capacitor bank. The PWM output inverter consists of six IGBT switches (SW_{i1}-SW_{i6}) and anti-parallel diodes that synthesize ac voltage waveforms for motor or non-motor loads. The LC network (L_f, C_f) is used to filter the inverter switching ripple. It is also assumed that the output filter and loads are balanced. The input phase currents are measured for control purposes.

One important contribution of this paper is to accomplish the harmonic disturbance estimation and rejection in high-power systems with slower switching frequencies such as 5 kHz and limited current controller bandwidth. For instance, the frequencies of the 5th and 7th line harmonics that fall at 300 Hz and 420 Hz (for 60 Hz line frequency) can be comparable to the current

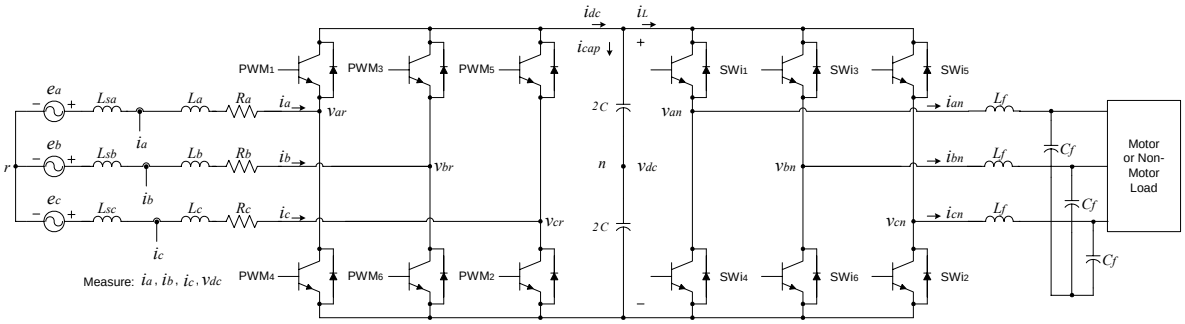

Figure 1. Four-quadrant ASD or UPS with active front-end (AFE) voltage source converter (VSC).

controller bandwidth of high-power converters, making harmonic elimination very challenging. The control algorithms are designed to overcome the detrimental impact of digital processing delay effects.

In this paper, an existing active rectifier model [16] is extended for control purposes by applying a different coordinate system to the power circuit in Figure 1, assuming a balanced three-phase system without a neutral connection. The three-phase quantities are transformed to *d-q* quantities in a rotating reference frame that is synchronous with the utility voltage. Eqs. (1-3) are the key circuit equations for the active rectifier using variables in the synchronous reference frame (designed by the ^{e} superscript). The inputs are the utility voltages (e^e_d, e^e_q) and the IGBT duty cycles (d^e_d, d^e_q), and the output is the dc link voltage (v_{dc}). The active rectifier voltage and current regulator implementations are based on this coordinate system and mathematical model.

$$L \cdot \frac{\mathrm{d}i^e_d}{\mathrm{d}t} + i^e_d \cdot R = e^e_d - d^e_d \cdot v_{dc} + \omega \cdot L \cdot i^e_q \tag{1}$$

$$L \cdot \frac{\mathrm{d}i^e_q}{\mathrm{d}t} + i^e_q \cdot R = e^e_q - d^e_q \cdot v_{dc} - \omega \cdot L \cdot i^e_d \tag{2}$$

$$C \frac{\mathrm{d}v_{dc}}{\mathrm{d}t} = \frac{3}{2}(i^e_d \cdot d^e_d + i^e_q \cdot d^e_q) - i_{dc} \tag{3}$$

III. Observer Model Formulation and Analysis of Source Harmonic Disturbances

A. Discrete Time Domain Observer Formulation

A module designed to estimate the state of a system from measurements of the outputs is called a state observer or simply an observer for that system. If the observer operates in an open-loop fashion without utilizing any actual measurements of the systems output, errors are likely to exist between the actual state values and their observed values. For improved performance, the difference between the measured output and the observed output is fed back to the observer to continuously correct the model and minimize the state variable divergence.

Figure 2 provides a block diagram representation of a closed-loop observer in the discrete *z*-domain. It is important to realize that the command input is applied in an identical way to both the plant and the observer equations.

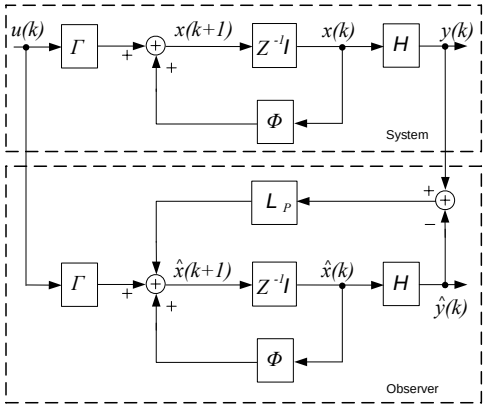

Figure 2. Block diagram of closed-loop observer system in discrete *z*-domain.

The system state space equations are expressed in the discrete *z*-domain [17] as follows:

$$X(k+1) = \Phi \cdot X(k) + \Gamma \cdot u(k) \tag{4}$$

$$Y(k) = H \cdot X(k) + J \cdot u(k) \tag{5}$$

$$\hat{X}(k+1) = \Phi \cdot \hat{X}(k) + \Gamma \cdot u(k) \tag{6}$$

$$\hat{X}(k+1) = (\Phi - L_p \cdot H) \cdot \hat{X}(k) + \Gamma \cdot u(k) + L_p \cdot Y(k) \tag{7}$$

Where ϕ, Γ, and H are the state-space matrices, $X(k)$ is the state variable vector, $u(k)$ is the input variable vector, and $Y(k)$ is the output variable vector in the discrete z-domain. $\hat{X}(k)$ represents the vector of observed state variables, and L_p is the observer gain matrix.

This observer formulation is referred to as a prediction estimator [17] since a measurement at time k results in an estimate of the state vector at time $k + 1$, which means the observed values are predicted one step ahead.

The dynamics of this system are determined by the characteristic matrix $[\Phi - L_p \cdot H]$. The goal is to place the observer poles such that this characteristic matrix represents an asymptotically stable system in which the observed state variables $\hat{X}(k)$ will converge toward the actual values $X(k)$ regardless of their initial values $\hat{X}(0)$.

B. Sinusoidal Disturbance Formulation

Consider a sinusoidal disturbance represented as:

$$x = A \cdot \sin(\omega t) \tag{8}$$

The 1st and 2nd derivatives of this sinusoidal function are:

$$\dot{x} = A \cdot \omega \cdot \cos(\omega t) \tag{9}$$

$$\ddot{x} = - A \cdot \omega^2 \cdot \sin(\omega t) = - \omega^2 \cdot x \tag{10}$$

Thus, the sinusoidal disturbance can be modeled in a state-space form as:

$$\begin{bmatrix} \dot{x} \\ \ddot{x} \end{bmatrix} = F_d \cdot \begin{bmatrix} x \\ \dot{x} \end{bmatrix} \tag{11}$$

Where

$$F_d = \begin{bmatrix} 0 & 1 \\ -\omega^2 & 0 \end{bmatrix} \tag{12}$$

In this investigation, the angular frequency of the sinusoidal disturbance can be at the fundamental, 5th, or 7th harmonic frequencies, etc. These disturbance terms will be added to the state-space formulations for forming the augmented system that is used for the observer development.

C. System Observer Model Formulation and Analysis

In place of using the actual state feedback for control, the state-space observer formulation is developed to apply the observed state vector for control purposes. It is important to structure the system such that the input u that is applied to the plant must also be applied to the observer as shown in Figure 2. Figure 3 shows the observer and plant system diagram including the disturbance w. The estimated disturbance is expressed as $\hat{w}$.

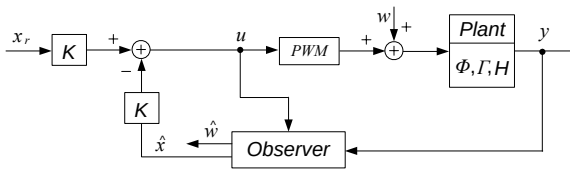

Figure 3. System block diagram including the disturbance w and closed-loop disturbance observer.

The disturbance w can cause the physical system to produce undesirable results such as harmonic distortion in the electrical distribution system. In order to minimize the effects of the disturbance w, the estimated disturbance will be used to compensate and cancel the actual disturbance. By driving the plant model in the observer with the same inputs that are applied to the actual plant, the estimation errors can be minimized.

Referring to Figure 3, the input signal delivered to the plant and observer is expressed as:

$$u = - K \bullet (\hat{x} - x_r) \tag{13}$$

Combining (4) – (7) and (13), one obtains the augmented state space matrices in (14) including both the physical system and observer state space variables.

$$\begin{bmatrix} x \\ \hat{x} \end{bmatrix}_{k+1} = \begin{bmatrix} \Phi & -\Gamma \bullet K \\ L_p \bullet H \Phi & -\Gamma \bullet K - L_p \bullet H \end{bmatrix} \bullet \begin{bmatrix} x \\ \hat{x} \end{bmatrix}_k + \begin{bmatrix} \Gamma \bullet K \\ \Gamma \bullet K \end{bmatrix} \bullet x_r + \begin{bmatrix} \Gamma \\ 0 \end{bmatrix} \bullet w_k \tag{14}$$

In the synchronous reference frame, the 5th and 7th harmonics become 6th order, so that the vector of the system state variables in this rotating reference frame is:

$$x = \begin{bmatrix} i_d & i_q & e_{d1} & e_{q1} & e_{d6} & \dot{e}_{d6} & e_{q6} & \dot{e}_{q6} \end{bmatrix}^T \tag{15}$$

Where

i_d: d-axis phase input current

i_q: q-axis phase input current

e_{d1}: source phase fundamental d-axis voltage

e_{q1}: source phase fundamental q-axis voltage

e_{d6}: source phase d-axis voltage due to the 5th and 7th harmonic voltages

e_{q6}: source phase q-axis voltage due to the 5th and 7th harmonic voltages

The error in the observer estimation is defined as:

$$\tilde{X} = X - \hat{X} \tag{16}$$

Substituting (4), (5) and (6) into (16), it can be determined that the dynamics of the resulting system are described by the observer error equation:

$$\tilde{X}(k+1) = \Phi \bullet \tilde{X}(k) \tag{17}$$

Using the approach outlined in this paper, a disturbance observer has been developed [19] for a three-phase 15 hp, 480 V voltage-source converter (VSC) with line impedance parameter values of R = 0.3 Ω and L = 5 mH (see (1) to (3)). The IGBT-based VSC switching frequency is assumed to be 5 kHz. The sampling rate for the discrete z-domain implementation has been set at 5 kHz, the same as the switching frequency.

Applying the observer formulations and gains calculated for this demonstration system [19], the observer results can be plotted to evaluate how well the observed variables $\hat{X}$ track their actual values X. Figure 4 shows that the predicted observer errors for the input currents exhibit very well-behaved decaying responses. It can be shown that all of the other observed state variables are predicted to track their corresponding actual values with similar dynamics.

Figure 5 shows the pole-zero map of the system including the harmonics disturbance observer. The 5th and 7th harmonic poles in the open-loop system are located on the unit circle of the z-domain, suggesting poor dynamic response. In the closed-loop system, the poles are moved inside the unit circle, reflecting the improved dynamic performance associated with the closed-loop configuration.

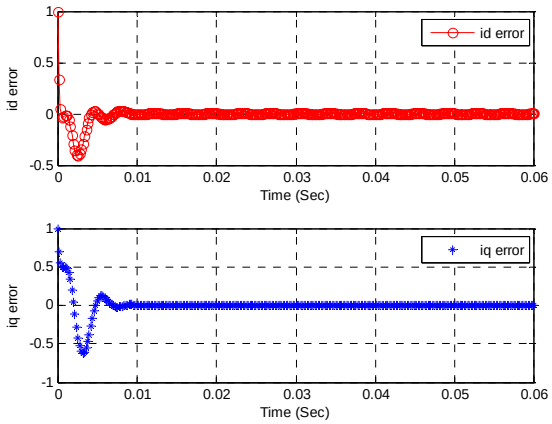

Figure 4. Predicted observer errors for the fundamental *dq* input currents (5 kHz sampling) in the synchronous reference frame.

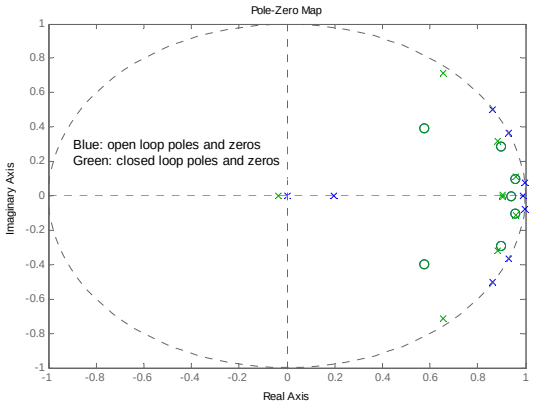

Figure 5. Controller pole-zero diagram in complex *z*-plane including the 5th and 7th harmonics observers (5 kHz sampling).

D. Observer Integration into Converter Controller

Figure 6 shows the observer-based controller block diagram for harmonics compensation in the synchronous reference frame. The output of the estimator block is the observed disturbance which is used to minimize the input current harmonics. The outer dc link voltage regulator produces the *d*-axis current reference signal for the inner current loop regulator, described in more detail in the next section. The input command vector u is fed to both the observer and to the plant itself.

The input disturbance includes 5th and 7th harmonic voltages that cause the physical system to produce undesirable input current harmonic distortions in the electrical distribution system. In order to cancel the effects of these disturbances, another summing junction is added as illustrated in Figure 6 so that the estimated disturbance vector $\hat{v}_{dq}$ from the observer model is added as an input to the plant. If the estimated disturbance $\hat{v}_{dq}$ asymptotically converges to the actual disturbance v_{dq} after the initial transients settle out, then $\hat{v}_{dq} = v_{dq}$ such that the plant is not disturbed.

IV. Digital Controller Implementation and Simulation Results

The active rectifier feedback control topology is implemented with an outer dc link voltage regulator which forms the *d*-axis current command to regulate the real power flow from the utility. The *q*-axis current

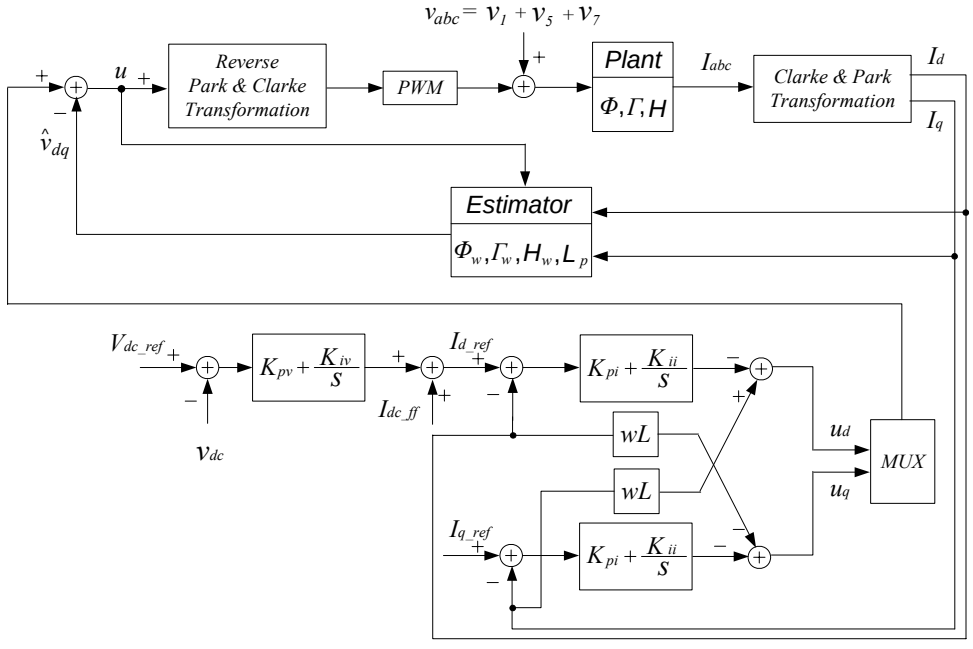

Figure 6. Block diagram of the observer-based control configuration including input current harmonic compensation.

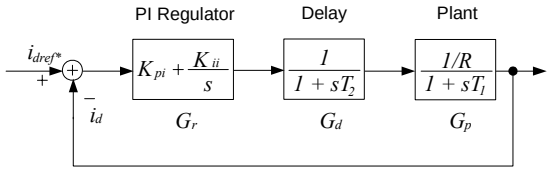

Figure 7. Block diagram of the closed-loop current regulator with PI controller.

command is used to control the input power factor. The combined *dq* current commands are the inputs to the inner-loop current regulators, as indicated in Figure 6. In addition, the dc link current is introduced as a feedforward term to the *d*-axis current command for improving the dynamic performance.

The controller has been designed using the Symmetrical Optimum (SO) technique [16], including the digital and process delay effects. The inner current controller block diagram is depicted in Figure 7. The individual transfer functions for the blocks in this figure are presented in (18-20). In the vicinity of the crossover frequency, the term $j\omega T_1 >> 1$ so that the plant transfer function can be approximated as shown in (20).

$$G_r = K_r \frac{1 + S\,T_r}{S\,T_r} = K_{pi} + \frac{K_{ii}}{S} \tag{18}$$

$$G_d = \frac{1}{1 + S\,T_2} \tag{19}$$

$$G_p = \frac{1/R}{S\,T_1} \tag{20}$$

Where

T_1: time constant of the input inductor (L/R)

T_2: computational and processing delay of 200 µs

$K_{pi} = K_r$: proportional gain of the PI regulator

T_r: time constant of the PI regulator

The frequency response locus is a semi-circle in the first quadrant [18] with a maximum phase at:

$$\omega_c = \omega_m = \frac{1}{\sqrt{T_r\,T_2}} \tag{21}$$

The maximum phase is expressed as:

$$\varphi_{0\,max} = \arctan\sqrt{\frac{T_r}{T_2}} - \arctan\sqrt{\frac{T_2}{T_r}} \tag{22}$$

Using the SO controller design technique, T_r is defined as:

$$T_r = a^2\,T_2, \qquad a > 1 \tag{23}$$

With a = 1.7, T_2 = 200 μs, R = 0.3 Ω, L = 5 mH, the frequency characteristics of the system including the delay are plotted in Figure 8. The current controller bandwidth and phase margin are 460 Hz and 30º, respectively.

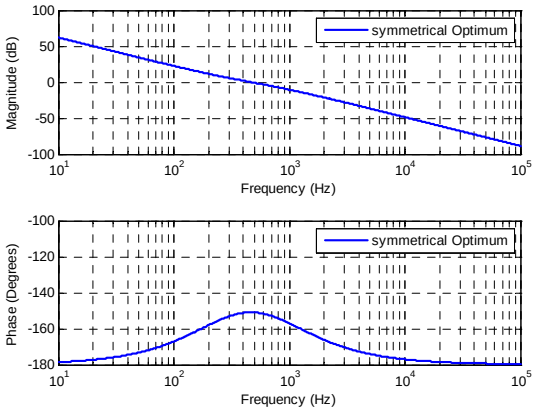

Figure 8. Bode diagram of the current controller based on the Symmetrical Optimum (SO) method (5 kHz).

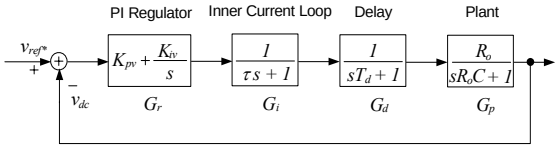

Figure 9. The plant and dc link voltage PI controller block diagram for the closed loop system with the delay element.

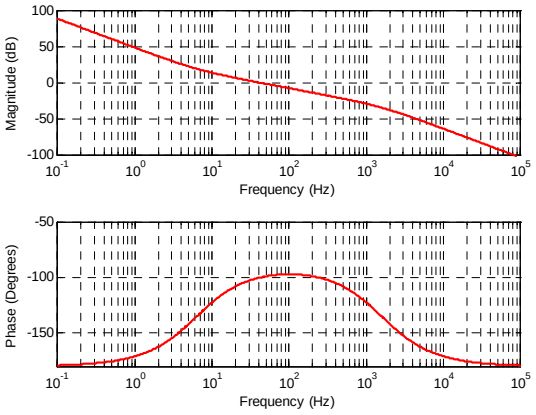

Figure 10. Bode diagram of the dc link voltage controller based on pole-zero cancellation method (5 kHz sampling).

Similarly, the dc link voltage control loop is modeled in Figure 9. The coefficients associated with the blocks in the dc link controller block diagram are summarized as:

K_{pv}: proportional gain of the PI regulator

K_{iv}: integral gain of the PI regulator

τ: time constant of the inner current controller loop

T_d: computational and process delay time

C: dc link capacitance value

R_o: dc link load resistance value

A pole-zero cancellation technique has been used to set the gains of the PI voltage regulator block. The resulting Bode diagram for the voltage regulator is shown in Figure 10. The dc link voltage controller bandwidth and phase margin are 40 Hz and 80º, respectively.

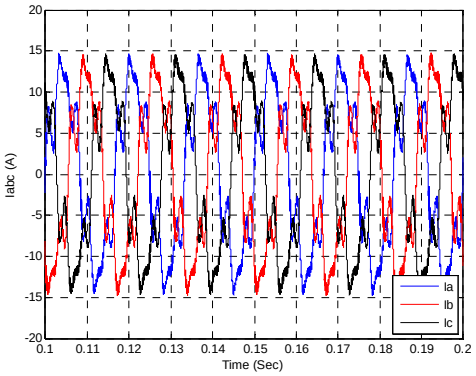

Figure 11. Simulated input current waveforms without observers resulting in 31.3% THD harmonic content.

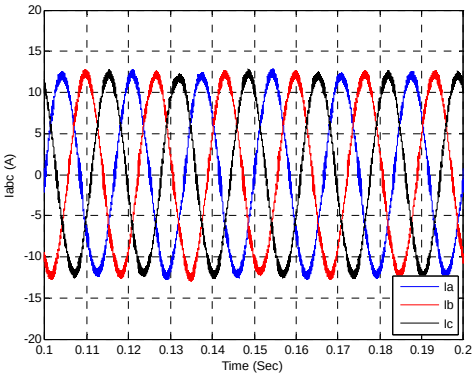

Figure 12. Simulated input current waveforms with observers resulting in 1.2% THD harmonic content.

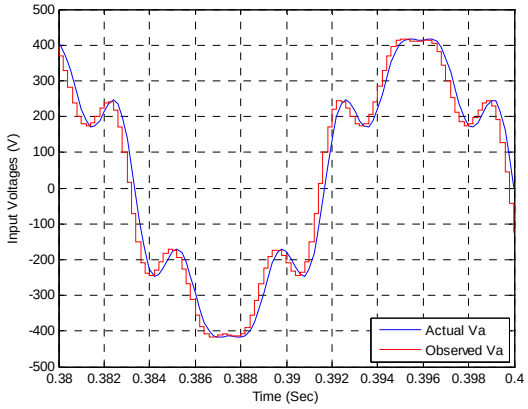

Figure 13. Zoomed-in view of simulated phase-A input voltage and the observed input voltage (5 kHz sampling).

A complete time-domain simulation with the proposed observer-based harmonic compensation has been conducted. A co-simulation platform that consists of PSIM for the power electronics circuits interfaced with Matlab/Simulink for the controller has been used for this analysis. The system parameters include: v_{dc} = 500 V, L_a = 5 mH, R_a = 0.3 Ω, switching frequency f_s = 5 kHz. The inverter in Figure 1 has been replaced in this simulation by a simpler equivalent resistive load R_L = 54 Ω.

Figure 14. View of experimental verification test equipment.

The input voltage disturbance for this simulation contains 5th and 7th harmonics with a total harmonic distortion (THD) of 12.3%. The resulting simulated input current waveforms shown in Figures 11 and 12 exhibit an impressive reduction of the harmonic content from 31.3% to 1.2% THD as a result of the observer-based compensation.

Figure 13 provides more insight into the operation of the observer by showing the simulated observed input voltage waveform compared to the "actual" input line voltage for the simulation. The observed voltage leads the actual voltage in order to compensate for the computational and process delay.

These simulation results indicate that the observer-based controller shows promise for almost completely eliminating the input current distortion caused by the input voltage disturbance and the digital delay.

V. Experimental Verification

The results from the analytical and simulation models presented in the previous sections have been verified experimentally using a laboratory testbed that includes a Semikron SKiiP 642GB 120 2D system (Figure 15). The test configuration includes a three-phase programmable power source which can be configured to produce various input power disturbances; a delta-wye step-up isolation transformer from 208V to 480V; an active front-end IGBT-based rectifier; a FPGA (Field Programmable Gate Array) interface board that includes current and voltage analog signal conditioning and fault protection circuitry; a dc load bank (54Ω); and a dSpace DS1103 rapid prototyping system. Figure 14 shows the actual lab setup.

The total input voltage THD was recorded as 12.3% with 10% 5th harmonic and 7% 7th harmonic components Figure 16 shows the measured input currents and dc link voltage (green trace) before and after applying the observer harmonics compensation, demonstrating the major reduction in harmonic content achieved with the controller.

Table I provides a comparison of the simulation and experimental current THD results that demonstrate very good agreement. The results illustrate the effectiveness of the observer-based harmonics compensation methods, even when severe input voltage distortions exist.

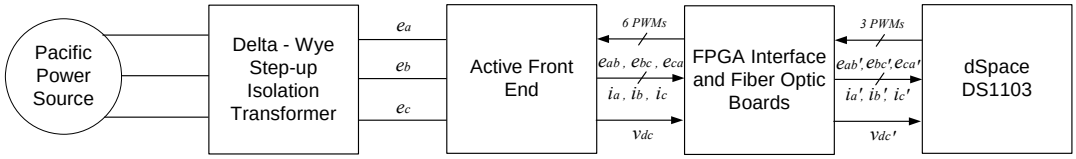

Figure 15. Block diagram of experimental test configuration.

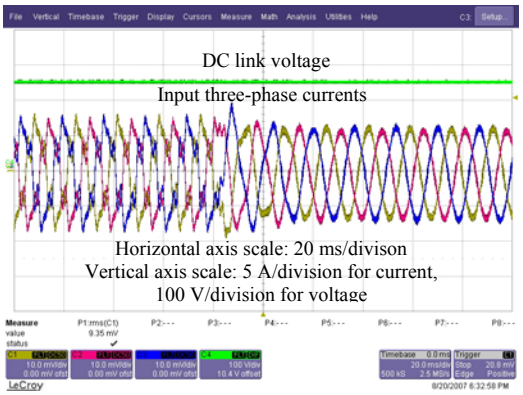

Figure 16. Experimental dc link voltage and input currents before and after compensation.

TABLE I. SIMULATION AND EXPERIMENTAL INPUT CURRENT THD COMPARISONS

Conditions	*Simulation THD*	*Experimental THD*
Without observers	31.27%	33.95%
With observers	1.15%	1.0%

VI. CONCLUSIONS

In this paper, new cost-effective sinusoidal disturbance estimation and harmonics elimination techniques are demonstrated to be very effective for high-power active front-end converters with slower PWM switching frequencies (e.g., 5 kHz) and limited current controller bandwidth. Since the active rectifier is in series with the source and the load, there is no need to add additional hardware for harmonic elimination. The new methods play two key roles: (a) the observed sinusoidal disturbances are used to cancel the actual disturbance effects; and (b) the observers make it possible to compensate the disturbance effects contributed by computational and digital processing delays.

In addition to the observer formulation and analysis, the inner current loop regulator and outer dc link voltage regulator designs have been analyzed including the effects of digital delays. A combination of simulation and experimental tests has demonstrated the effectiveness of the observer-based control scheme for suppressing the 5th and 7th harmonics in the line currents. If higher PWM switching frequencies are achievable in the front-end converter, the same algorithm can be readily extended to compensate the 11th and 13th harmonic components as well.

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