Analysis of Power Cycling Capability of IGBT Modules in a Conventional Matrix Converter

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Abstract — this paper analyzes the power cycling capability of IGBT modules in a conventional matrix converter used as a motor drive. The analysis is made under various condition for this topology, including low speed operation capability, high speed thermal and power cycle capability and etc. It was found that the power cycling Mean Time to Failure (MTTF) of IGBT in a matrix converter is low when the input and output frequency is close to each other or when the output frequency of the converter is low. As a result, the chip size of the conventional matrix converter may be larger than the other candidates. In the end of the paper, some guidance of designing a matrix converter for long term reliabilities is also discussed.

Keywords – power cycle, thermal cycle, conventional matrix converter, Mean Time to Failure (MTTF)

I. INTRODUCTION

The conventional matrix converter has been introduced to the world for over twenty years [1]-[5]. The pros and cons of this converter has been studied thoroughly and compared with the most widely used rectifier-inverter system, such as voltage/current quality, control schemes, efficiencies, reliabilities and etc. Comparing to the rectifier-inverter system, it has the following advantages: adjustable input power factor, bi-directional power flow, high quality input/output waveforms, and the possibility of a compact design due to the lack of large energy storage component [1]. Figure.1 shows a conventional matrix converter topology with back to back IGBT connection for each switching cell.

One disadvantage of the matrix converter is that it has much more numbers of power switches than other topologies. Since power semiconductor is one of the most costly components in a converter, it is beneficial to investigate the long term reliability and the sizing of the semiconductors used in the matrix converter. The end of life period of complex multi-chip modules is often defined by the thermo-mechanical failure mechanisms [6]-[9]. Two of most important failure schemes have been carried out – power cycling and thermal cycling capability. The power cycling capability defines wear out mechanisms of the bond-wire on the silicon chip. It is closely related the temperature cycling of the silicon die during the working condition. The thermal cycling capability classifies the failure mechanism of the solder layer where the substrate of the module is soldered on the base-plate. It is determined by the temperature variation of the base plate during the overall working condition.

II. CIRCUIT AND SYSTEM CONFIGURATION

In order to simplify the analysis, it is assumed that there is no input filter in the input of the matrix converter, thus, the following equations can be obtained from figure 1.

\[ L_s = 0; \quad C_f = 0; \quad V_{sx} = V_x; \quad i_{sx} = i_x \]  

Where

\[ L_s/C_f \] is the filter inductance/capacitance
\[ x: \] input phase name, can be phase A, B or C
\[ V_{sx}, i_{sx}: \] phase x source voltage and current

This paper investigates the power cycling capability of the IGBT being used in a matrix converter. Firstly, the losses calculation of the IGBT and diode under various conditions are studied. Then, a simplified electrical thermal cycle of a matrix converter is built up and the temperature cycles are studied under various condition. After that, the power cycle and thermal cycle capability of the IGBT under various operating condition are studied and compared. It is concluded that MTTF of the IGBT is low when the input and output frequency the matrix converter are close to each other or when the output frequency of the converter is low. As a consequence, a bigger IGBT module may have to be selected in order to guarantee an acceptable life expectation for a matrix converter.

Figure 1. The conventional matrix converter topologies
$V_x, i_x$: phase x converter side voltage and current

It is assumed that the input source voltage and output load are both balanced. The input voltage $V_s$ and output current $i_o$ are represented as:

$$
\dot{V}_s = \sqrt{3} \left( V_{sa} + \alpha \cdot V_{sb} + \alpha^2 \cdot V_{sc} \right) = V_m e^{i \omega t},
$$

$$
\dot{i}_o = \sqrt{3} \left( i_u + \alpha \cdot i_v + \alpha^2 \cdot i_w \right) = i_{om} e^{i \left( \omega t + \phi \right)},
$$

where, $\alpha = e^{i \frac{2 \pi}{3}}$, $V_m$ and $i_{om}$ are the per phase input voltage and output current amplitude respectively. $\omega$ and $\omega_o$ are the angular frequency of the input and output of the converter respectively. $\phi$ is the initial angle of the output current.

Another attractive character of the matrix converter is that a unity power factor can be achieved from the input side. Under this condition, the maximum voltage transfer ratio can be achieved. In this paper, it is assumed that the matrix converter is controlled under unity input power factor. Then, the following assumption can be made:

$$
\dot{V}_s = V_{om} e^{i \left( \omega t + \phi \right)}
$$

where, $\phi_v$ is the angle of the converter output voltage.

III. POWER LOSSES CALCULATION OF IGBT/DIODES

A three phase matrix converter is studied to drive an induction motor. The information of the matrix converter is defined as:

- Input line voltage: 480 Vac line to line
- Output frequency: 0 Hz ~ 60 Hz
- Switching frequency: 4 kHz,
- Output rated voltage: 415 Vac line to line voltage
- Rated current: 65 Arms
- IGBT module: FS100R12KE3

Due to the theory of the symmetry, only the IGBT/Diode losses of $S_{up}$, $S_{an}$, and $D_{up}$, $D_{an}$ in switch $S_{an}$ in figure 1 will be analyzed. The similar power losses curves can be derived for all other IGBTs and Diodes.

A. PWM control and duty ratio $d_1$, $d_2$ calculation

Various PWM control method has been discussed for the matrix converter. In this paper, a similar PWM method as shown in reference [11] will be discussed.

The basic commutation method as discussed in [11] separates the matrix converter into six intervals according to input source voltage as shown Figure 2 (a). In each PWM cycle, two portions are separated as shown in Figure 2 (b). In this figure, Duty ratio $d_1$ and $d_2$ are calculated from the input voltage synchronization angle and can keep the input current waveform to be sinusoidal. The detailed calculation of $d_1$ and $d_2$ are listed in Table I.

In each portion, the matrix converter can be simplified as a traditional inverter as described in Figure 2 (c). In this figure, $V_{sx}$ and $V_{sy}$ are the two of the three input phase voltages. The name of these two voltages in each portion and the corresponding commutation voltage are listed in Table I.

In this table: $\theta_a$, $\theta_b$, $\theta_c$ are the commanded current angle of phase A, B and C respectively, where

$$
\theta_a = \omega t ; \quad \theta_b = \omega t - \frac{2 \pi}{3} ; \quad \theta_c = \omega t - \frac{4 \pi}{3}
$$

![Figure 2](image-url)
B. Duty ratio $d_u, d_v$ and $d_w$ calculation

Duty ratios $d_u, d_v$, and $d_w$ are directly derived from the output voltage command vector. In this paper, a third order harmonics is added to the duty ratios to increase the voltage transfer ratio. The following duty ratio value can be defined:

$$d_u = \frac{1}{2} \left[ \cos(\omega_0 t + \phi_a) + \frac{1}{4} \cos(3\omega_0 t + 3\phi_a) \right]$$

$$d_v = \frac{1}{2} \left[ \cos(\omega_0 t + \phi_a) - \frac{2\pi}{3} \right]$$

$$d_w = \frac{1}{2} \left[ \cos(\omega_0 t + \phi_a) + \frac{2\pi}{3} \right]$$

(5)

where, $k$ is the voltage modulation index level of the converter and it is proportional to the ratio between output voltage and input voltage.

C. Duty ratio and conduction losses calculation of $S_{au}$

Combining Table I and Eq.4, the duty ratio of $S_{au}$ can be calculated as

$$d_{au} = \begin{cases} 
  d_u & -\frac{\pi}{6} \leq \theta_a < \frac{\pi}{6} \\
  d_2d_u & \frac{\pi}{6} \leq \theta_a < \frac{5\pi}{6} \\
  d_3d_u & \frac{5\pi}{6} \leq \theta_a < \frac{7\pi}{6} \\
  d_4d_u & \frac{7\pi}{6} \leq \theta_a < \frac{11\pi}{6} \\
  d_5d_u & \frac{11\pi}{6} \leq \theta_a < 2\pi \\
\end{cases}$$

(6)

According to Figure 1, the IGBT $S_{au}$ and $D_{au}$ conducts only when phase U current is positive and when switch $S_{au}$ turns on. On the other hand, $S_{an}$ and $D_{an}$ conduct only when phase U current is negative and when switch $S_{an}$ is turned on.

The conduction losses of $S_{au}$ and $D_{au}$ can be calculated by

$$P_c(S_{au}) = \begin{cases} 
  d_{au}(V_f + V_{Rd})i_u & i_u > 0 \\
  0 & i_u \leq 0 
\end{cases}$$

$$P_c(D_{au}) = \begin{cases} 
  0 & i_u > 0 \\
  d_{au}(V_f + V_{Rd})i_u & i_u \leq 0 
\end{cases}$$

(7)

where, $P_c(S_{au})$ and $P_c(D_{au})$ are the conduction losses of $S_{au}$ and $D_{au}$ respectively; $V_f$ and $R_f$ are the threshold voltage and slope resistance of IGBT $S_{au}$; $V_d$ and $R_d$ are the threshold voltage and slope resistance of Diode $D_{au}$.

Figure 3 (a) and (b) illustrates the average conduction losses of $S_{au}$ and $D_{au}$ under motoring and regenerating condition.

D. Switching losses of $S_{au}$ and $D_{au}$

In each portion, the matrix converter can be simplified as a three phase DC/AC inverter by keeping only six switches switching in each portion. Then, the switching losses can be generated for switching $S_{au}$ and $D_{au}$ when either $V_{sa}$ or $V_{sy}$ in Figure 2 (b) is represented by phase A. When input phase A appears to be $V_{sa}$ as shown in Figure 2 (b) and phase U current is positive. The switching losses will be generated on $S_{au}$. In contrary, when phase U current is negative, the switching losses will be generated on $D_{au}$.

Combining Table I, the switching losses of $S_{au}$ can be calculated as

$$P_s(S_{au}) = \begin{cases} 
  k_sV_{abc}i_u & \frac{9\pi}{6} \leq \theta_a < \frac{11\pi}{6} \text{ and } i_u > 0 \\
  k_s(V_{abc} + V_{sac})i_u & \frac{\pi}{6} \leq \theta_a < \frac{\pi}{6} \text{ and } i_u > 0 \\
  k_sV_{sac}i_u & \frac{\pi}{6} \leq \theta_a < \frac{3\pi}{6} \text{ and } i_u > 0 \\
  0 & \text{other cases} 
\end{cases}$$

(8)

where, $k_s$ is a switching losses constant for the IGBT. $E_{on}$ and $E_{off}$ are the turn on and off losses respectively. $V_n$ and $I_n$ are the nominal voltage and current for the IGBT module.

Similarly, the switching losses of $D_{au}$ can be calculated as

$$P_s(D_{au}) = \begin{cases} 
  k_dV_{abc}i_u & \frac{9\pi}{6} \leq \theta_a < \frac{11\pi}{6} \text{ and } i_u < 0 \\
  k_d(V_{abc} + V_{sac})i_u & \frac{\pi}{6} \leq \theta_a < \frac{\pi}{6} \text{ and } i_u < 0 \\
  k_dV_{sac}i_u & \frac{\pi}{6} \leq \theta_a < \frac{3\pi}{6} \text{ and } i_u < 0 \\
  0 & \text{other cases} 
\end{cases}$$

(9)

where, $k_d$ is the switching losses constant for the diode. $E_{rec}$ is the reverse recovery losses of the diode from the datasheet.
Figure 3. Losses of $S_{\text{aup}}$ and $D_{\text{aup}}$ in every input cycle (input frequency: 60Hz, Output current/frequency: 65Arms/59Hz, $k = 1.732$, unity input/output power factor).
(a): conduction losses at motoring condition, (b) conduction losses at regenerating condition, (c): switching losses at motoring condition, (d) switching losses at regenerating condition, (e): overall losses at motoring condition, (f) overall losses at regenerating condition.
E. Overall power losses of the Saup and Daup

Combining equation (7) ~ (9), the overall losses of Saup and Daup can be calculated as

\[ P(S_{aup}) = P_c (S_{aup}) + P_s (S_{aup}) \]

\[ P(D_{aup}) = P_c (D_{aup}) + P_s (D_{aup}) \]  

(10)

Figure 3 illustrates the average conduction, switching and overall losses of Saup and Daup under motoring and regenerating condition. In this figure, the losses are averaged in every input voltage source cycle (1/60Hz). The output load operates at 59Hz and rated current (65Arms).

Figure 4 further demonstrates the average power losses of the Saup Saun, Daup and Daun at various output power factor conditions. In this figure, all losses are averaged in every slip frequency between the input voltage source and output load frequency (1/(f_i-f_o)).

The following conclusion can be made from Figure 3 and 4.

- According to Figure 3 (a) and (b), the conduction losses of both switches in the matrix converter are modulated by a low frequency component. The frequency is approximately two times of the input and output slip frequency 2*(f_i-f_o).

- Figure 3 (c) and (d) demonstrates the switching losses of Saup and Daup at motoring and regenerating conditions. According to these two figures, the switching losses of the both switches are modulated by a low frequency component (f_i-f_o).

- From Figure 3 (c) and (d), the magnitude of the switching losses for both switches are similar to each other; however, a phase shift of the conduction losses and the switching losses can be seen between the motoring and regenerating condition of the converter.

- According to Figure 3 (e) and (f) and equation (10), it can be concluded that there are two low frequency components in the overall losses for both switches.

- According to Figure 3 (e) and (f), the overall losses of Saup are much higher at motoring condition than that in the regenerating condition. In comparison, the overall losses of Daup are much lower at motoring condition.

- Figure 4 demonstrates that the conduction losses of Daup and Saun are much lower at motoring condition and losses during the regenerating condition.

- If the characters of the load are defined, it is possible to size the Saup, Saun, Daup, and Daun appropriately to achieve the best price and performance ratio. For example, if a motoring load is designed, then the size of Saup and Daun can be much bigger than that of Saun and Daup.

- However, it is not possible to eliminate the number of switches as the dual bridge matrix converter shown in reference [13]. Under that case, as few as 9 switches are needed.

IV. THERMAL MODELLING OF THE MATRIX CONVERTER SYSTEM

A. Thermal Modelling of the Diode and IGBT chips

The thermal modeling of the Diode and IGBT chips in one heat-sink has been discussed by many articles. Figure 5 shows a simplified thermal system for the matrix converter systems. In this figure, Z_{jc} and Z_{jcd} are the thermal impedance between the junction and case layer of the IGBT and diode chip respectively. Z_{ch} and Z_{chd} are the thermal impedance between the case layer and the heat sink. The similar thermal impedance value as shown in [12] are applied. R_h and C_h are the thermal resistance and capacitance of the heat-sink.

The thermal resistance and time constants of the diode and IGBT chips are listed in Table. II. The thermal resistance and
time constants of the heat-sink are selected as $R_h = 0.06 \text{ k}/\text{w}$ and a time constants of $\tau_h = R_h C_h = 120 \text{ s}$

![Figure 5](image)

**Figure 5.** Simplified thermal system of the matrix converter system. (a) overall thermal network model, (b) thermal impedance between the junction and case layer of one chip.

<table>
<thead>
<tr>
<th>TABLE II. THERMAL IMPEDANCE OF THE TESTED IGBT/DIODE</th>
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<tbody>
<tr>
<td>Segments</td>
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<tr>
<td>Ri: (K/W)</td>
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<tr>
<td>$\tau_i$: (s)</td>
</tr>
<tr>
<td>Rd: (K/W)</td>
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<tr>
<td>$\tau_d$: (s)</td>
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**B. Junction temperature of IGBT and Diode under various input/output frequencies**

With all above analysis, the junction temperatures of the IGBT and Diode chips in switch $S_{au}$ under different output frequency are plotted.

From Figure 6 (a), the input and output frequency of the converter has only 1Hz difference. A big temperature variation with a low frequency on each IGBT and Diode chips was shown when the input and output frequency of the converter is close to each other. Similarly, from Figure 6 (c), a low frequency variation can also be seen when the converter operates under low output frequency.

![Figure 6](image)

**Figure 6.** Junction temperature profile of the matrix converter under various output frequency. (a) input frequency: 60Hz, switching frequency: 4kHz; (b) output frequency: 59Hz, (c) output frequency: 1Hz
V. POWER CYCLING MTTF CALCULATIONS

A. Failure Mode of the IGBT/Diode Chips and MTTF estimation of the module

Studies have shown that power cycling of the IGBT caused by the low cycle fatigue is one of the dominant failure mechanisms higher power IGBT multi-chip modules [6][7][8][9][10]. The driving force of the mechanism is the mismatch in the thermal expansion coefficients of aluminum and silicon. During operation, the junction temperature of each chip may increase or decrease quickly for more than 60°C. This produces a differential elongation of the bond-wire in respect to the substrate, and it results into a plastic flow of the wire material. Especially at the periphery of the bonding interface where the shear stress reaches its maximum strength.

A typical model of predicting the number to failure of the IGBT based power cycling capability has been studied in reference [9] as

\[ N_f(T_m, \Delta T_j) = A \cdot \Delta T_j^{m} \cdot \exp\left(\frac{Q}{R \cdot T_m}\right) \]  

(11)

where, \(A, \alpha, Q, R\) are all constant and is decided by way the module is built up, \(\Delta T_j\) is the variation of the junction temperature, \(T_m\) is the mean junction temperature in one power cycle.

Based on the reliability data from the supplier, the following extracted values are used in this paper.

\[ A = 654.8 \]
\[ \alpha = -7.801 \]
\[ \frac{Q}{R} = 1.378 \times 10^4 \, ^\circ\text{C} \]  

(12)

To predict the MTTF of the module under power cycling capability, one widely used method is called linear accumulation of the thermal cycle fatigue damage models as shown in reference [8]. Under this assumption, the mean time to failure (MTTF) of the bond-wires for a silicon chip can be estimated as:

\[ \text{MTTF} = \frac{T}{\int N_f(T_m(t), \Delta T_j(t)) \, dt} \]  

(13)

where \(T\) is the unit cycle time period of the load to be studied, \(N_f(T_m(t), \Delta T_j(t))\) is the number of power cycles of the silicon die with an average junction of \(T_m(t)\) and temperature variation of \(\Delta T_j(t)\) in each period. \(N_f(T_m(t), \Delta T_j(t))\) is the number of cycles to failure of the chip under the same temperature condition.

Detailed description of how equation (13) is derived is beyond the scope of this paper and will not be discussed.

Due to the limitation of the laboratory setup, the MTTF study of matrix converter is not shown; however, the effectiveness of this approach has been verified successfully in a separate paper [14] to predict the lifetime of IGBT in a DC/AC inverter system by the same author.

B. Power Cycling MTTF Estimation of the Module under full load conditions

Based on the analysis above, the MTTF estimation of the IGBT module under full load is studied by combining equation (11) and (13). During the study, it is assumed that the converter operates at rate current 65Arms with a fixed load power factor (0.9). The output frequency of the converter is adjusted from 0.25Hz to 57.75Hz. The average temperature \(T_m\) and temperature variation \(\Delta T_j\) of each frequency is simulated under Simpleror program and calculated in excel spreadsheet.

Figure.7 further shows the MTTF estimation of \(S_{sup}\) and \(D_{un}\) under the studied condition. From this figure, it can be found that the matrix converter has a much shorter life when the output frequency is close to input frequency or when the output frequency is low.

C. Power Cycling MTTF Estimation of the Module under Repeated Overload Operating Conditions

The similar studies are made for the converter at repeated overload mode. Under this condition, the converter operates 50% overload (output current: 97.5Arms) for every 3 seconds and rated load (output current: 65Arms) for 57 seconds repeatedly as shown in Figure.8 (a).

Figure.8 (b) shows the MTTF estimation of \(S_{sup}\) and \(D_{un}\) under the studied condition. From this figure, it can also be found that the matrix converter has a much shorter life when the output frequency is close to input frequency or when the output frequency is low.

From Figure.8 (b), the MTTF of the IGBT and Diode are very limited under overloaded condition. For example, when the output frequency is less than 10Hz, the life of the \(S_{sup}\) and \(D_{un}\) is much less than 1 year. As a result, both IGBT and diode chips may have to be oversized in order to achieve an acceptable life.

D. Discussion

Based on above analysis, the following conclusions can be obtained.
VI. CONCLUSION

This paper calculates the losses and MTTF of the IGBT and Diode chips under matrix converters. The following conclusions can be made.

- A higher temperature variation on the silicon chips can be seen when the output of the converter is low or when the input and output frequency are close to each other.
- The MTTF of the silicon chips are reduced under above two conditions. Thus, sizing of the silicon has to be properly made to avoid earlier failure of the converter.
- This power cycling characteristic of matrix converter may further increase the silicon sizes and result in a higher silicon cost than other topologies.
- To optimize the silicon size of the matrix converter, the characteristics of the load has to be closely studied.
- When the converter output frequency is high and approaching the input frequency, the MTTF might be able to be improved by selecting a proper commutation scheme for the matrix converters. This is beyond the scope of this paper and will not be discussed.

VII. REFERENCES