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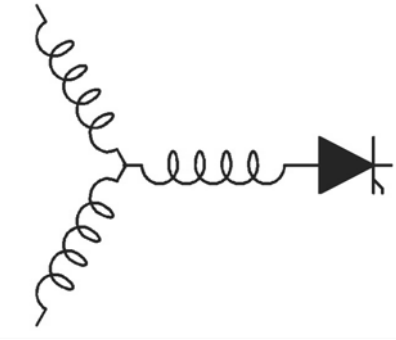

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Comparison of IGBT Cycling Capabilities for Different AC/AC Topologies

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***Abstract*—This paper analyzes the insulated gate bipolar transistor (IGBT) power cycling capability for a dual-bridge matrix converter (DBMC) used as a motor drive and compares the result with the traditional dc/ac inverter and the conventional matrix converter (CMC). Two pulsewidth modulation (PWM) control methods for the DBMC are investigated. One is called zero-current PWM (ZCPWM), which allows zero current commutation of the rectifier side switches. The other is named zero-voltage PWM (ZVPWM), which generates zero-voltage switching in the inverter IGBT. It is found that the DBMC under the ZVPWM method shows much higher power cycling capabilities in the IGBT than that of the ZCPWM and the other two topologies. Moreover, by appropriately selecting the sequence of the ZVPWM and ZCPWM methods, the DBMC shows overall advantages on the sizing of the IGBT and the balancing of the thermal system. It is also shown that the IGBT applied in the DBMC inverter is easier to operate under higher switching frequency conditions.**

***Index Terms*—Mean time to failure, power cycle, zero-current switching, zero-voltage switching.**

I. Introduction

THE dual-bridge matrix converter (DBMC) is a relatively new concept [1]–[5] developed through the years. Compared to the conventional matrix converter (CMC) [6], the DBMC possesses the same high quality performance, including near sinusoidal input/output waveforms, an adjustable input power factor, and a compact system design due to the absence of large energy storage components. It also has a number of other advantages, including safe commutation, reduced number of switches, simple clamp circuit, easier operation with multimotor configurations [5], and etc. With all these advantages, the DBMC is suitable to be used for variable frequency conversion applications, including distributed electrical power systems or many onboard electrical power generation systems. The freedom of selecting input and output frequencies helps operate the system with lower volume, weight, and cost.

One disadvantage of the matrix converter is that it has a much higher number of power switches. Since power switches are some of the most costly components in a converter, it is beneficial to investigate the long-term reliability and sizing of these components. The end of the life period of complex multichip modules is often defined by thermomechanical failure mechanisms [8]–[10]. Power cycling capability is one of most important failure schemes. It defines the wear out mechanisms of the bond wire on the silicon chip. In [10]–[12], it was found out that the lifetime of the bond wire for the chip might be very short if the temperature variation on the insulated gate bipolar transistor (IGBT) is too high. Thus, investigating the power cycling mean time to failure (MTTF) of the IGBT is important for the design and application of a converter.

Papers have been published to analyze the power cycling capabilities of traditional inverter [11] and CMC [12]. Reference [11] shows that the dc/ac inverter has a very low power cycling MTTF at low speed. It also verified that more than seven times of lifetime improvement can be seen while changing the inverter switching frequency from 8 kHz to 4 kHz. In [12], it is concluded that the power cycling MTTF of an CMC is very limited at low speed and when the input/output frequency are close to each other.

This paper analyzes the power cycling MTTF of IGBT modules used in a DBMC and compares the result with the dc/ac inverter and the CMC. Two pulsewidth modulation (PWM) control methods have been investigated. The first is called zero-current PWM (ZCPWM) method, where all line-side switches commutate under zero current. The second method, which has been discussed in [3], is called zero-voltage PWM (ZVPWM), where all load side switches commutate under zero voltage. It was found from this paper that these two PWM methods demonstrate much different power cycling MTTF value sfor the inverter IGBT. Moreover, the power cycling MTTF of the DBMC can be optimized by appropriately selecting the ZCPWM and ZVPWM method.

This paper is organized as follows. First, the ZCPWM and ZVPWM methods of DBMC are introduced. Second, the power losses of both the IGBT and the diode are calculated and compared. Third, the junction temperature variations of the IGBTs under both PWM methods are studied. Finally, the power cycling MTTF of the inverter IGBT in DBMC are calculated and compared with a dc/ac inverter and a CMC. The advantages of DBMC over the other two topologies will be summarized at the end of this paper.

II. Circuit and System Configuration

To simplify the analysis, it is assumed that there is no input filter in the input of the DBMC. The following equations can be

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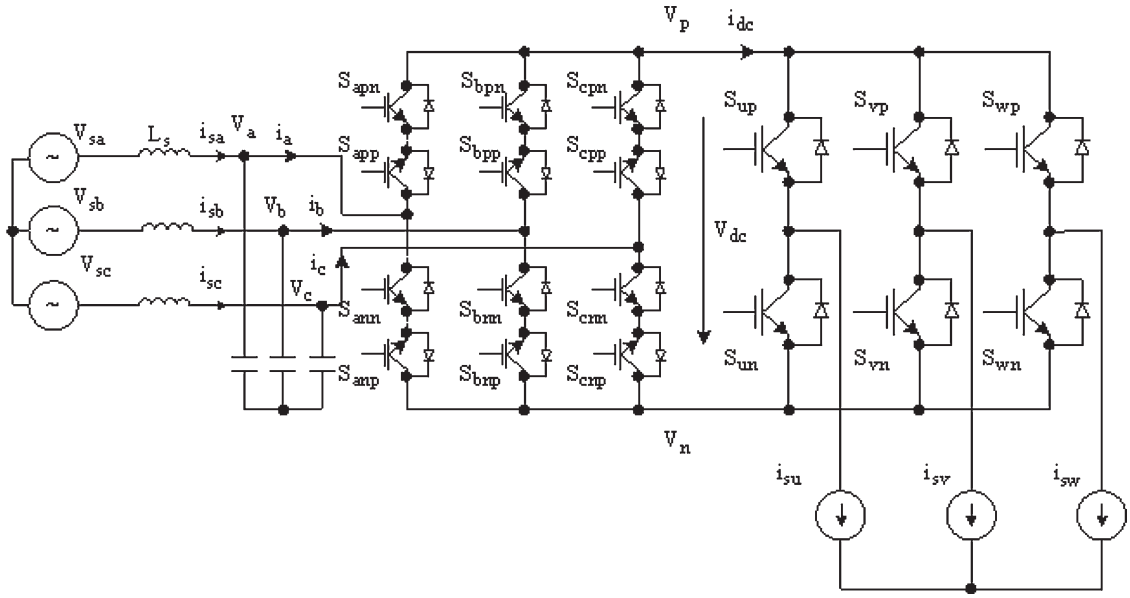


Fig. 1. 18-switch DBMC topology.

obtained from Fig. 1:

$$L_s = 0 \quad C_f = 0 \quad V_{sx} = V_x \quad i_{sx} = i_x \tag{1}$$

where

L_s/C_f	filter inductance/capacitance;
x	input phase name (can be phase A, B or C);
V_{sx}, i_{sx}	phase x source voltage and current;
V_x, i_x	phase x converter-side voltage and current.

It is also assumed that the input source voltage and output load are balanced. The input voltage $\vec{i}_o$ and output current $\vec{i}_o$ are represented as

$$\vec{V}_s = \sqrt{\frac{2}{3}}(V_{sa} + \alpha \cdot V_{sb} + \alpha^2 \cdot V_{sc}) = V_m e^{j\omega_i t}$$
$$\vec{i}_o = \sqrt{\frac{2}{3}}(i_u + \alpha \cdot i_v + \alpha^2 \cdot i_w) = i_o e^{j(\omega_o t + \varphi_i)} \tag{2}$$

where $\alpha = e^{j2\pi/3}$; V_m and i_o are the per phase input voltage and output current amplitude, respectively; ω_i and ω_o are the input and output angular frequency of the converter, respectively; and φ_i is the initial angle of the output current.

Another attractive characteristic of the DBMC is that a unity input power factor can be achieved with the maximum voltage transfer ratio. In this paper, it is assumed that the DBMC is controlled under the unity input power factor. Then,

$$\vec{i}_s = \sqrt{\frac{2}{3}}(i_a + \alpha \cdot i_b + \alpha^2 \cdot i_c) = i_m e^{j\theta_a} = i_m e^{j\omega_i t}$$
$$\vec{V}_o = V_{om} e^{j(\omega_o t + \varphi_v)} \tag{3}$$

where $V_{\rm om}$ is the output voltage of the converter and φ_v is the angle of the output voltage.

To make comparisons, the same rating of the IGBT and the inverter, as shown in [11], [12], are studied for the DBMC:

input line voltage	480 Vac line to line;
output frequency	1 Hz $\sim$ 60 Hz;
switching frequency	4 kHz;
output-rated voltage	415 Vac line-to-line voltage;
rated current	65 Arms;
IGBT module	FS100R12KE3;
motor power factor	0.85.

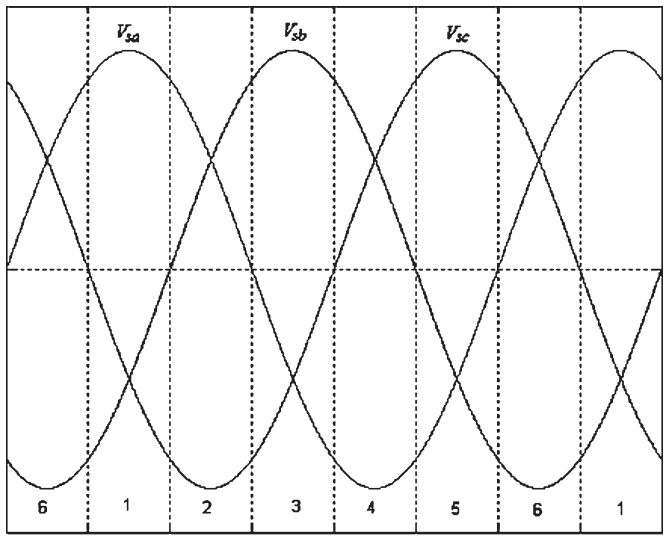


Fig. 2. Line-side intervals definition for the rectifier.

III. Duty Ratio Calculation of the DBMC

A. Nonzero Vector and its Duty Ratio of the Rectifier

A similar duty ratio calculation method as discussed in [1], [3] will be applied in this paper. It separates the DBMC into six intervals as shown in Fig. 2. In each PWM cycle, two nonzero vectors of the rectifier are generated in each interval. Table I shows the dc-link bus voltage and the nonzero vectors of the rectifier in each interval and their corresponding duty ratios.

TABLE I
NON ZERO VECTORS AND THEIR DUTY RATIOS OF LINE-SIDE CONVERTER IN EACH PWM CYCLE

interval	Non-Zero V_{r1}				Non Zero V_{r2}			
	d_{r1}	V_p	V_n	V_{dc1}	d_{r2}	V_p	V_n	V_{dc2}
1	$\lvert\cos\theta_b\rvert$	V_{sa}	V_{sb}	V_{sab}	$\lvert\cos\theta_c\rvert$	V_{sa}	V_{sc}	V_{sac}
2	$\lvert\cos\theta_b\rvert$	V_{sb}	V_{sc}	V_{sbc}	$\lvert\cos\theta_a\rvert$	V_{sa}	V_{sc}	V_{sac}
3	$\lvert\cos\theta_c\rvert$	V_{sb}	V_{sc}	V_{sbc}	$\lvert\cos\theta_a\rvert$	V_{sb}	V_{sa}	V_{sba}
4	$\lvert\cos\theta_c\rvert$	V_{sc}	V_{sa}	V_{sca}	$\lvert\cos\theta_b\rvert$	V_{sb}	V_{sa}	V_{sba}
5	$\lvert\cos\theta_a\rvert$	V_{sc}	V_{sa}	V_{sca}	$\lvert\cos\theta_b\rvert$	V_{sc}	V_{sb}	V_{scb}
6	$\lvert\cos\theta_a\rvert$	V_{sa}	V_{sb}	V_{sab}	$\lvert\cos\theta_c\rvert$	V_{sc}	V_{sb}	V_{scb}

B. Inverter-Side Duty Ratio Calculation

Inverter-side duty ratios $d_u d_v$ and d_w are directly derived from the output voltage command. A third-order harmonic is added to the duty ratios to increase the voltage transfer ratio

$$\begin{aligned} d_u &= \frac{1}{2} + \frac{k}{2}\left[\cos(\omega_o t + \varphi_v) - \frac{1}{4}\cos(3\omega_o t + 3\varphi_v)\right] \\ d_v &= \frac{1}{2} + \frac{k}{2}\left[\cos\left(\omega_o t + \varphi_v - \frac{2\pi}{3}\right) - \frac{1}{4}\cos(3\omega_o t + 3\varphi_v)\right] \\ d_w &= \frac{1}{2} + \frac{k}{2}\left[\cos\left(\omega_o t + \varphi_v + \frac{2\pi}{3}\right) - \frac{1}{4}\cos(3\omega_o t + 3\varphi_v)\right] \end{aligned} \tag{4}$$

where k is the modulation index of the inverter. It is proportional to the ratio between the output and input voltage

IV. ZERO VECTORS AND ZCPWM/ZVPWM

The DBMC is a converter connecting a current source rectifier and a voltage source inverter directly. When either the rectifier or the inverter has zero vectors, the DBMC generates zero vectors. Under zero vector condition, both zero current vectors in the rectifier and zero voltage vectors to the inverter-side are generated.

There are three types of zero vectors in DBMC.

- Type I: Both rectifier and inverter stays at zero vector condition as shown in Fig. 3(a): The current in the line-side IGBTs and the voltage in the inverter-side IGBTs are all zero. Under this condition, changing the switching states of an IGBT generates either zero voltage switching at the inverter-side or zero current switching at the rectifier side. After the transition, the DBMC still remains at zero vector.
- Type II: Only the inverter-side remains at zero vector as shown in Fig. 3(b). Under this type of vectors, the current in all rectifier side IGBT are zero, and changing the switching state of the rectifier generates zero current switching losses. The voltage stress of inverter IGBTs are not zero.
- Type III: Only the rectifier side remains at zero vector as shown in Fig. 3(c). Under this condition, the voltage stress across all inverter-side IGBTs are zero, and changing the switching state of the inverter generates zero voltage switching losses. The currents of the rectifier IGBTs are not all zero.

Proper selection of the zero vector type helps relocate the switching losses between the rectifier and the inverter [3]. Fig. 4(a) shows the well-known ZCPWM method of the DBMC. In this case, the rectifier side IGBT only switches at zero inverter vectors. Only type I and II zero vectors exist in the PWM sequence.

Fig. 4(b) shows an example of how the inverter-side ZVPWM is generated. In this figure, the duty ratios of nonzero vectors are the same as Fig. 4(a), except for a different commutation sequence. The inverter-side IGBT only switches when the rectifier side vector is zero as shown in Table II for each interval. Under ZVPWM, only type I and III zero vectors exist in the PWM sequence.

For both Fig. 4(a) and (b), type II and III zero vectors are only used to generate the expected switching losses during the transition between nonzero and zero vectors. The DBMC always stay under type I zero vectors after the transition to minimize conduction losses and to relocate switching losses.

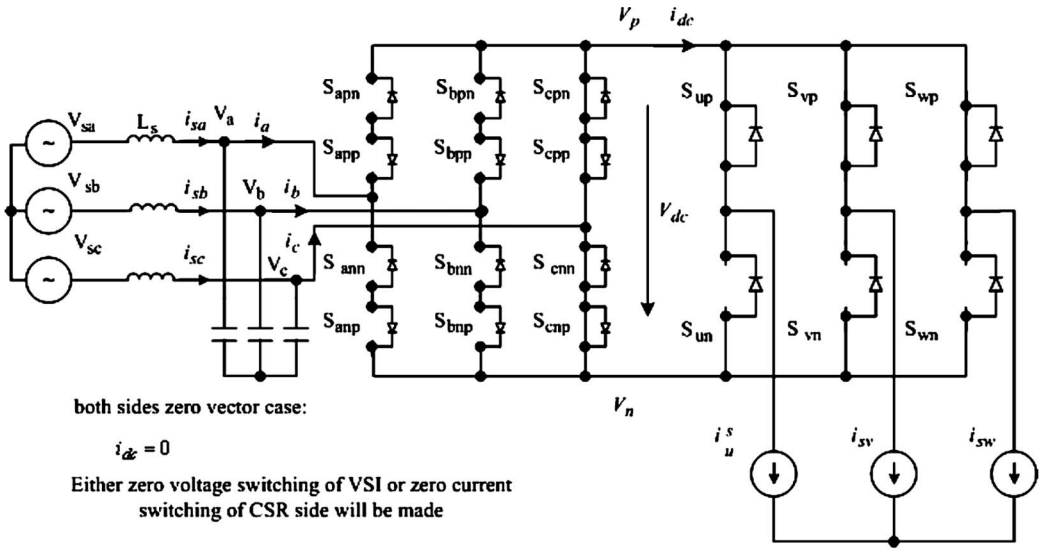
V. POWER LOSSES AND JUNCTION TEMPERATURE PROFILE COMPARISON OF THE TWO METHODS

During the operation, the rectifier side IGBT operates at line frequency (60 Hz). The fundamental time period is much lower than the time constant of the IGBT junction to case thermal impedance. The temperature variation of the junction temperature is low. The power cycling MTTF of the rectifier side IGBT is long [11] and can be neglected. Thus, only the inverter-side losses and the junction temperatures will consequently be analyzed.

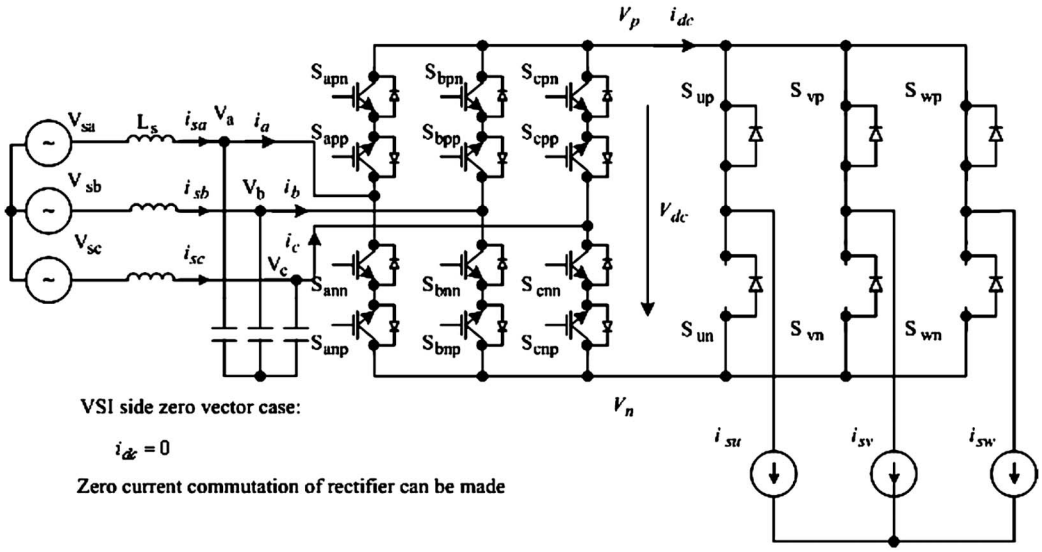
A. Conduction Losses Calculation

The conduction losses of the two PWM methods are the same as the dc/ac inverter. According to [12], the on-state voltage drop of the IGBT $V_{\rm ce}(t)$ and diode chip $V_d(t)$ for one module can be approximated by the following equations from the datasheet:

$$\begin{aligned} V_{ce}(t) &= V_t + R_t \cdot i(t) \\ V_d(t) &= V_d + R_d \cdot i(t) \end{aligned} \tag{5}$$



(a)



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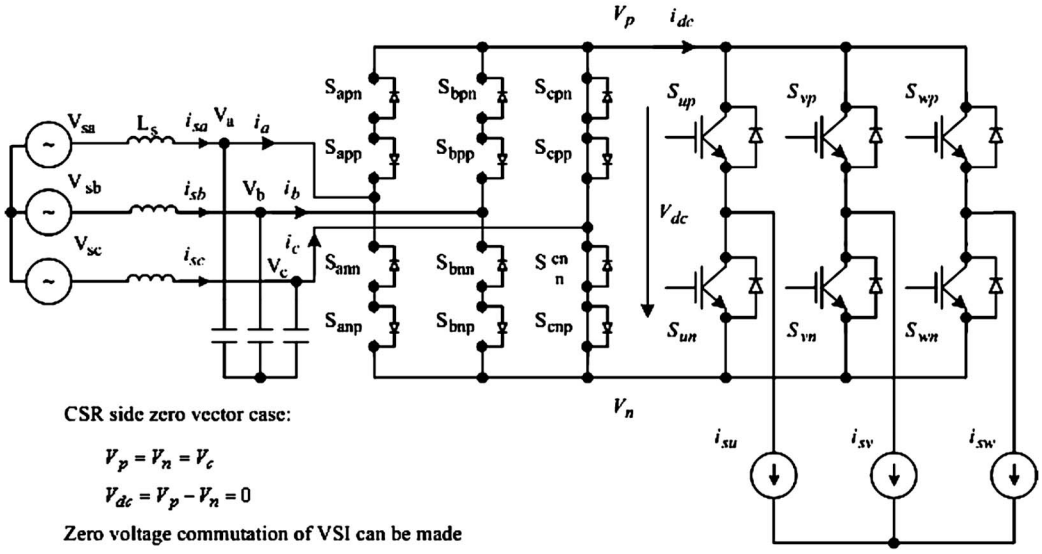

(c)

Fig. 3. Zero vector of DBMC (a) Type I: zero vector on both side vector; (b) Type II: inverter-side zero vector; and (c) Type III: rectifier side zero vector.

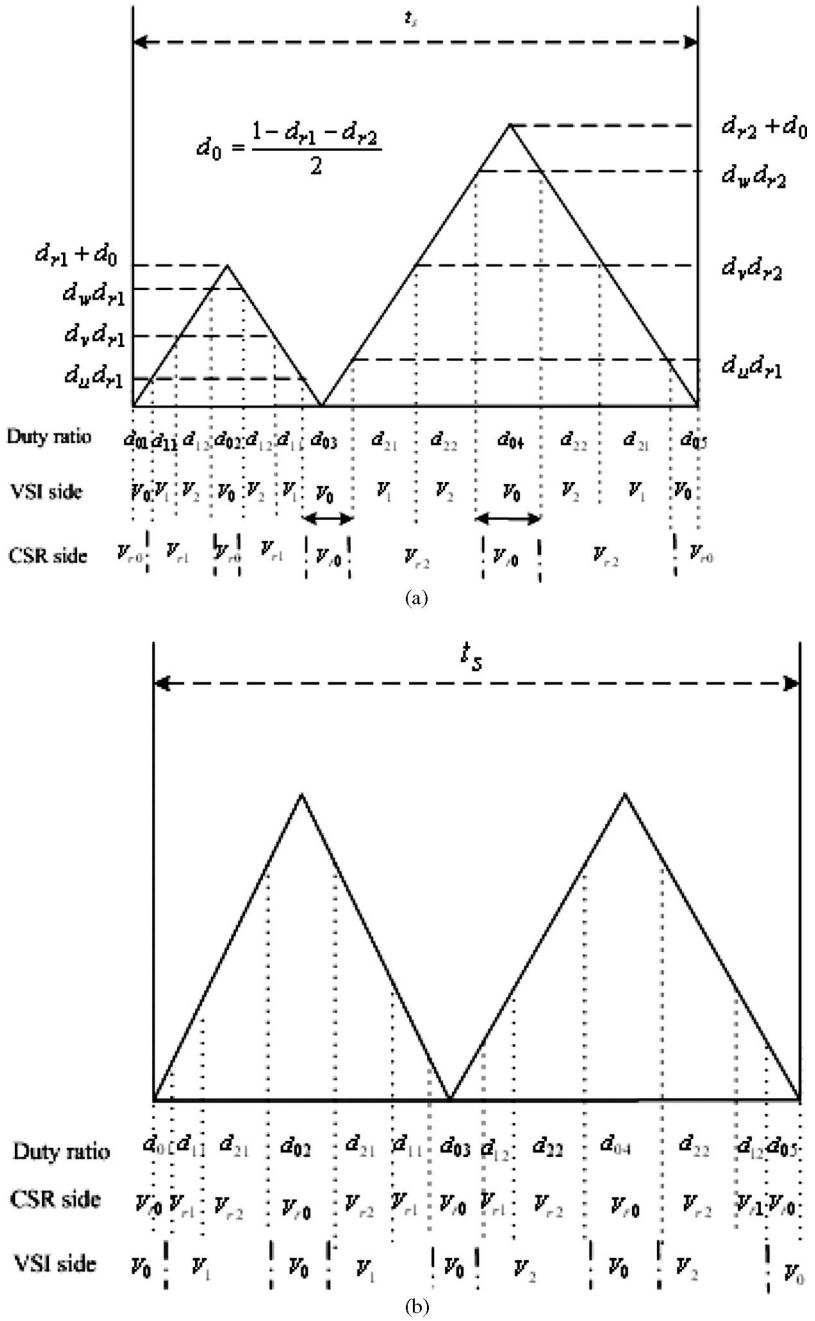

Fig. 4. ZCPWM and ZVPWM: (a) rectifier side ZCPWM and (b) inverter-side ZVPWM.

where V_t and V_d are the approximate voltage drop of the IGBT and diode chip at near zero forwarding current while R_t and R_d are the slope resistance of the IGBT and diode chip, respectively.

The average conduction losses of $S_{\rm up}$ and $d_{\rm up}$ under one switching cycle can be calculated by

$$P_c(S_{\rm up}) = \begin{cases} d_u(V_t + R_t i_u) i_u, & i_u > 0 \\ 0, & i_u \le 0 \end{cases}$$
$$P_c(D_{\rm up}) = \begin{cases} 0, & i_u > 0 \\ d_u(V_d + R_d i_u) i_u, & i_u \le 0 \end{cases} \quad (6)$$

where $P_c(S_{\rm up})$ and $P_c(D_{\rm up})$ are the conduction losses of $S_{\rm up}$ and $d_{\rm up}$, respectively.

The average losses of the inverter IGBT (PI) and diode (PD) under one cycle of the inverter output fundamental cycle can be simplified as shown in [13]

$$PI_c = \left(\frac{1}{2\pi} + \frac{k\cos\varphi_o}{8}\right) V_t I_m + \left(\frac{1}{8} + \frac{k\cos\varphi_o}{3\pi}\right) R_t I_m^2$$
$$PD_c = \left(\frac{1}{2\pi} - \frac{k\cos\varphi_o}{8}\right) V_d I_m + \left(\frac{1}{8} - \frac{k\cos\varphi_o}{3\pi}\right) R_d I_m^2. \quad (7)$$

B. Switching Losses Calculation of the Two PWM Methods

According to previous analysis, the switching losses of the inverter IGBT/diode are only generated with the ZCPWM

TABLE II
RECTIFIER SIDE ZERO VECTORS UNDER EACH INTERVAL FOR ZVPWM

Interval	1	2	3	4	5	6
V_{sx}	V_{sa}	V_{sc}	V_{sb}	V_{sa}	V_{sc}	V_{sb}
V_{sy}	V_{sa}	V_{sc}	V_{sb}	V_{sa}	V_{sc}	V_{sb}

method. Under this condition, the average switching losses of $S_{\rm up}/d_{\rm up}$ in one switching cycle can be simplified as

$$P_s(S_{\rm up}) = \begin{cases} f_s \cdot (E_{\rm on} + E_{\rm off}) \cdot \frac{(V_{dc1}+V_{dc2})\cdot i_u}{V_n \cdot I_n}, & i_u > 0 \\ 0, & i_u \le 0 \end{cases}$$
$$P_s(D_{\rm up}) = \begin{cases} 0, & i_u > 0 \\ f_s \cdot E_{\rm rec} \cdot \frac{(V_{dc1}+V_{dc2})\cdot i_u}{V_n \cdot I_n}, & i_u \le 0 \end{cases} \quad (8)$$

where $P_s(S_{\rm up})$ and $P_s(d_{\rm up})$ are the switching losses of the IGBT and diode chips, respectively; V_n and i_n are the nominal voltage (half of the rated IGBT voltage) and rated current for the IGBT module, respectively; $E_{\rm on}$ and $E_{\rm off}$ are the IGBT turn on and off losses under nominal voltage and current; and $E_{\rm rec}$ is the reverse recovery losses of the diode under the same condition.

Based on (8), the average switching losses of each IGBT and diode chip can be simplified as

$$PI_s = \frac{1}{\pi} f_s \cdot (E_{\rm on} + E_{\rm off}) \cdot \frac{V_{\rm dc} \cdot i_m}{V_n \cdot I_n}$$
$$PD_s = \frac{1}{\pi} f_s \cdot E_{\rm rec} \cdot \frac{V_{\rm dc} \cdot i_m}{V_n \cdot I_n} \quad (9)$$

where $V_{\rm dc} = (1/\pi/6) \cdot \int_0^{\pi/6} (V_{sab} + V_{sac}) d\omega_i t \approx 2.858 V_m$.

From (9), it can be found that the equivalent switching losses of the ZCPWM equal to that of the dc/ac inverter with an equivalent dc-bus voltage $V_{\rm dc}$ of 2.858 V_m. Compared to a standard dc/ac inverter with a dc bus voltage of approximately 1.654 V_m, the switching losses of DBMC IGBT under ZCPWM condition are 72.3% higher than that of a dc/ac inverter IGBT. Since the switching losses has a significant effect to the power cycling MTTF of the IGBTs [11], this indicates a higher thermal stress for the inverter-side IGBT/diode under the ZCPWM method.

C. Total Losses of $S_{\rm up}$ and $D_{\rm up}$

Combing (6) and (8), the average losses per switching cycle of the IGBT $S_{\rm up}$, $P(S_{\rm up})$, and diode $d_{\rm up}$, $P(D_{\rm up})$ under ZCPWM can be calculated as

$$P(S_{\rm up}) = P_s(S_{\rm up}) + P_c(S_{\rm up})$$
$$P(D_{\rm up}) = P_s(D_{\rm up}) + P_c(D_{\rm up}). \quad (10)$$

Under the ZVPWM method, the switching losses of the inverter IGBTs are all zero, where

$$P(S_{\rm up}) = P_c(S_{\rm up})$$
$$P(D_{\rm up}) = P_c(D_{\rm up}). \quad (11)$$

Fig. 5(a) and (b) show the power losses of $S_{\rm up}/S_{\rm app}$ and diode $d_{\rm up}/d_{\rm apn}$ for the two PWM control methods under the rated output current. The following conclusions can be observed.

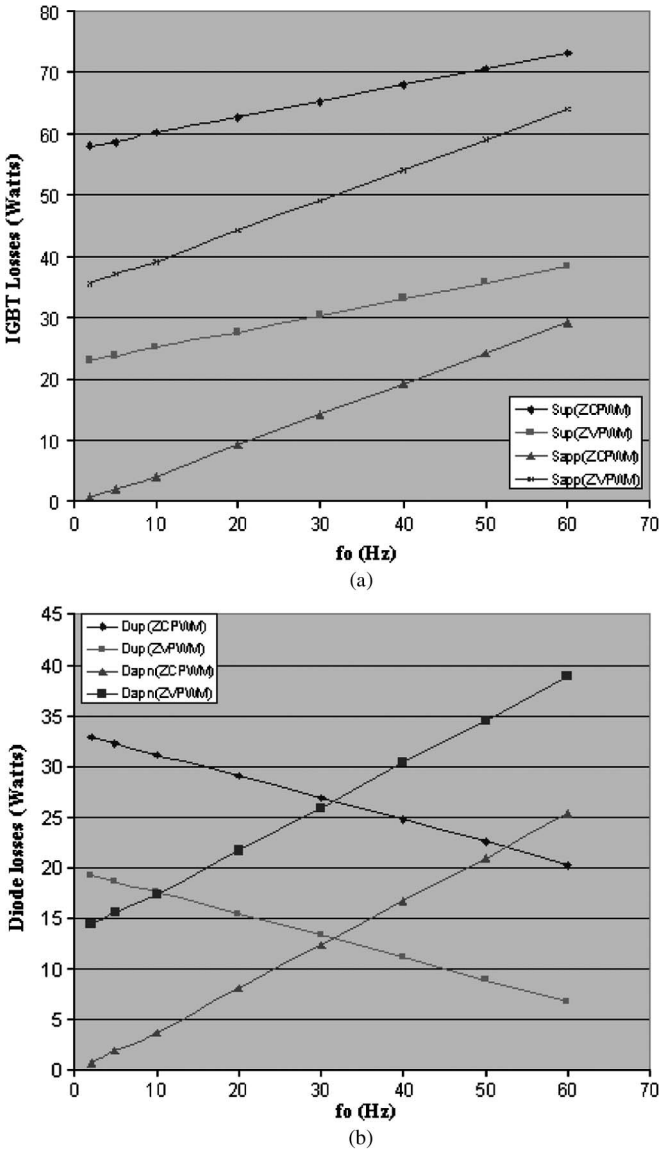

Fig. 5. Comparison of average power losses at different output frequency and rated output current (65 Arms) (a) IGBT losses comparison, (b) Diode losses comparison.

The power losses of the inverter-side IGBT/diode are much lower under ZVPWM condition. This indicates that a smaller chip can be selected for the inverter IGBTs for ZVPWM.

On the contrary, the power losses of the rectifier side IGBT under ZVPWM are much higher than that of the IGBT under ZCPWM. This implies the presence of larger IGBT/diode chips under the ZVPWM for the rectifier side switches

The power losses of the rectifier side IGBTs are closer to the inverter-side IGBT under ZCPWM. If the same IGBT chips are selected for both the rectifier and the inverter, the ZCPWM method has better overall IGBT utilizations.

VI. JUNCTION TEMPERATURE PROFILE COMPARISON OF THE TWO METHODS AND LIFETIME STUDY

A. Junction Temperature Calculation

Fig. 6 shows a simplified thermal system for the DBMC. In this figure, $Z_{\rm jc}$ and $Z_{\rm jcd}$ are the thermal impedance between

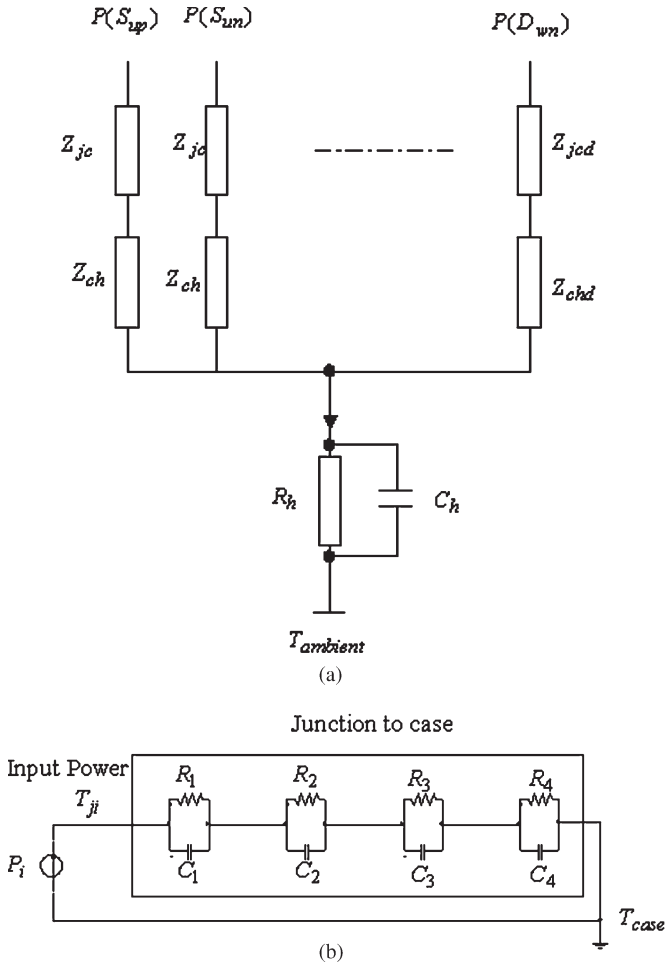

Fig. 6. Simplified thermal system of the DBMC: (a) overall thermal network model and (b) thermal impedance between the junction and case layer of one chip.

TABLE III
THERMAL IMPEDANCE OF THE TESTED IGBT/DIODE

Segments	1	2	3	4	Z_{ch}
R_i: (K/W)	0.00493	0.01501	0.13088	0.10919	0.13
τ_i: (s)	1.187e-5	0.002364	0.02601	0.06499	0.7
R_d: (K/W)	0.00908	0.02726	0.24202	0.20164	0.15
τ_d: (s)	1.187e-5	0.002364	0.02601	0.06499	0.7

the junction and case layer of the IGBT and diode chip, respectively. $Z_{\rm ch}$ and $Z_{\rm chd}$ are the thermal impedance between the case layer and the heat sink. The similar thermal impedance value as shown in [11], [12] are applied. The thermal resistance and time constants of the diode and IGBT chips are listed in Table III. The thermal resistance and time constants of the heat sink are selected as $R_h = 0.06$ k/w and $\tau_h = R_h C_h = 120$ s

Fig. 7(a) and (b) show temperature profile of the inverter-side IGBT $S_{\rm up}$ at 60 Hz and 2 Hz under rated current. From this figure, the following conclusions can be made.

- The temperature variation of inverter IGBTs under ZCPWM is much higher than that of the IGBTs under the ZVPWM method.
- The maximum junction temperature of ZVPWM is much lower than that of the ZCPWM. Therefore, the thermal stress of the ZVPWM for inverter IGBT is much lower than that of the ZCPWM.
- Due to zero inverter switching losses for the ZVPWM, the maximum inverter junction temperature of $S_{\rm up}$ at 2 Hz condition is slightly higher than that at 60 Hz condition.
- The maximum junction temperature of $S_{\rm up}$ under ZCPWM is much higher than that of ZVPWM under the same condition. The ZVPWM is more favorable in low speed conditions.
- The temperature variation at 60 Hz condition for both PWM control methods are less than 10 °C.

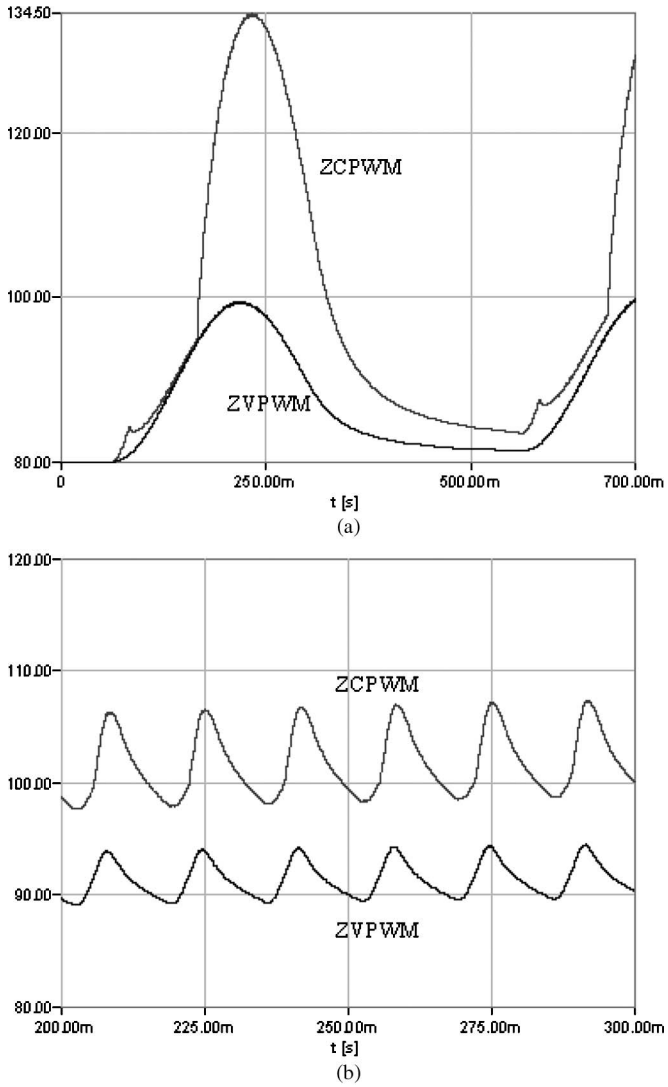

Fig. 7. Junction temperature profile of $S_{\rm up}$ at various output frequency under rated output current 65 Arms: (a) 2 Hz and (b) 60 Hz.

B. Power Cycling Failure Mode of the IGBT Chips and Power Cycling MTTF Estimation of the Module

A typical model of predicting the number to failure of the IGBT-based power cycling capability has been studied in reference [8]–[10] as

$$N_f(T_m, \Delta T_j) = A \cdot \Delta T_j^{\alpha} \cdot \exp\left(\frac{Q}{R \cdot T_m}\right) \qquad (12)$$

where A, α, Q, R are all constant and are decided by the way the module is built up; ΔT_j is the variation of the junction temperature; and T_m is the mean junction temperature in one power cycle.

Based on the reliability data from the supplier, the following extracted values are used in this paper.

$$A = 654.8$$
$$\alpha = -7.801$$
$$Q/R = 1.378 \times 10^4\,^{\circ}\mathrm{C} \tag{13}$$

To predict the power cycling MTTF of the module under power cycling capability, one widely used method is called linear accumulation of the thermal cycle fatigue damage models as shown in reference [9], [10]. Under this assumption, power cycling MTTF of the bond wires for a silicon chip can be estimated as

$$\mathrm{MTTF} = \frac{T}{\int_0^T \frac{N(T_m(t),\Delta T_j(t))}{N_f(T_m(t),\Delta T_j(t))}dt} \tag{14}$$

where T is the unit cycle time period of the load to be studied and $N(T_m(t), \Delta T_j(t))$ is the number of power cycles of the silicon die with an average junction of $T_m(t)$ and temperature variation of $\Delta T_j(t)$ in each period T. $N_f(T_m(t), \Delta T_j(t))$ is the number of cycles to failure of the chip under the same temperature condition.

C. Power Cycling MTTF Estimation of the Module Under Full Load Conditions

Based on the previous analysis, the power cycling MTTF estimation of the IGBT module under full load is studied by combining (11) and (13). During the study, it is assumed that the converter operates at rated motor current and rated power factor (0.85). The output frequency of the converter is adjusted from 1 Hz to 60 Hz. The average junction temperature T_m and temperature variation ΔT_j at different output frequencies are simulated under Ansoft Simplorer program and the power cycling MTTF is calculated in an Excel spreadsheet.

Fig. 8 further shows the MTTF estimation of S_{up} under both PWM conditions. Moreover, the similar estimations have been made to study the IGBT lifetime S_{up} for a dc/ac inverter [11] and S_{aup} for a CMC [12]. The power cycling MTTF of the IGBTs in these two converters are also shown in Fig. 8.

D. Discussion

The following conclusions can be made from Fig. 8.

- Under ZVPWM, the DBMC shows much higher power cycling MTTF than the ZCPWM, CMC, and dc/ac inverter. This is because the ZVPWM method shows zero switching losses in the inverter-side IGBTs.
- The power cycling MTTF of the DBMC under ZCPWM is much lower than that of the dc/ac inverter. This is because the switching losses on the inverter IGBTs are much higher under ZCPWM.

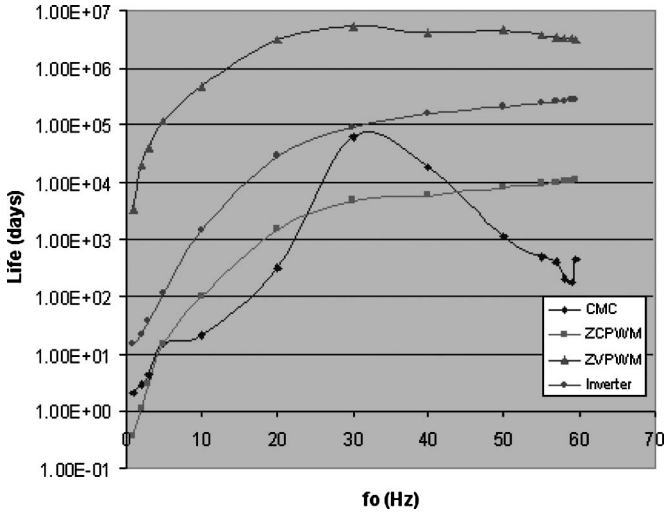

Fig. 8. Power cycling MTTF of the IGBT used in a DBMC, a CMC, and a dc/ac inverter at rated output current condition (65 Arms).

- The power cycling MTTF of the DBMC for inverter-side IGBT has a similar trend as the dc/ac inverter. They are both low under low speed and high under high speed conditions. At high output frequency condition, the power cycling failure are not the main failing factors of the IGBT for DBMC and dc/ac inverters.
- The power cycling MTTF of the CMC is low when the output frequency is low and when the input and output frequency are closer to each other. A bigger IGBT may have to be applied to guarantee a longer life;
- The DBMC can achieve the best overall power cycling performance by combining the ZCPWM and ZVPWM methods. For example, under low speed, a ZVPWM should be applied to increase the power cycling MTTF of the inverter IGBT. Under higher speed condition, the ZCPWM method can be selected so that a smaller chip size can be used for the rectifier side IGBT.

VII. Conclusion

This paper has discussed two zero-switching PWM control methods for DBMC and compared the IGBT power cycling capability of the DBMC with a dc/ac inverter and a CMC. The following conclusions are made.

- The ZVPWM method minimizes the losses of the inverter-side IGBT and diode; on the contrary, the ZCPWM method minimizes the losses of the rectifier side IGBT/diode.
- The DBMC under the ZVPWM method shows much higher power cycling MTTF in the IGBTs than that of the DBMC under the ZCPWM, dc/ac inverter, and the CMC.
- There is considerable advantage using the DBMC in improving the lifetime of an IGBT.

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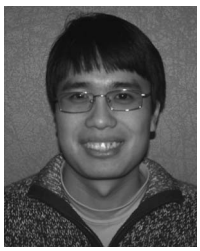

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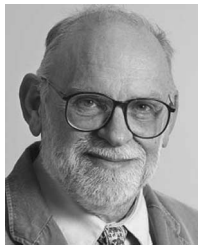

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