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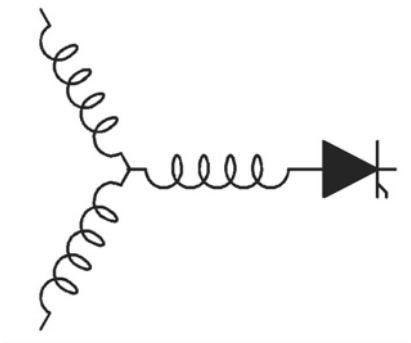
Performance Improvement of Dual-Half-Controlled-Converter and Its Applications in Utility Rectifiers

Y. Wang, D. Panda*, T. A. Lipo, D. Pan**

University of Wisconsin - Madison,
Madison, WI 53705, USA

*TCI LLC.,
Milwaukee, WI 53224, USA

**Hanyang University
Ansan-si, Gyeonggi-do, Korea



Wisconsin
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University of Wisconsin-Madison
College of Engineering
Wisconsin Power Electronics Research Center
2559D Engineering Hall
1415 Engineering Drive
Madison, WI 53706-1691

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Y. Wang[1], D. Panda[2], T. A. Lipo[3], and D. Pan[1]
[1] University of Wisconsin - Madison, Madison, WI 53705, USA
[2] TCI LLC., Milwaukee, WI 53224, USA
[3] Hanyang University, Ansan-si, Gyeonggi-do, Korea

***Abstract*-- This paper presents improved control techniques for the three-phase three-wire dual-half-controller-converter (DHCC) using an interleaved pulse-width-modulation (PWM) technique. Compared with the hysteresis controller presented in earlier literatures, the proposed PWM controllers require smaller filtering elements and/or a lower sampling frequency. While the same number of active switches are used compared to a conventional voltage-source-converter (VSC), the current rating for each device in DHCC is significantly lower. The proposed system is free of shoot through and it provides system redundancy. Both simulations and experimental results are presented.**

***Index Terms*—Half-controlled-converter, interleaving, PWM, volt-seconds**

I. INTRODUCTION

A half-controlled-converter (HCC) is a voltage-source-converter (VSC) having only three switches and six diodes, as shown in Fig. 1 [1]. The converter can be realized as either a common-emitter (CE) or common-collector (CC) configuration. A CE configuration is usually preferred due to its simple gate drive implementtation. In [1] a single HCC and its potential as controlled rectifier are explored. The effect of series line reactor and displacement power factor angle on the performance of a single HCC is reported.

A dual-half-controlled-converter (DHCC) consists of two paralleled complementary HCCs [2][3], and the harmonic content in the total input current is significantly reduced. The complementary configuration can be realized using complementary converter topologies (i.e. CE and CC) or by using a transformer with two secondary windings of opposite polarities [2][3]. The input current and power can be shared equally between the two HCCs, resulting in a significantly lower current rating for all the devices in a DHCC compared to a conventional VSC rated for the same power. DHCC is free of shoot-through and it provides system redundancy, i.e. the system remains operational in case one of the two HCCs fails, at the price of reduced power output and increased harmonics. The issue of high DC output ripples as presented in [2] is resolved by combining the two DC links [3] while the input characteristics are identical. A simpler controller is introduced in [3] that imposes a 0.5 pu hard peak current limit for each HCC.

Hysteresis controllers are reported in earlier literature for regulating the HCC and DHCC currents [1][2][3] due to the lack of a linear model and control means. Hysteresis modulators are simple and effective; however, it has inherent disadvantages of variable switching frequency, which complicates the thermal design and filter design. Also, successful implementation of such current regulators demands fast sampling. In this paper, PWM-based controllers are proposed that make DHCC a more attractive topology for active rectifiers.

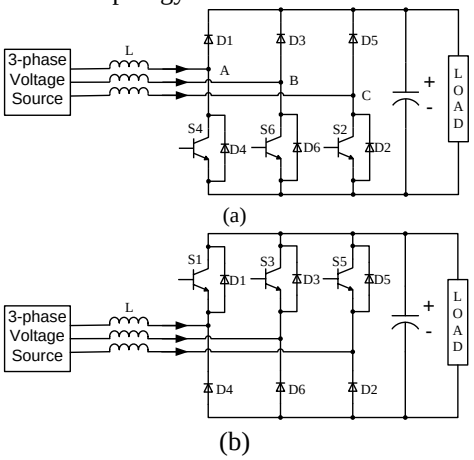

Fig. 1. HCC configurations: CE (a) and CC (b) [1]

II. DHCC CONFIGURATIONS AND OPERATING PRINCIPLES

A DHCC rectifier is shown in Fig. 2 [3]. The isolation transformer has two secondary windings of opposite polarities, which effectively makes the two CE HCCs complementary to each other. Each side of the transformer can be either Y or delta connection as long as the two secondary circuits are coupled in the same magnetic path. By paralleling complementary HCCs, the even harmonics generated by each HCC are automatically cancelled in the mains, but proper control techniques are still needed to eliminate the non-triplen odd harmonics.

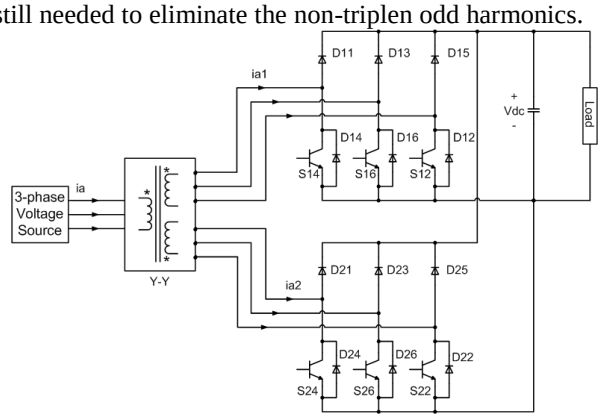

Fig. 2. DHCC rectifier [3]

Define three-phase voltages and commanded currents:

$$\begin{cases} v_a(\varphi) = V_S\cos(\varphi+\theta) \\ v_b(\varphi) = V_S\cos(\varphi-\frac{2\pi}{3}+\theta) \\ v_c(\varphi) = V_S\cos(\varphi+\frac{2\pi}{3}+\theta) \end{cases} \quad (1)$$

$$\begin{cases} i_a^*(\varphi) = I_S^*\cos(\varphi) \\ i_b^*(\varphi) = I_S^*\cos(\varphi-\frac{2\pi}{3}) \\ i_c^*(\varphi) = I_S^*\cos(\varphi+\frac{2\pi}{3}) \end{cases} \quad (2)$$

Define L to be the line inductance, and ω the line frequency in rad/sec. A full cycle of 2π can be divided into six equal length periods. Taking the $[-\frac{\pi}{6},\frac{\pi}{6}]$ period as an example, without any active compensation between two HCCs, the phase current in each HCC consists of the following sequential segments:

For $\varphi \in [-\frac{\pi}{6},\varphi_s]$,

$$\begin{cases} i_a(\varphi) = I_S^*\,cos(\varphi) \\ i_b(\varphi) = -i_a(\varphi) \\ i_c(\varphi) = 0 \end{cases} \quad (3)$$

where φ_s is the angle at which phase-C current starts to flow,

$$\varphi_s = -tan^{-1}\left[\frac{V_S\left[\cos\left(\frac{2\pi}{3}+\theta\right)-\cos\left(\frac{2\pi}{3}-\theta\right)\right]}{-V_S\left[\sin\left(\frac{2\pi}{3}-\theta\right)+\sin\left(\frac{2\pi}{3}+\theta\right)\right]+\omega LI_S^*}\right] \quad (4)$$

For $\varphi \in [\varphi_s,\varphi_h]$,

$$\begin{cases} i_a(\varphi) = I_S^*\,cos(\varphi) \\ i_b(\varphi) = -\frac{\sqrt{3}V_S}{2\omega L}[cos(\varphi+\theta)-cos(\varphi_s+\theta)]-\frac{I_S^*}{2}[cos\,\varphi+cos\varphi_s] \\ i_c(\varphi) = \frac{\sqrt{3}V_S}{2\omega L}[cos(\varphi+\theta)-cos(\varphi_s+\theta)]-\frac{I_S^*}{2}[cos\,\varphi-cos\varphi_s] \end{cases} \quad (5)$$

where φ_h is the angle at which phase-B current either reaches zero or rejoins the command, if $\varphi_h \le \frac{\pi}{6}$, then

$$\varphi_h = sin^{-1}\left[\frac{-\sqrt{3}V_S\cos(\varphi_s+\theta)+\omega LI_S^*\cos(\varphi_s)}{\sqrt{(\sqrt{3}V_S sin\theta)^2+(-\sqrt{3}V_S cos\theta-\omega LI_S^*)^2}}\right]-tan^{-1}\left[\frac{-\sqrt{3}V_S cos\theta-\omega LI_S^*}{\sqrt{3}V_S sin\theta}\right] \quad (6)$$

$$\begin{cases} i_a(\varphi) = I_S^*\cos(\varphi) \\ i_b(\varphi) = 0 \qquad ,\varphi \in [\varphi_h,\frac{\pi}{6}] \\ i_c(\varphi) = -i_a(\varphi) \end{cases} \quad (7)$$

Otherwise (i.e. $\varphi_h > \frac{\pi}{6}$),

$$\varphi_h = sin^{-1}\left[\frac{-\sqrt{3}V_S\cos(\varphi_s+\theta)+\omega LI_S^*\cos(\varphi_s)}{\sqrt{(\sqrt{3}V_S sin\theta-\omega LI_S^*)^2+(-\sqrt{3}V_S cos\theta)^2}}\right]-tan^{-1}\left[\frac{-\sqrt{3}V_S cos\theta}{\sqrt{3}V_S sin\theta-\omega LI_S^*}\right] \quad (8)$$

So far, all segments of period $\varphi = -\frac{\pi}{6}\sim\frac{\pi}{6}$ have been presented; the other five periods are merely replicates of (3) ~ (8) with different phase shift and phase index. The total current waveform is plotted with dashed trace in Fig. 3, with 0.08 pu line reactance at unity displacement power factor. The waveform shape varies depending on the line reactance and the displacement power factor.

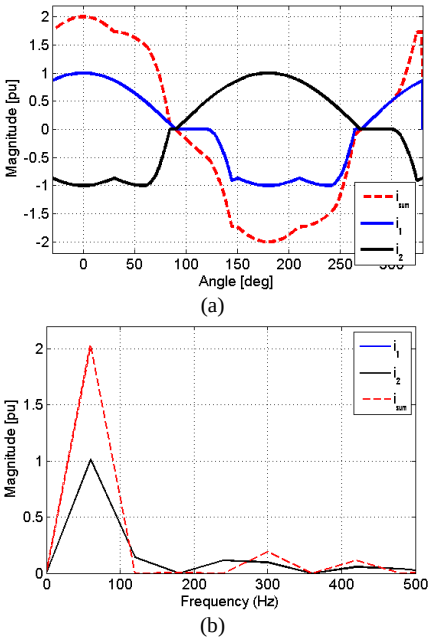

Fig. 3. DHCC phase current without active compensation, (a) waveforms, and (b) spectrums

The above results confirm that the current in each HCC contains even order harmonics while the total current does not; however, non-triplen odd harmonics in both HCCs add up in the total current. To eliminate these harmonics, an active compensation technique was presented in earlier literature that utilizes current command cross-coupling and hysteresis switching method [2][3]. In this paper, however, two different PWM-based techniques are presented.

III. Formulated Current Compensation

If the currents in two phases are directed into the HCC, then it is a fully-controlled interval, otherwise it is a partially controlled period. These two types of periods are of equal length and are present in an alternating manner. The key to synthesizing sinusoidal total line current is to utilize the fully-controlled periods to compensate for the partially-controlled periods of the complementary HCC.

The desired compensated phase current in each HCC is illustrated in Fig. 4 with which a sinusoidal total current can be achieved. The dashed traces are the original currents in HCC and the solid traces are the desired currents. However, this compensation is infeasible, because the current direction cannot be reversed during the fully-controlled periods. As a result, a compromise must be made, i.e. either accepting a slightly imperfect compensation as shown in Fig. 5, or adopting a slightly lagging power factor for perfect compensation as shown in Fig. 6.

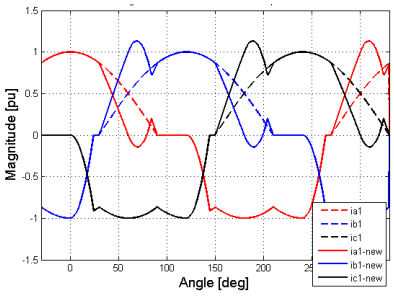

Fig. 4. HCC original and new phase current with desired (non-feasible) compensation

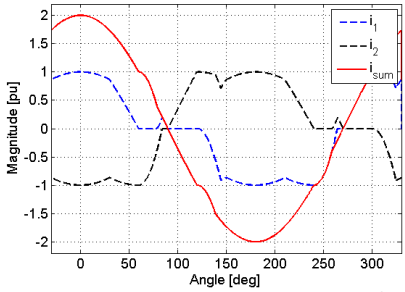

Fig. 5. HCC original and new phase current with feasible but compromised compensation

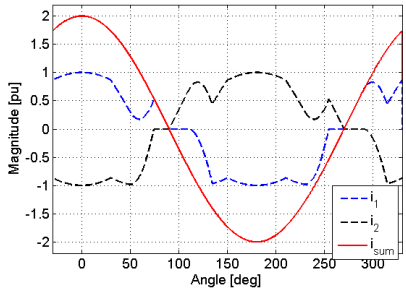

Fig. 6. HCC original and new phase current with compensation at 10 degrees lagging power factor

Based on the circuit parameters and the operating point, the instantaneous operating conditions of a DHCC and the necessary compensation can be estimated using (3) ~ (8), which are then used to calculate the voltage commands and the resultant switching duty cycles during each PWM period. This method is named "*formulated current compensation*" because all the calculation and control are based on estimated formulas.

Take the period $\varphi \in [-\frac{\pi}{6}, \frac{\pi}{2}]$ as example, the voltage command calculations for an HCC in a DHCC are presented below, where $e(k)$ is the source phase voltage measured at each sampling instant, $i(k)$ is the measured current, $i^*(k)$ is the current command, $v(k)$ is the desired voltage output of each HCC, and T_s is the sampling period.

For $\varphi \in [-\frac{\pi}{6}, \varphi_s]$, only phase-A can be controlled,

$$v_a(k) = [e_a(k) - e_b(k)] - \frac{2L}{T_s}[i_a^*(k) - i_a(k)] \quad (9)$$

For $\varphi \in [\varphi_s, \varphi_h]$, only phase-A can be controlled,

$$v_a(k) = \frac{3}{2}\left[e_a(k) - \frac{L}{T_s}[i_a^*(k) - i_a(k)]\right] \quad (10)$$

For $\varphi \in [\varphi_h, \frac{\pi}{6}]$, only phase-A can be controlled,

$$v_a(k) = [e_a(k) - e_c(k)] - \frac{2L}{T_s}[i_a^*(k) - i_a(k)] \quad (11)$$

For $\varphi \in [\frac{\pi}{6}, \frac{\pi}{2}]$, phase-A and B can be controlled,

$$\begin{cases} v_a(k) = 2\left[e_a(k) - \frac{L}{T_s}[i_a^*(k) - i_a(k)]\right] + \left[e_b(k) - \frac{L}{T_s}[i_b^*(k) - i_b(k)]\right] \\ v_b(k) = 2\left[e_b(k) - \frac{L}{T_s}[i_b^*(k) - i_b(k)]\right] + \left[e_a(k) - \frac{L}{T_s}[i_a^*(k) - i_a(k)]\right] \end{cases} \quad (12)$$

The other two periods $[\frac{\pi}{2}, \frac{7\pi}{6}]$ and $[\frac{7\pi}{6}, \frac{11\pi}{6}]$, as well as all the complementary counterparts, are merely replicates of (9) ~ (12) with the appropriate phase index.

The overall controller structure is shown in Fig. 8. The two PWM carriers for two HCCs are interleaved with 180 degrees out of phase switching, so that the switching ripple in the total current will be further reduced.

IV. Coordinated Volt-Seconds Modulation

The coordinated volt-second modulation is based on the D-Q equivalent circuit of DHCC utility rectifier as shown in Fig. 7, where E and $\underline{i}_{dq}$ are the source voltage and current respectively, L_s is the transformer primary side leakage inductance, L_m is the transformer magnetizing inductance, L_c is the converter side inductance including transformer secondary leakage inductance, R_s is total line resistance, $\underline{v}_{dq1}$ and $\underline{v}_{dq2}$ are the voltages synthesized by the two HCCs respectively, $\underline{i}_{dq1}$ and $\underline{i}_{dq2}$ are the current flowing into the two HCCs respectively. The D-Q voltage commands are calculated using (13) ~ (14) during each PWM interval. Note that the resultant total D-Q voltage commands need to be further scaled and assigned to both HCCs.

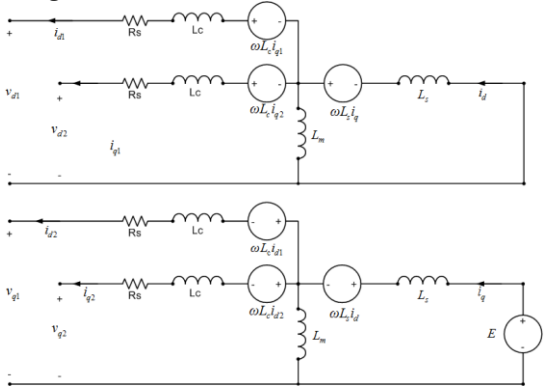

Fig. 7. D-axis (upper) and Q-axis (lower) equivalent circuits of DHCC rectifier system

$$v_q^*(k) = 2E - \frac{(2L_s+L_c)[i_q^*(k)-i_q(k)]}{T_s} - R_s i_q(k) - \omega(L_c + 2L_s) i_d(k) + 2v_{q-PI}^*(k) \quad (13)$$

$$v_d^*(k) = -\frac{(2L_s+L_c)[i_d^*(k)-i_d(k)]}{T_s} - R_s i_d(k) + \omega(L_c + 2L_s) i_q(k) + 2v_{d-PI}^*(k) \quad (14)$$

The overall volt-seconds controller is presented in Fig. 9. Besides the D-Q voltage commands generated by a PI regulator (i.e. v_{q-PI}^* and v_{d-PI}^*), decoupling terms as well as volt-seconds compensation terms are incorporated in (13) ~ (14) for improving the dynamic performances. However, the resultant phase voltage commands v_{abcN}^* cannot be directly used for generating gate pulses, because the neutral voltage of each HCC remains unknown due to the lack of controllability, which is the major barrier for utilizing PWM regulators in this case.

To handle this key issue, (15) below is proposed to convert the neutral-referenced voltage commands into

ground-referenced values, and hence can be used for generating gate signals. This function is represented in Fig. 9 as the "Voltage Command Calculator" block. The secondary side tied to HCC1 is assumed to have the same polarity as the source.

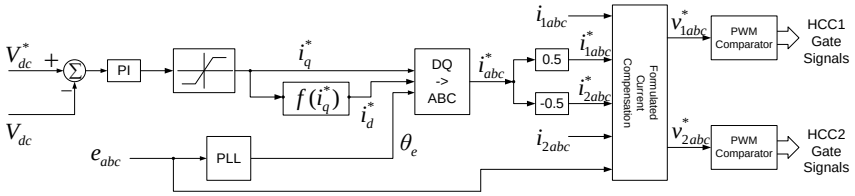

Fig. 8. Overall controller diagram of formulated current compensation

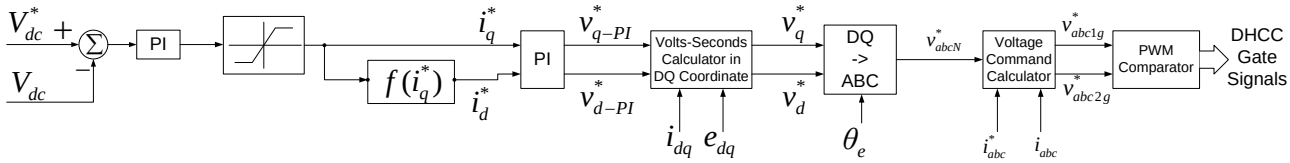

Fig. 9. Overall controller diagram of coordinated volt-seconds modulation

The conversion shown in (15) is in effect "controlling" rather than "estimating" neutral voltages by injecting a third harmonic component in the modulation index.

$$\begin{cases} v^*_{abc1-N1}(k) = \frac{v^*_{abc-N}(k)}{2} \\ v^*_{abc2-N2}(k) = -\frac{v^*_{abc-N}(k)}{2} \\ \hat{v}_{N1}(\mathrm{k}) = -\min[v^*_{abc1-N1}(k)] \\ \hat{v}_{N2}(\mathrm{k}) = -\min[v^*_{abc2-N2}(k)] \\ v^*_{abc1-G}(k) = v^*_{abc1-N1}(k) + \hat{v}_{N1}(\mathrm{k}) \\ v^*_{abc2-G}(k) = v^*_{abc2-N2}(k) + \hat{v}_{N2}(\mathrm{k}) \end{cases} \quad (15)$$

However, further investigations reveal that the above presented control technique may result in untamed current peak in each HCC under certain circumstances. Therefore, an additional step (16) is added after (15) for neutral voltages adjustment, where the "limit" is the upper limit of the current amplitude in each HCC, i.e. 0.5 pu in this case.

$$\begin{cases} \hat{v}_{N1}(k) = v_{dc} - max[v^*_{abc1-N1}(k)], if\ i_{abc1} > limit \\ \hat{v}_{N2}(k) = v_{dc} - min[v^*_{abc2-N2}(k)], if\ i_{abc2} > limit \end{cases} \quad (16)$$

Again the two PWM carriers are interleaved with a 180 degree phase difference, so that the switching ripples in the total current will be further reduced.

V. SIMULATION RESULTS

All the simulation results are presented in per-unit. The voltage base is the phase-to-neutral voltage peak, and the current base is the phase current peak.

A. Current Command Cross-Coupling

The current command cross-coupling technique presented in [3] is simulated and the results are presented below as a benchmark for comparison. The simulation is done at unity displacement power factor, with a 40 kHz sampling frequency and 0.14 pu line reactance. The current peak in each HCC is restricted to 0.5 pu.

Define I_{rated} as the rated current; the current in each HCC is 53.5% of I_{rated} in terms of RMS value, and about 51% in terms of peak. The THD of the total phase current is 3.8% while the THD of the current in each HCC is 40%.

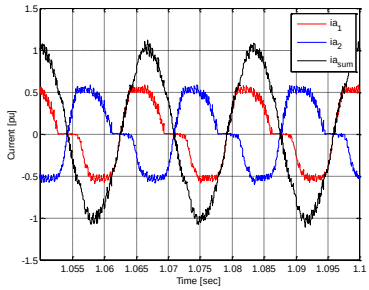

Fig. 10. DHCC current waveforms using current command cross-coupling

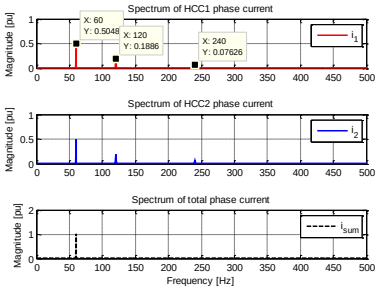

Fig. 11. Spectrums of DHCC current waveforms using current command cross-coupling

B. Formulated Current Compensation

The simulation of formulated current compensation is done with a 10 kHz PWM frequency and 0.14 pu line reactance. In order to achieve ideal compensation, a 10 degrees lagging power factor is adopted. As a result, the current amplitude is slightly increased by 1.5%, which is almost negligible.

The current in each HCC is 53.4% of I_{rated} in terms of RMS value, and about 51.5% in terms of peak. The THD of the total phase current is 3.5% while the THD of the current in each HCC is 29%. Notice that the even-order harmonics in each HCC are much lower than in case-A.

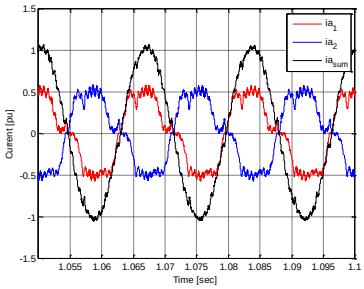

Fig. 12. DHCC current waveforms using formulated current compensation

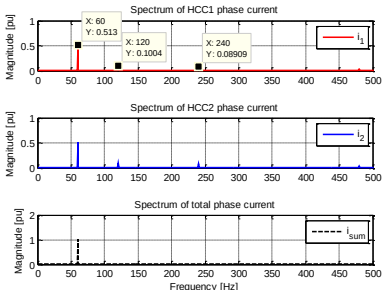

Fig. 13. Spectrums of DHCC current using formulated current compensation

C. Coordinated Volt-Second Modulation

The simulation of coordinated volt-seconds modulation is done at unity displacement power factor, with 10 kHz PWM, and 0.14 pu line reactance. The results presented in Fig. 14 and Fig. 15 are derived without incorporating (16). The resultant current in each HCC is 59.2% of I_{rate} in terms of RMS value, and about 72% in terms of peak. The THD of the total phase current is 3.2% while the THD of the current in each HCC is 64.3%. Note that the even-order harmonics in each HCC are higher than the other two cases.

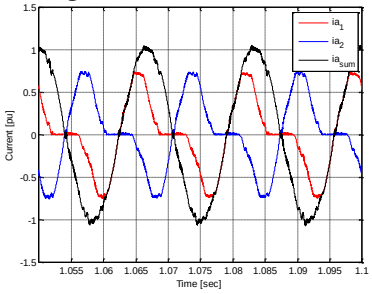

Fig. 14. DHCC current waveforms using coordinated volt-seconds modulation, without limiter

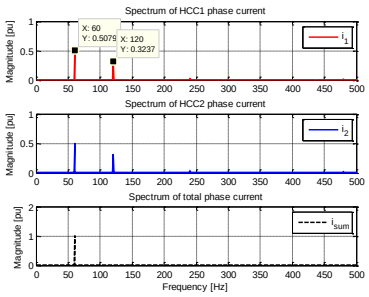

Fig. 15. Spectrum of DHCC current waveforms using coordinated volt-seconds modulation, without limiter

Next, the additional adjustment (16) is activated in the controller, and the corresponding results are presented below. The resultant current in each HCC is 54% of I_{rated} in terms of RMS value, and about 56% in terms of the peak value. The THD of the total phase current is 4.2% while the THD of the current in each HCC is 42%. However, the 2nd harmonic in each HCC is significantly reduced which reduces the current amplitude and RMS values.

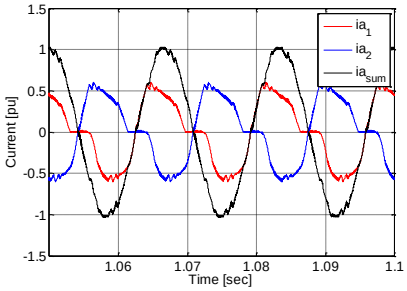

Fig. 16. DHCC current waveforms using coordinated volt-seconds modulation, with limiter

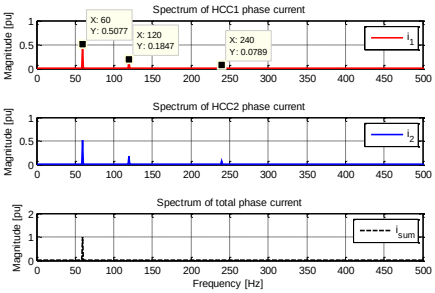

Fig. 17. Spectrum of DHCC current waveforms using coordinated volt-seconds modulation, with limiter

A transient condition is simulated and the results are presented below. The load is decreased by 50% at 0.4 sec and restored to 100% at 0.6 sec. The system shows perfect stability throughout the transient.

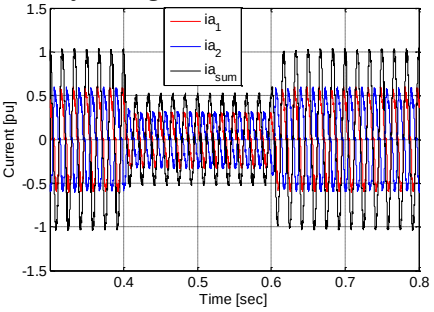

Fig. 18. DHCC phase currents during load transient

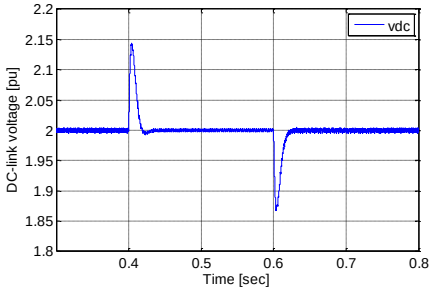

Fig. 19. DHCC DC-link voltage during load transient

VI. Observations and Discussions

The current command cross-coupling method with hysteresis regulator used in [2][3] is simple and robust, and it is straightforward for restricting the peak current

in each HCC to 0.5 pu. However, it requires large filtering elements and/or fast sampling. Also, it results in undetermined switching frequency as well as possible switching oscillation instabilities.

The formulated current compensation is based on estimated operating conditions and therefore its performance relies heavily on the parameter estimation accuracy. This method has the lowest device current rating because the resultant even harmonics in each HCC are minimal. Utilizing fixed-frequency PWM enables interleaved switching, which plays a crucial role in further reducing current ripples on the mains. In this type of computed current reference, if there is any error in reference due to a mismatch between the estimated and actual circuit parameters, then the error never gets corrected irrespective of the closed-loop operation and thus it is often criticized as open loop current regulator. This problem, however, can be resolved by incorporating a closed-loop estimator for fine-tuning the line reactance estimation.

Coordinated volt-seconds modulation is a closed-loop controller with a fixed switching frequency and lower sampling rate, and the resultant current and DC-link voltage are smoother and more stable. Compared with the formulated current compensation, it can operate over a wider range of power factor. It is also confirmed in the simulations and experiments that the system performance is not very much affected by the parameter estimation accuracy. With the neutral voltage adjustment technique, the current rating can be restricted to similar level as the other two control techniques. Based on the simulations and analyses results, the coordinated volt-seconds modulation approach can be considered as the most preferred current regulation technique for the interleaved DHCC system, which will also be the focus of experimental demonstrations.

VII. Converter Current Rating

It is essential to study the variation of current ratings as a function of the operating conditions; and for the volt-seconds modulation it is also useful to investigate the effectiveness of current limiting technique under different operating conditions. The coordinated volt-seconds modulation is assumed for the discussions in this section.

Fig. 20 illustrates the variations in the current peak and RMS values in each HCC as a function of line reactance, both with and without the current limiting technique. Without the peak current limiter, as the line reactance increases, both peak and RMS current values in each HCC increase accordingly, and the peak value increases faster. This is caused by the increase of the 2nd harmonic current. However, by introducing peak current limiter (16), the current rating is effectively reduced especially for the peak value. Note that the traces of peak and RMS current values with peak current limiter overlap each other.

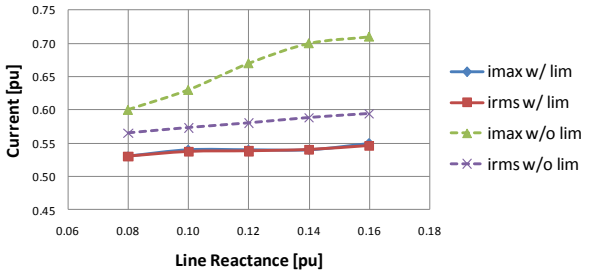

Fig. 20. Simulated current in HCC as a function of line reactance

As shown in Fig. 21, the THD variation caused by the current limiting technique is insignificant with different line reactance values.

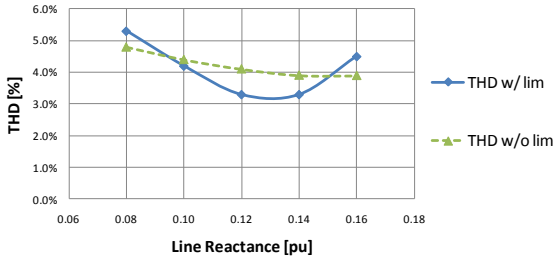

Fig. 21. Simulated current THD as a function of line reactance

Fig. 22 presents the variations in the HCC current as a function of displacement power factor with 0.12 pu line reactance. A positive angle designates a lagging power factor. Generally speaking, both the peak and RMS values of HCC current keep declining as the power factor becomes more lagging until they level out at approximately 10 degrees lagging. This result means that, although the total current is minimal at unity power factor given any certain output power, the minimum current in each HCC may actually be achieved at a slightly lagging power factor. The current limiting technique proves to be very effective but has limited impact for leading power factors, and it is not critical for lagging power factors since a lagging power factor itself contributes to the current rating reduction. As shown in Fig. 23, the THD variation caused by the current limiting technique is again insignificant across the operating power factor range.

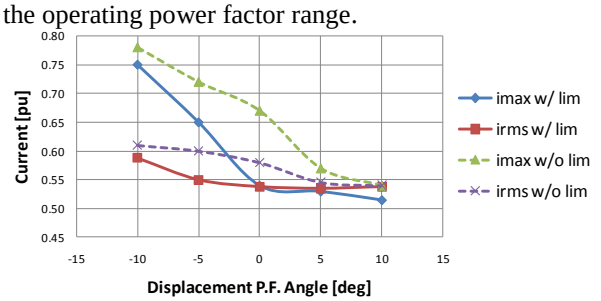

Fig. 22. Current in HCC as a function of power factor angle

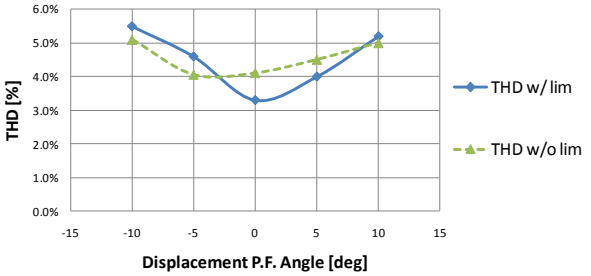

Fig. 23. Current THD as a function of power factor angle

The key to choosing a proper device current rating, which is also a major future work of DHCC rectifier, involves a detailed device loss calculation, especially given the fact that the currents in HCCs are highly non-sinusoidal. Given the special current waveforms in an HCC, the most practical analysis approach is to embed the loss calculation in the circuit simulation. To be more specific, at each simulation step, the instantaneous current value can be used to extract from the datasheets the corresponding device voltage drop, turn-on/off losses, reverse recovery losses, etc., hence the dynamic loss profile is obtained, which can be further integrated with the device/converter thermal equivalent circuit model, enabling dynamic characterization of thermal profile.

VIII. Nominal DC-Link Voltage

The nominal DC-link voltage selection also has a significant impact on the system performance. Fig. 24 shows the HCC current rating and total current THD as functions of the DC-link voltage. Simulations have been carried out using coordinated volt-seconds modulator operating at unity displacement power factor, and the load is varied according to the DC voltage to maintain the same power output, which means the input voltage and current remain the same.

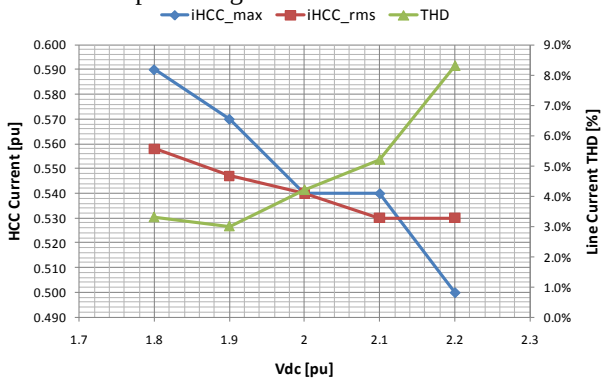

Fig. 24. Current rating and THD as functions of DC-link voltage

As the DC-link voltage increases, the HCC current ratings drop slightly because the peak current limiter becomes more effective with more available voltage; on the other hand, however, the increase in the line current THD is also mainly attributed to the limiter. Each time the limiter is triggered, the modulation pattern has a step change, resulting in steep variations in the currents, which become more severe with a higher DC-link voltage. Therefore the nominal DC-link voltage needs to be chosen with considerations in both current ratings and harmonics.

IX. Experimental Results

The experimental results of coordinated volt-seconds modulation are presented in this section. The two secondary sides of the transformer have slightly different leakage inductance, causing slightly uneven current sharing between the two HCCs. The average phase inductance is approximately 0.15 pu.

Fig. 25 and Fig. 26 present the DHCC operation at unity power factor without and with peak current limiter respectively. An autotransformer is used as the grid source, and its leakage inductance results in the somewhat noisy source voltage waveform.

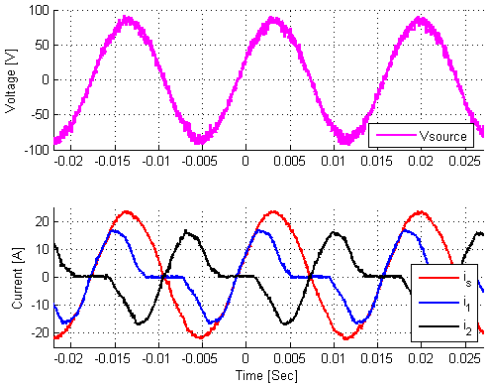

Fig. 25. Experimental results at unity power factor without peak current limiter in each HCC; upper: source voltage; lower: total current and currents in both HCCs

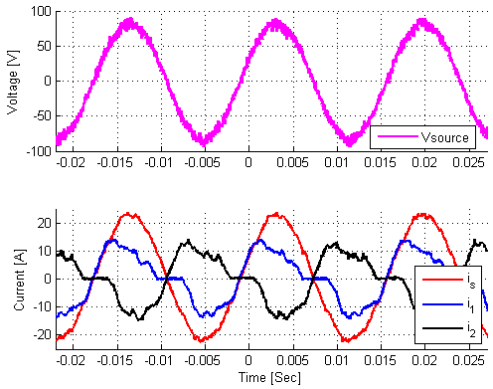

Fig. 26. Experimental results at unity power factor with peak current limiter in each HCC; upper: source voltage; lower: total current and currents in both HCCs

Fig. 27 and Fig. 28 present the DHCC operation at 5 degrees lagging power factor without and with peak current limiter respectively.

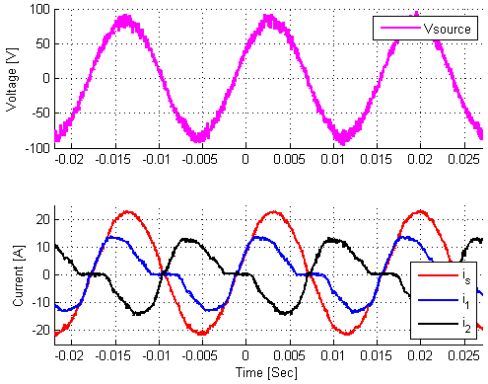

Fig. 27. Experimental results at 5 degrees lagging power factor without peak current limiter in each HCC; upper: source voltage; lower: total current and currents in both HCCs

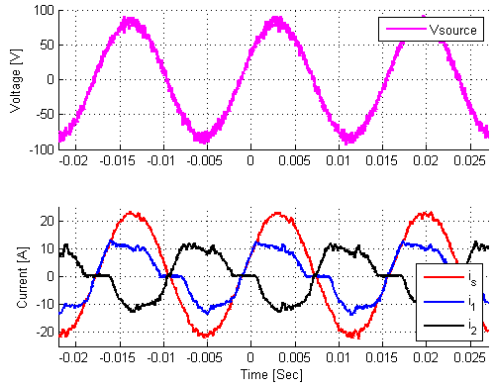

Fig. 28. Experimental results at 5 degrees lagging power factor with peak current limiter in each HCC; upper: source voltage; lower: total current and currents in both HCCs

The above results have proven the effectiveness of volt-seconds modulation technique and its associated peak current limiter. More experiments are carried out and the resultant current ratings are plotted in Fig. 29. The results show a good comparison with theory, e.g. Fig. 22. These results confirm that the peak current limiter is less effective in the leading power factor region, and not necessary for 10 degrees lagging power factors.

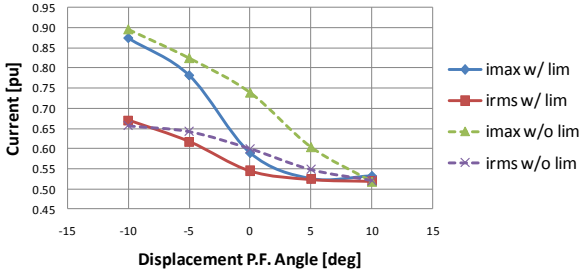

Fig. 29. Experimental results: maximum and RMS currents in each HCC with and without peak current limiter

Load transients have also been demonstrated in the experiments where two step changes in the DC load is applied, i.e. from 100% to 75% and back to 100%. The experimental results show that the system is stable throughout the load transient. As shown in Fig. 30, the peak variation of the DC-link voltage during load transients is about 3.6%.

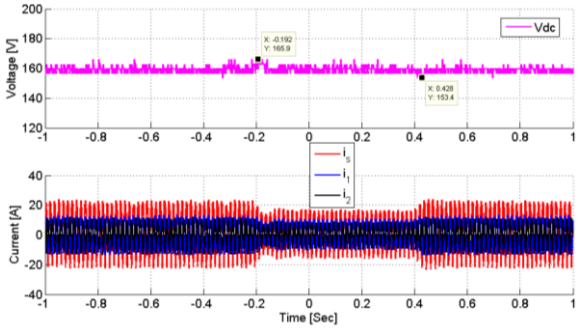

Fig. 30. Experimental results: 25% load transients, DC-link voltage and DHCC currents, with peak current limiter

X. Conclusions

This paper presents two PWM-based control techniques that boost the overall system performance of the three-phase three-wire DHCC rectifier. The benefits and limitations of both techniques are discussed and compared with the hysteresis regulator presented in earlier literature. The analyses suggest that the coordinated volt-seconds modulation may be the most promising control technique for DHCC, and the corresponding experimental results have confirmed the theoretical analyses. The considerations in converter current rating and DC-link voltage selection have been discussed. Enabled by the proposed control techniques, the DHCC promises to be a very economic solution for active rectifiers with improved system reliability and fault redundancy.

Appendix

Simulation parameters:
Source voltage = 1 pu;
Input power = 1 pu;
DC-link voltage = 2 pu;
DC-link capacitor = 0.55 pu

Experiment setup parameters:
PWM frequency = 10 kHz
Source phase voltage peak = 85V
Input line current peak = 22A
Total line inductance for HCC1 ~ 3.3mH (0.159pu)
Total line inductance for HCC2 ~ 2.9mH (0.140pu)
DC-link voltage command = 160V
DC-link capacitor = 4800 uF
DC load ~ 10Ω
Output power ~2500W

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