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Performance Analysis of the Three Transistor Voltage Source Inverter Using Different PWM Techniques

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***Abstract*-- A new three phase three transistor voltage source inverter has recently appeared in the literature which has attractive features compared to the conventional voltage source inverter topologies. In particular, it requires a less number of costly switching devices, such as high performance transistors. This inexpensive design is considered to be advantageous in medium to high power application requiring traditional silicon based power electronic transistors or with newly-evolving yet expensive Silicon Carbide or Gallium Nitride based power semiconductor devices. This paper investigates the realization of the inverter circuit using several different PWM techniques. Theoretical analyses and simulation results are provided to verify the performance and feasibility of the proposed concept.**

***Index Terms*—Voltage Source Inverter, Pulse Width Modulation, Third Harmonic Injected PWM, Space Vector Modulation.**

I. Introduction

Inverters are power electronic converters comprised of semiconductor electronic switches and are utilized extensively in numerous applications such as induction heating, variable speed AC motor drives, uninterruptable power supplies (UPS), distributed generation (DG) units, FACTS and HVDC systems to name only a few[1],[3]. Semiconductor electronic switches are one of the major components of the converter which essentially determine the complexity, cost and efficiency of the system. Presently, Silicon (Si) based power electronic switches are very mature and widely utilized in the power electronics market. However, rapidly evolving wide band-gap semiconductors, predominantly Silicon Carbide (SiC) or Gallium Nitride (GaN) based semiconductors have attracted increasing attention for their promising superiority in terms of voltage blocking capability, operational temperature, and switching frequency [4].

Nevertheless, regardless of their type, at medium to high voltage levels such semiconductor switches become very expensive. Thus, the newly proposed three phase, three transistor voltage source inverter (TTVSI) is a promising power electronic converter where only three expensive power transistors are used. In [5] the TTVSI was first proposed, where the theoretical analysis and the simulation results were provided to verify its performance and feasibility. This major reduction in power transistor count is achieved by using low cost thyristors along with the transistors. In Fig. 1 schematic of the TTVSI is shown, from the figure is can be seen that the transistors of each phase, are placed between two thyristors. Thyristors are used to provide positive to negative current commutation, and transistors are used to employ a suitable PWM technique to the circuit.

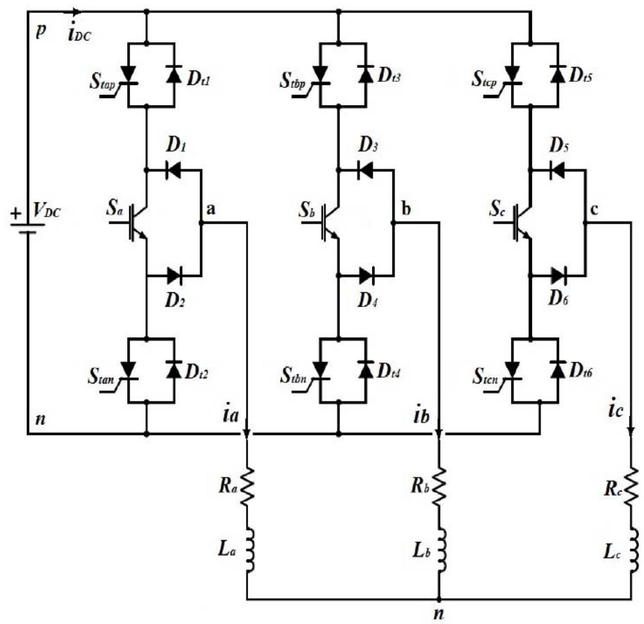


Fig. 1. Schematic of the three transistor VSI topology

At a high voltage level, thyristors are considered viable devices due to their cost effectiveness. However, thyristor based power converters show poor performance due to their inability to self-commutate as well as inability to operate at high frequency. In contrast, transistors show better performance with high frequency, and able to perform at high voltage level only with series string connection until they reach desired voltage level. The TTVSI adopts positive characteristics from both switch types and it is a combinational utilization of low cost feature of a thyristor and high performance characteristics of transistor type semiconductor devices. Moreover, thyristors of the TTVSI do not require complex and expensive forced commutation which is essential for conventional thyristor based VSIs [5],[7]. In [6] several AC-AC matrix converter topologies were proposed based on the TTVSI replacing the conventional six transistor

VSI. The authors analyzed the topologies theoretically and verified the performance and feasibility of a six-transistor matrix converter topology with the simulation results, since all of the proposed topologies share the same operational principle as the TTVSI.

This paper extends the work of [5] and analyzes the performance of the TTVSI using several different PWM modulation techniques and compares its performance with the conventional 6 switch VSI. Here, sine triangle PWM (ST-PWM), third harmonic injected PWM (THPWM), and space vector PWM (SVPWM) techniques are used to realize the topology. System level simulation study is conducted using MATLAB/SIMULINK and the simulation results are provided to verify the performance. This paper will provide performance analysis based upon simulation result.

II. Basic Operation of the Topology

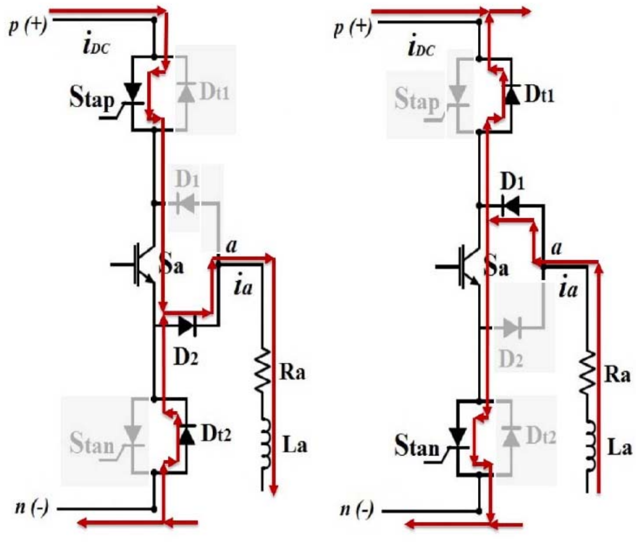
As illustrated in Fig. 1, it can be seen that each phase of the topology consists of a transistor connected in between two thyristors and several diodes which are connected antiparallel with each of the switches. In [5] the output voltage and output current equations of such topology is given as follows

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} S_{tap} & S_{tan} \\ S_{tbp} & S_{tbn} \\ S_{tcp} & S_{tcn} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_n \end{bmatrix} + \begin{bmatrix} S_{ap} & S_{an} \\ S_{bp} & S_{bn} \\ S_{cp} & S_{cn} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_n \end{bmatrix} \quad (1)$$

$$\begin{aligned} i_a &= I_o \cos(\omega_o t + \varphi_o) \\ i_b &= I_o \cos(\omega_o t + \varphi_o - \frac{2\pi}{3}) \\ i_c &= I_o \cos(\omega_o t + \varphi_o + \frac{2\pi}{3}) \end{aligned} \quad (2)$$

where "S_x" are switching devices according to their phase positions as shown in Fig. 1, and they take values "1" or "0" when the corresponding switch is on or off accordingly. Also, in equation 2, the amplitude of the output current, output angular frequency and initial angle of the phase output current are I_0, ω_0, and φ_0 respectively.

The operational principle and the switching technique for the TTVSI are described briefly here. For positive i_a current, thyristor S_{tap} is first turned on with S_{tan} off. Transistor S_a is then switched on and off using any PWM technique. Within this period, positive current flows through S_{tap}, S_a, D_2, and D_{t2} as shown in Fig. 2(a). At the end of this positive half cycle; when current reaches zero, S_{tap} is turned off by removing the gate signal from S_a. After the recovery period of S_{tap}, S_{tan} is turned on with S_{tap} remaining off. Again, for this negative half cycle S_a is turned on and off using pulse width modulation. Also, in this period, negative current flows through D_1, D_{t1}, S_a, and S_{tan} as shown in Fig. 2(b). The basic strategy continues for the rest of the legs according to their phase order.



(a) (b)

Fig. 2. Basic operation and the commutation technique for phase "*a*": (a) positive, and (b) negative current flow.

III. PWM Control Scheme

To realize the circuit, conventional PWM schemes can be utilized for transistors' switching and thyristors' commutation. In [8] naturally sampled sine-triangle PWM (ST-PWM) technique was selected to investigate the TTVSI. However, the topology could be realized with any PWM scheme. In this paper different PWM techniques are used to analyze the circuit and compare its performance with the conventional six transistor VSI.

To program a desirable inverter output-voltage waveform, carrier based PWM techniques employ "per-carrier cycle volt-sec balance". Two major implementation techniques are: the triangular intersection method and the direct digital method [9]. One of the examples of the triangular intersection methods is the ST-PWM technique, where it uses a single triangular carrier signal to compare against three sinusoidal reference waveforms displaced in time by 120^o [8]. This type of modulation is generally termed double-edge naturally sampled modulation. Where the equations for phase voltages using ST-PWM are as follows

$$\begin{aligned} V_{az} &= V_o \cos\omega_o t = MV_{DC} \cos\omega_o t \\ V_{bz} &= V_o \cos(\omega_o t - \frac{2\pi}{3}) = MV_{DC} \cos(\omega_o t - \frac{2\pi}{3}) \\ V_{cz} &= V_o \cos(\omega_o t + \frac{2\pi}{3}) = MV_{DC} \cos(\omega_o t + \frac{2\pi}{3}) \end{aligned} \quad (3)$$

The fundamental target three-phase line-line output voltages are,

$$\begin{aligned} V_{ab} &= V_{az} - V_{bz} = M\sqrt{3}V_{DC} \cos(\omega_o t + \frac{\pi}{6}) \\ V_{bc} &= V_{bz} - V_{cz} = M\sqrt{3}V_{DC} \cos(\omega_o t - \frac{\pi}{2}) \\ V_{ca} &= V_{cz} - V_{az} = M\sqrt{3}V_{DC} \cos(\omega_o t + \frac{5\pi}{6}) \end{aligned} \quad (4)$$

where, V_0 = output voltage peak magnitude, M = modulation index = V_0/V_{DC}, and the reference waveforms are defined by considering "z" as a fictitious DC bus center point.

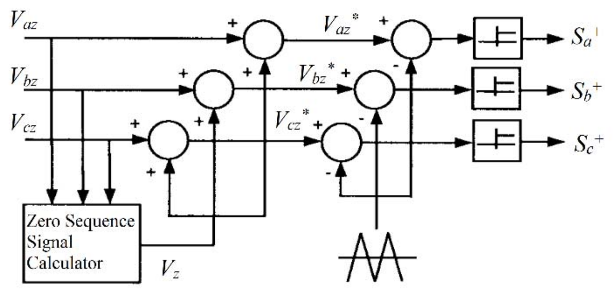


Fig. 3. The signal block diagram of the triangle intersection technique-based PWM employing the zero-sequence injection principle.

However, in case of ac motor drive applications, normally no neutral current path exists, therefore the neutral point is isolated. In such case, any zero sequence signals can be injected to the reference modulation signals. "V_z" is the potential difference between the neutral point "n" and the fictitious mid-point of the DC link voltage "z", it is the n-z potential and it can easily be changed according to the requirement. Fig. 3 shows this degree of freedom of the injected signals. A properly selected zero-sequence signal can extend the volt-second linearity range of ST-PWM. Furthermore, it can improve the waveform quality, modulation index, dc link voltage utilization, and reduce the switching losses significantly [8]. Thus, equation (3) becomes,

$$\begin{aligned} V_{az}^* &= V_{az}+V_z = V_o\cos\omega_o t = MV_{DC}\cos\omega_o t + V_z \\ V_{bz}^* &= V_{az}+V_z = V_o\cos(\omega_o t - \tfrac{2\pi}{3}) = MV_{DC}\cos(\omega_o t - \tfrac{2\pi}{3}) + V_z \\ V_{cz}^* &= V_{az}+V_z = V_o\cos(\omega_o t + \tfrac{2\pi}{3}) = MV_{DC}\cos(\omega_o t + \tfrac{2\pi}{3}) + V_z \end{aligned} \quad (5)$$

For a three phase inverter, the fundamental principle of space vector modulation is based on eight switching states which is conventionally implemented by the direct digital implementation method. Among the eight switching states, two states produce zero AC output line voltage: "0" (000) and "7" (111), and the remaining states produce non-zero output AC line voltage. A reference frame can be created containing these active vectors, shown in Fig. 4, where a rotating reference vector can be approximated in each switching cycle by switching between adjacent active vectors and the zero vectors. In order to maintain the effective switching frequency at a minimal value, the sequence of the toggling between these vectors is organized in such a manner that only one leg is affected in every step. Within sampling period, V^* is synthesized using adjacent vectors and zero vectors [8].

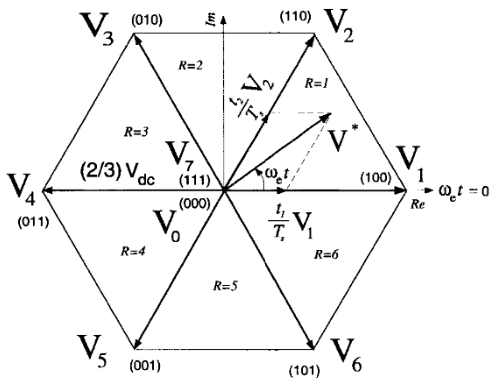


Fig. 4. The space vector diagram and its different sectors.

However, to achieve increased modulation index *"M"* a common mode third harmonic term can be injected into the fundamental reference [8],[9]. This way "*M*" can be increased over 1.0 without exceeding the over-modulation region. Including the third harmonic component the equation (5) becomes,

$$\begin{aligned} V_{az(ref+3)}^* &= V_{DC}[M\cos\omega_o t + M_3\cos 3\omega_o t] \\ V_{bz(ref+3)}^* &= V_{DC}[M\cos(\omega_o t - \tfrac{2\pi}{3}) + M_3\cos 3\omega_o t] \\ V_{cz(ref+3)}^* &= V_{DC}[M\cos(\omega_o t + \tfrac{2\pi}{3}) + M_3\cos 3\omega_o t] \end{aligned} \quad (6)$$

By including the third harmonic PWM (THPWM), the modulation index "M" can be increased to 1.15 before V_{az} reaches V_{DC}. In [9] it is determined that, theoretically, a 15% increase in the modulation index can be achieved only by injecting 1/6 third harmonic into the reference fundamental waveforms. Furthermore, the optimum amount of odd triplen harmonics (along with the 3rd harmonics) injection can increase in modulation index such that it exactly matches the amount what can be achieved by implementing the space vector modulation method.

The realization of the topology with direct zero SVPWM, and the commutation method are illustrated in Fig. 5(a) – 5(e). Fig. 5(a) illustrates the SVPWM generation for phase "a". The resulting switching pulses by PWM methods for per phase transistors are shown accordingly in Fig. 5(c), and 5(e). Moreover, thyristor firing pulses and their conduction periods are given pictorially in Fig. 5(b), and 5(d). It is to be noted that in these figures, small blocks represent the firing pulses but the larger rectangular blocks denote the conduction period of the thyristor.

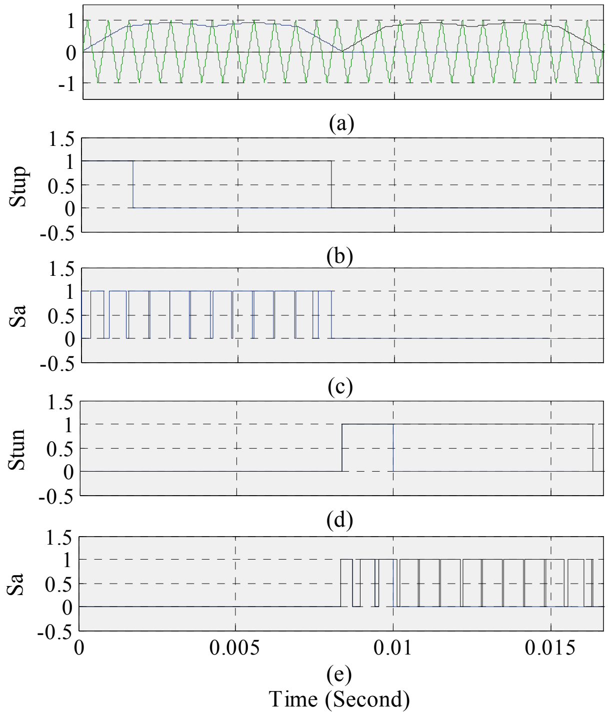


Fig. 5. PWM generation and switching pulses (a) SVPWM pulse generation method; (b) and (d) thyristor firing pulses and their conduction periods; (c), and (e) transistors switching pulses.

IV. Simulation Result

The TTVSI has been extensively investigated utilizing system level simulation with MATLAB/SIMULINK to analyze its performance. All the components and power semiconductor switches are used in the simulation software represents an ideal case. The simulation parameters are shown in Table I,

Table I Simulation Parameters

Parameter	Value
Input DC voltage, V_{DC}	220 V
Load Inductance, L	1 Ω
Load Resistance, R	0.5 mH
Carrier Frequency, f_c	2400 Hz
Modulation Index, M	0.8
Output Frequency, f_o	60 Hz

The TTVSI and the conventional VSI (CVSI) were realized with different carrier based PWM method to observe the performance difference between the new concepts against the conventional approach. As discussed earlier the PWM methods that have been utilized, are sine triangle PWM (ST-PWM), thrid harmonic PWM (THPWM), odd triplen harmonic PWM (TH-SVPWM) that shows exactly the same characteristics as the zero space vector PWM (SVPWM), and the SVPWM.

Simulation results of the TTVSI were obtained by utilizing the TH-SVPWM, and the direct SVPWM methods are illustrated from Fig. 6 to 9. Fig 6(a) shows the three phase output currents (e.g. $i_{a\ (p\text{-}p)}$ =108.9 A), Fig 6(b) depicts the output line to line voltages (e.g. $V_{ab\ (p\text{-}p)}$ =191.8 V), and Fig. 6(c) portrays the output phase voltages (e.g. $V_{az\ (p\text{-}p)}$ =109.5 V). Again Fig. 7 illustrates the total harmonic distortion (THD) of the output current waveform, which is 7.37 % for a 2400 Hz switching frequency. These results were achieved by using appropriate amount of the odd tiplen harmonic injected SVPWM method.

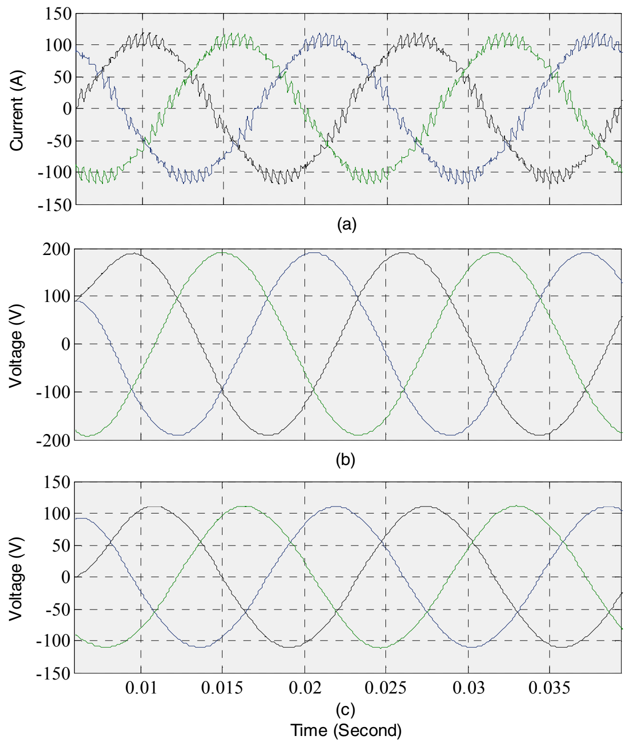


Fig. 6. Simulation result of the TTVSI topology utilizing TH-SVPWM technique, (a) three phase output currents; (b) output line voltages; (c) output phase voltages

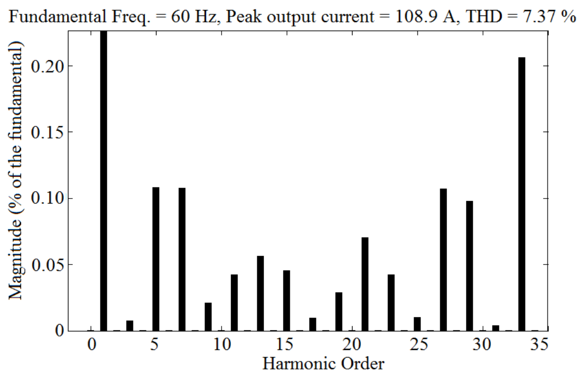


Fig. 7. THD of the output current utilizing TH-SVPWM

However, simulation results were obtained using the direct SVPWM method are shown in Fig. 8(a) – 8(c). Fig. 8(a) shows the three phase output currents (e.g. $i_{a\ (p\text{-}p)}$ =109.1 A), Fig. 8(b) depicts the output line to line voltages (e.g. $V_{ab\ (p\text{-}p)}$ =192.1 V), and Fig. 8(c) portrays the output phase voltages (e.g. $V_{az\ (p\text{-}p)}$ =109.9 V). Moreover, Fig. 9 illustrates the total harmonic distortion (THD) of the output current waveform, which is 7.38 % for a 2400 Hz switching frequency. From the simulation results it is evident that both PWM techniques show very close agreement. This result proves that the space vector concept adds odd triplen harmonic quantities to the basic PWM method in much the same manner as does the simple third harmonic injection technique.

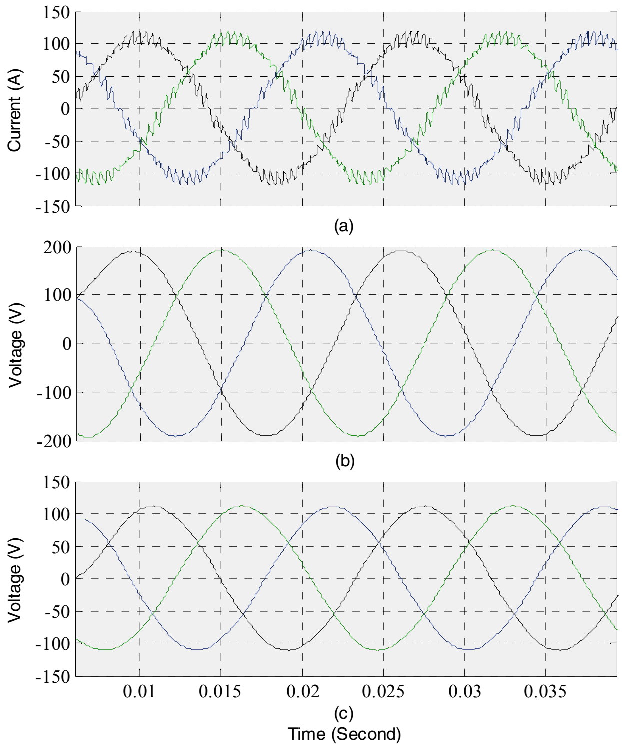


Fig. 8. Simulation result of the TTVSI topology utilizing SVPWM technique, a) three phase output currents; (b) output line voltages; (c) output phase voltages

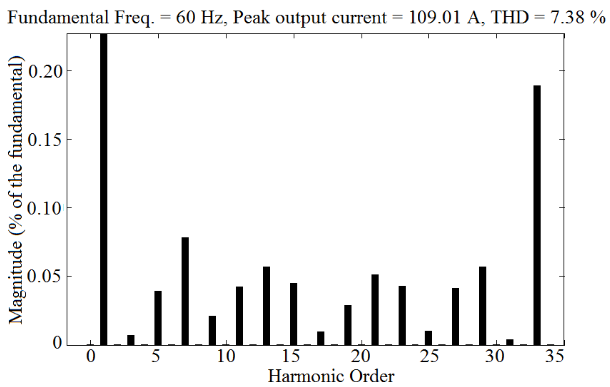


Fig. 9. THD of the output current of the utilizing SVPWM

Fig. 10 and Fig. 11 illustrate the simulation results of the conventional VSI using the direct SVPWM method. Fig. 10(a) shows the three phase output currents (e.g. $i_{a\,(p\text{-}p)}$ =112.2 A), Fig. 8(b) depicts the output line to line voltages (e.g. $V_{ab\,(p\text{-}p)}$ =197.9 V), and Fig. 8(c) portrays the output phase voltages (e.g. $V_{az\,(p\text{-}p)}$ =114.3 V). Moreover, Fig. 9 illustrates the total harmonic distortion (THD) of the output current waveform, which is 5.26 % for a 2400 Hz switching frequency. Because of the slight zero current intervals needed to allow the thyristors recover blocking ability a slight increase in the current THD was obtained compared to the conventional VSI.

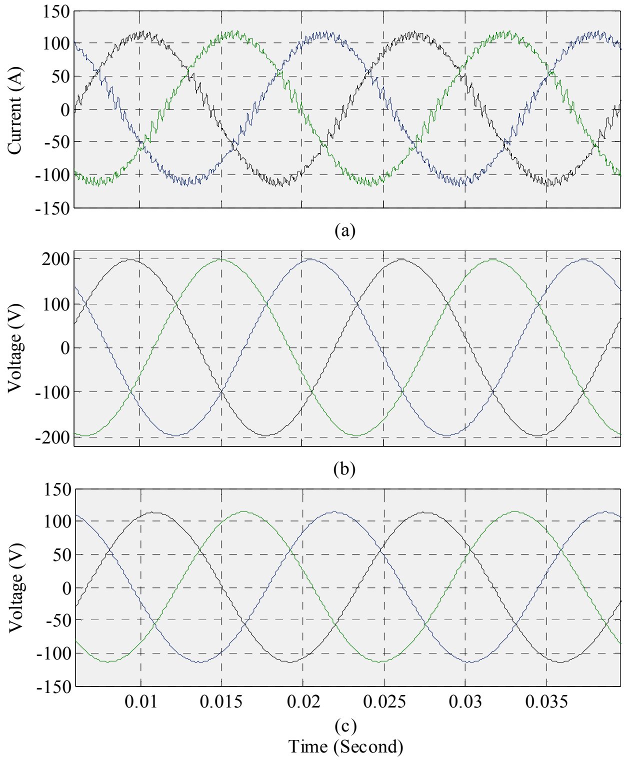


Fig. 10. Simulation result of the CVSI topology using the SVPWM technique, a) three phase output currents; (b) output line voltages; (c) output phase voltages

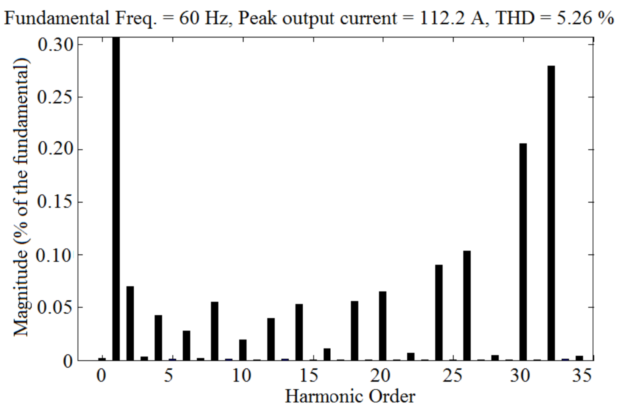


Fig. 11. THD of the output current of the conventional VSI using SVPWM method

Summary of the simulation result is show in the Table II. From the table it can be seen that, regardless the topology type, the lowest peak fundamental output line to line voltage was obtained by using the ST-PWM method. However, for both TTVSI and CVSI, when the THPWM was used, the line voltage was observed around 15.15% increased that of the line voltage obtained by the ST-PWM. Furthermore, the line to line voltage with the SVPWM method that had been generated by injecting appropriate amount of odd triplen harmonics to the fundamental reference signal was found approximately the exact as the zero space vector PWM technique for both conventional and the TTVSI topology.

TABLE II Summary of the Simulation Results

		ST-PWM	THPWM	SVPWM (TH)	SVPWM
Current (Amp)	TTVSI	93.65	107.4	108.9	109.1
	CVSI	97.19	110.3	111.8	112.2
THD (%)	TTVSI	9.75	7.46	7.37	7.38
	CVSI	6.51	5.49	5.28	5.26
Line Vo -ltage(V)	TTVSI	165.5	190.7	191.8	192.1
	CVSI	171.4	196.0	197.8	197.9

The same resulting trend can be observed for the output current value and the total harmonic distortion (THD) value for 2400 Hz switching frequency. From all the data found through the simulation show that, performance wise the conventional VSI obtained very slightly better results than the TTVSI. Furthermore, line voltages were found using different PWM scheme are very similar to the conventional topology (only 2.5% less). The reason for the slight dissimilarities is because the thyristor recovery time was considered as 6 times more than that of the data sheet. Also, it was achieved by chopping a portion of the fundamental reference signal. However, due to the flexibility of code writing in the experiment, the fundamental signal will not be required to chop off to provide the thyristor recovery time. Thus, with a small adjustment, the THD of the output current, the output current, and the line voltage could be improved.

V. CONCLUSIONS

The focal point of this paper is to analyze the performance of the TTVSI circuit using different PWM techniques. The performance and feasibility have been substantiated with a system level simulation. Performance wise it resembles conventional topologies but with certain advantages. This inexpensive topology shows promise to be an alternative solution for a mid to high power system where semiconductor electronic switches are very expensive. Alongside that the thyristors are commutated naturally without any external circuitry requirement by means of transistors' switching capability using different modulation techniques. Practical implementation of the TTVSI could provide greater DC link voltage utilization because it requires significantly less overall dead time than a conventional 6 transistor inverter. That is, unlike the conventional VSI this TTVSI requires dead times only at zero crossing instance of the output current since it consists of only one transistor per phase. One disadvantages of the topology is that the single transistor switch operates over a complete cycle. Therefore, the switching loss of the circuit is same as the conventional VSI topology. Moreover, the size of the single transistor will also be twice the conventional topology's single transistor. However, future topics of research will concern improvement of the switching technique, reduction of the harmonic content, and switching loss minimization. Moreover, the TTVSI could be investigated for a number of future power system applications at medium high power systems.

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